

THE POWER AND SPEED OF VISION



USER MANUAL

ELIIXA+ 16K/8K CXP MONOCHROME



Table of Contents

1 CAMERA OVERVIEW	5
1.1 Features	5
1.2 Key Specifications	5
1.3 Description.....	6
1.4 Typical Applications	6
1.5 Models	6
2 CAMERA PERFORMANCES	7
2.1 Camera Characterization	7
2.2 Image Sensor	8
2.3 Multi-Lines modes	8
2.4 Response & QE curves.....	9
2.4.1 Quantum Efficiency	9
2.4.2 Spectral Response	9
3 CAMERA HARDWARE INTERFACE.....	11
3.1 Mechanical Drawings.....	11
3.2 Input/output Connectors and LED.....	12
3.2.1 Power Over CoaXPress	13
3.2.2 Status LED Behaviour.....	13
3.2.3 Trigger Connector	14
4 STANDARD CONFORMITY	15
4.1 CE Conformity.....	15
4.2 FCC Conformity.....	15
4.3 RoHs Conformity.....	15
5 GETTING STARTED	16
5.1 Out of the box.....	16
5.2 Setting up in the system	16
6 CAMERA SOFTWARE INTERFACE.....	17
7 Camera Commands	18
7.1 Device Control	18
7.2 Image Format	20
7.2.1 Structure of the Sensor.....	21
7.2.2 Binning modes	21

7.2.3 Multi-Line Gain	22
7.2.4 HDR mode (Only available on “BH0” Models).....	22
7.2.5 Test Image Pattern Selector	23
7.3 Acquisition Control	24
7.3.1 External Triggers on GPIO Connector	25
7.3.2 CXP Trigger Line	25
7.3.3 Scan Direction.....	26
7.3.4 Full Exposure Control Mode	27
7.3.5 GenICam Triggers	29
7.3.6 Trigger Presets	30
7.3.7 Rescaler	31
7.4 Digital I/O Control.....	32
7.5 Counters & Timers Control	34
7.5.1 Counters	34
7.5.2 Timers	36
7.6 Gain and Offset.....	37
7.7 Flat Field Correction	40
7.7.1 Automatic Calibration.....	43
7.7.2 Manual Flat Field Correction	43
7.7.3 Save & Restore FFC in User Memory Banks	44
7.8 Look Up Table	45
7.8.1 Save & Restore LUT in User Memory Banks.....	45
7.9 Statistics and Line Profile.....	47
7.10 Privilege Level.....	48
7.11 Save & Restore Settings in User Memory Banks	49
APPENDIX	50
Appendix A. Test Patterns	51
A.1 Test Pattern 1: Vertical wave	51
A.2 Test Pattern 2: Fixed Horizontal Ramps	51
A.1.2 In 8 bits (Full) format – No Binning (16384 pixels).....	51
A.2.2 In 12 bits (Medium) format – No Binning (16384 pixels).....	52
A.3.2 In 8/12 bits Full/Medium format with Binning (8192 Pixels).....	53
Appendix B. Timing Diagrams	54
B.1 Synchronization Modes with Variable Exposure Time	54
B.2 Synchronisation Modes with Maximum Exposure Time.....	55

B.3 Timing Values	55
Appendix C. HDR Mode	56
C.1 HDR Block	56
C.2 Example with Ratio 2 and 10bits output	56
C.3 HDR With LUT 10bits => 8bits	57
C.4 Example of difference between “AB” and “C” Line :	57
Appendix D. Data Cables	58
Appendix E. Lenses Compatibility	59
Appendix F. Revision History	60

1 CAMERA OVERVIEW

1.1 Features

- Cmos Sensor 4x 16384 Pixels, 5 x 5µm
- Multi-Line structure (1, 2 or 4 lines to adapt the sensitivity)
- Interface :
 - CoaXPress® (4x Links)
- Line Rate :
 - Up to 100000 l/s
- Data Rate :
 - Up to 1,6GB/s in CoaXPress®
 - > CXP-3 : 4x3,125 Gbps
 - > CXP-6 : 4x6,25 Gbps
- Bit Depth : 8, 10 or 12bits
- Flat Field Correction
- Look Up Table
- Low Power Consumption : <18W
- Compliant with Standard Lenses of the Market
- Full Exposure Control, even in 4S “TDE” mode
- New Sensor version and HDR mode on “BH0” Models



1.2 Key Specifications

Note : All values in LSB is given in 12 bits format

Characteristics	Typical Value		Unit
Sensor Characteristics at Maximum Pixel Rate			
Resolution	4 x 16384	4 x 8192	Pixels
pixel size (square)	5 x 5	10 x 10	µm
Max line rate	100	100	kHz
Radiometric Performance at Maximum Pixel Rate and minimum camera gain			
Bit depth	8, 10, 12		Bits
Response (broadband)	450		LSB/(nJ/cm ²)
Full Well Capacity	27300 (in 2S or 4S mode and MultiGain at 1/2)		electrons
Response non linearity	0,3		%
PRNU HF Max	3		%
Dynamic range (1S / 2S / 4S mode)	67,6 / 70,7 / 68,7		dB

Functionality (Programmable via GenICam Control Interface)		
Analog Gain	Up to 12 (x4)	dB
Offset	-4096 to +4096	LSB
Trigger Mode	Timed (Free run) and triggered (Ext Trig, Ext ITC) modes	
Mechanical and Electrical Interface		
Size (w x h x l)	100 x 156 x 36	mm
Weight	700	g
Lens Mount	M95 x 1	-
Sensor alignment (see chapter 4)	±100	µm
Sensor flatness	±35	µm
Power supply	Power Over CoaXPress : 24	V
Power dissipation – Typ. while grabbing	< 18	W
General Features		
Operating temperature	0 to 55 (front face) or 70 (Internal)	°C
Storage temperature	-40 to 70	°C
Regulatory	CE, FCC and RoHS compliant	

1.3 Description

e2v's next generation of line scan cameras are setting new, high standards for line rate and image quality. Thanks to e2v's recently developed multi line CMOS technology, the camera provides an unmatched 100 000 lines/s in a 16k pixel format and combines high response with an extremely low noise level; this delivers high signal to noise ratio even when short integration times are required or when illumination is limited. The 5µm pixel size is arranged in four active lines, ensuring optimal spatial resolution in both scanning and sensor directions with off-the-shelf lenses. An outstanding data rate in excess of 1.6 Gpixels per second, delivered via a new CoaXPress interface, allows for extremely high throughput and opens up an array of new possibilities for the next generation of inspection systems for demanding applications such as flat panel display, PCB and solar cell inspection.

1.4 Typical Applications

- Flat Panel Display Inspection
- PCB Inspection
- Solar Cell Inspection
- Glass Inspection
- Print Inspection

1.5 Models

Part Number	Sensor	Details	Max Line Rate
EV71YC4MCP1605-BA0	4x Lines, 16k 5µm x 5µm	-	100 KHz
EV71YC4MCP1605-BH0	4x Lines, 16k 5µm x 5µm	New Sensor + HDR Modes	100 KHz

2 CAMERA PERFORMANCES

2.1 Camera Characterization

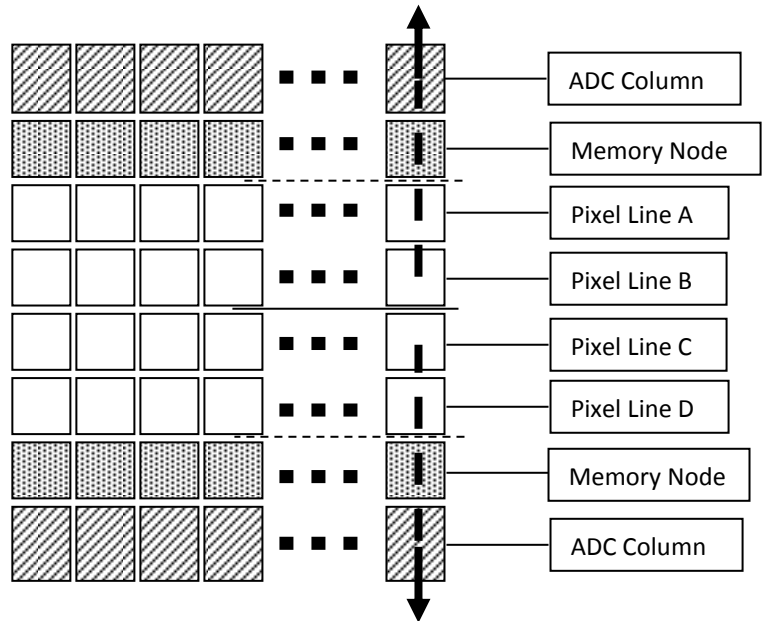
	Unit	Mode 1S (0dB)			Mode 2S (0dB)			Mode 4S (0dB)		
		Min	Typ.	Max	Min	Typ.	Max	Min	Typ.	Max
Dark Noise RMS	LSB	-	1,7	2,2		2,4	3,1		3	4
Dynamic Range	-	-	2394:1	-	-	3412:1 ^(*)	-	-	2730:1 ^(*)	-
Readout Noise	e-	-	5,7	-	-	8	-	-	10	-
Full Well Capacity	e-	-	13650	-	-	27300	-	-	27300	-
SNR	dB	-	40	-	-	43 ^(*)	-	-	43 ^(*)	-
Peak Response (660nm)	LSB/ (nJ/cm ²)	-	137	-	-	274	-	-	547	-
Non Linearity	%	-	0,3	-	-	0,3	-	-	0,3	-
Without Flat Field Correction :										
FPN rms	LSB	-	0,4	1,5	-	0,7	1,5	-	0,8	1,5
FPN pk-pk	LSB	-	3,2	15	-	5	15	-	5,6	15
PRNU hf (3/4 Sat)	%	-	0,13	0,25	-	0,1	0,25	-	0,1	0,25
PRNU pk-pk (3/4 Sat)	%	-	1	3	-	0,8	3	-	0,8	3

Test conditions :

- Figures in LSB are for a 12bits format.
- Measured at exposure time = 50μs and line period = 50μs in Ext Trig Mode (Max Exposure Time)
- Maximum data rate
- Stabilized temperature 30/40/55 °C (Room/Front Face/Internal)
- SNR Calculated at 75% Vsat with minimum Gain.
- (*) In mode 2S/4S, only with the use of the Multi-Line Gain

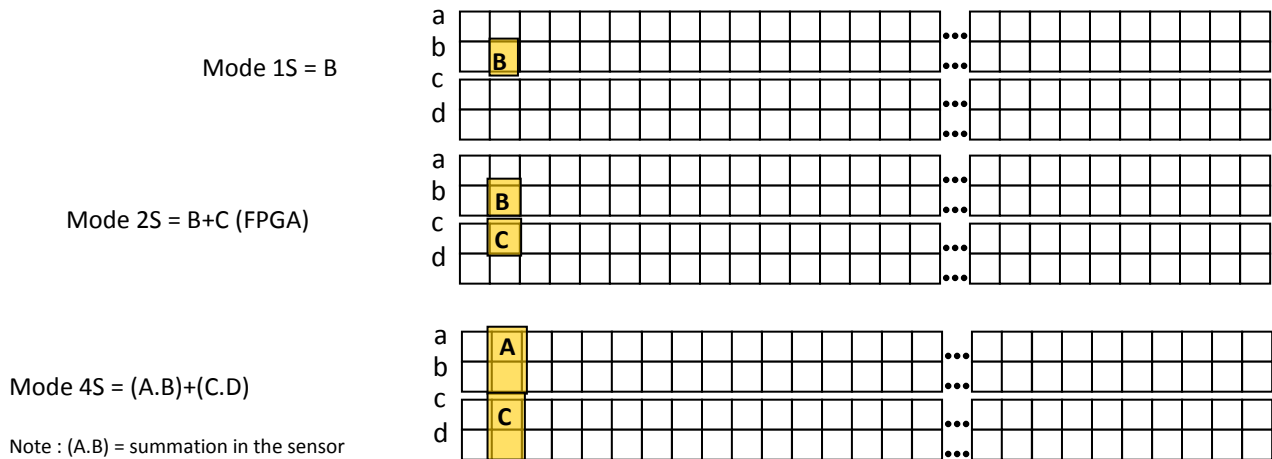
2.2 Image Sensor

The Eliixa+ 16k sensor is composed of two pairs of sensitive lines. Each pair of lines use the same Analog to Digital Column converter (ADC Column). An appropriate (embedded) Time delay in the exposure between each line this allows to combine two successive exposures in order to double the sensitivity of a single line. This Time Delay Exposure is used only in the 4S multi-line modes (4 Lines) as described below. The 16384 Pixels of the whole sensor are divided in 4 blocks of 4096 pixels.

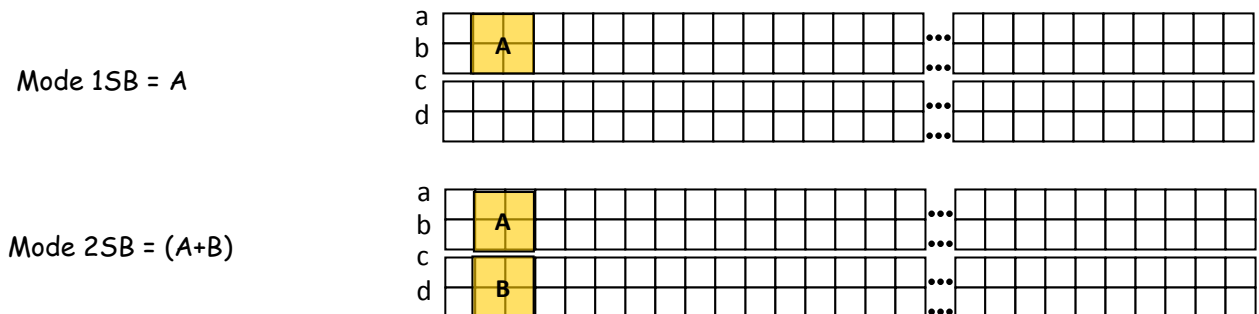


2.3 Multi-Lines modes

Multi-Lines Modes (16k Pixels Output)

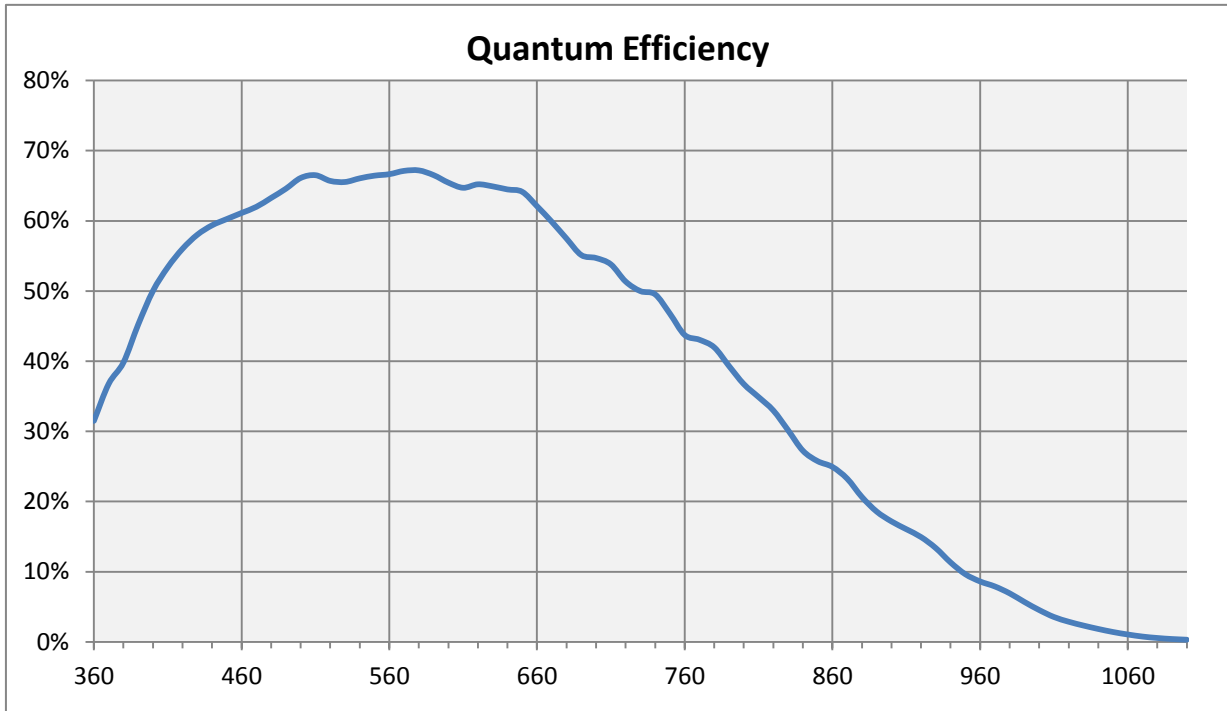


Binning Modes (8k Pixels Output)



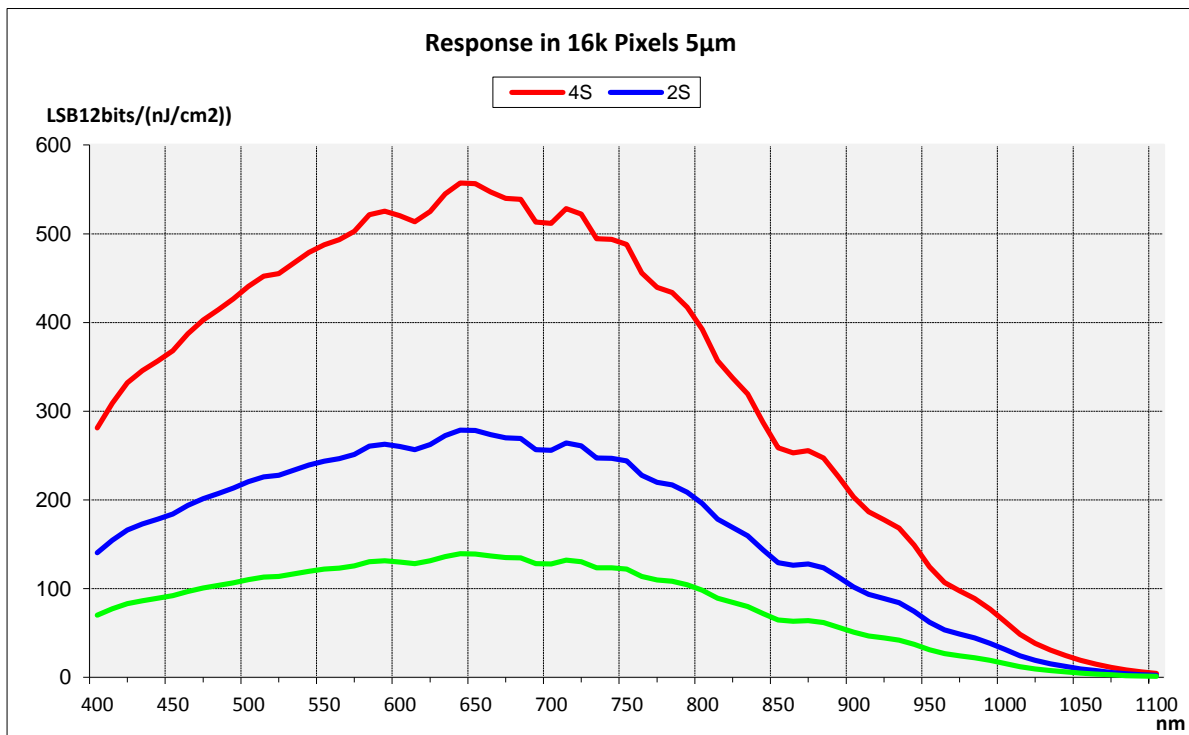
2.4 Response & QE curves

2.4.1 Quantum Efficiency

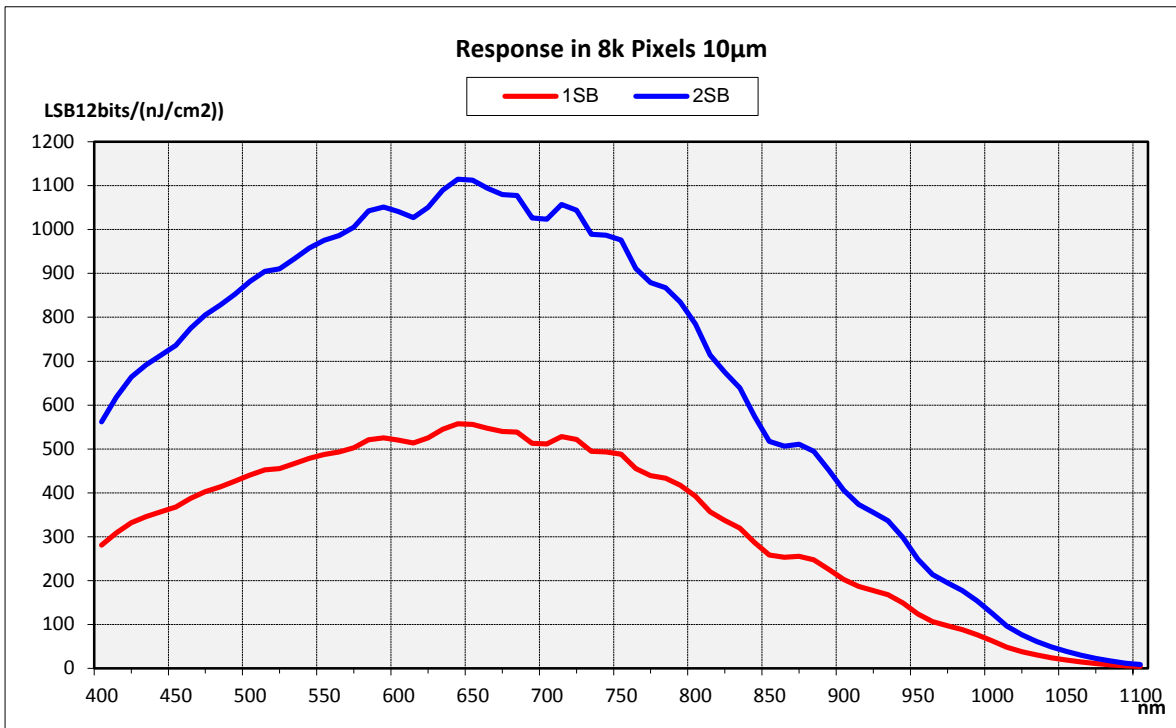


2.4.2 Spectral Response

Single Modes : 1S, 2S, 4S

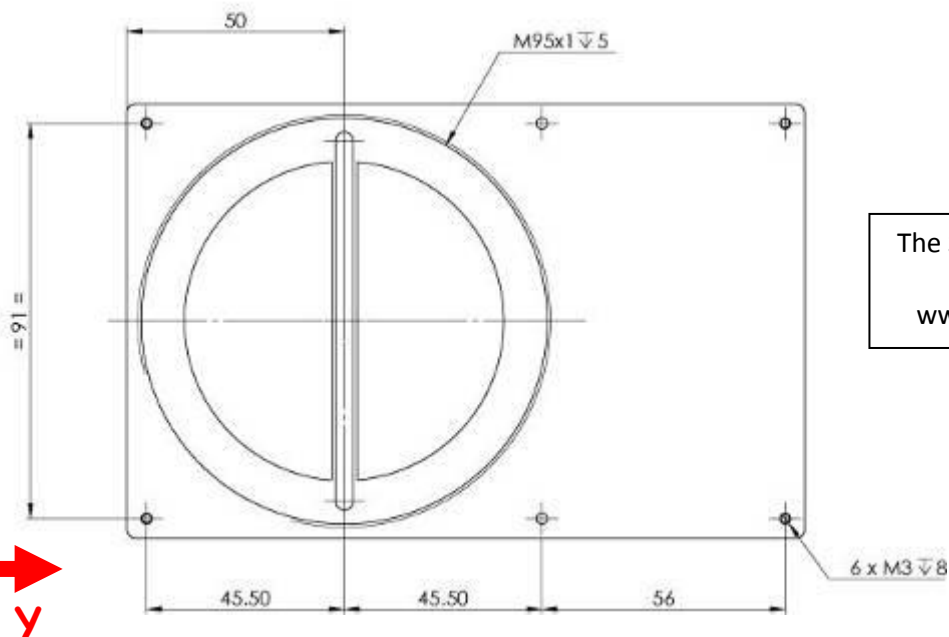
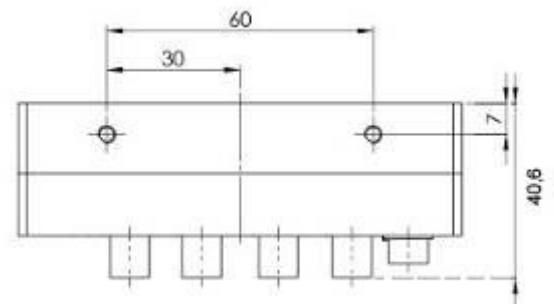
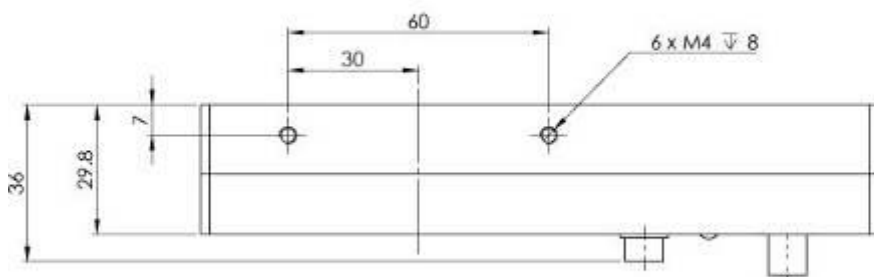
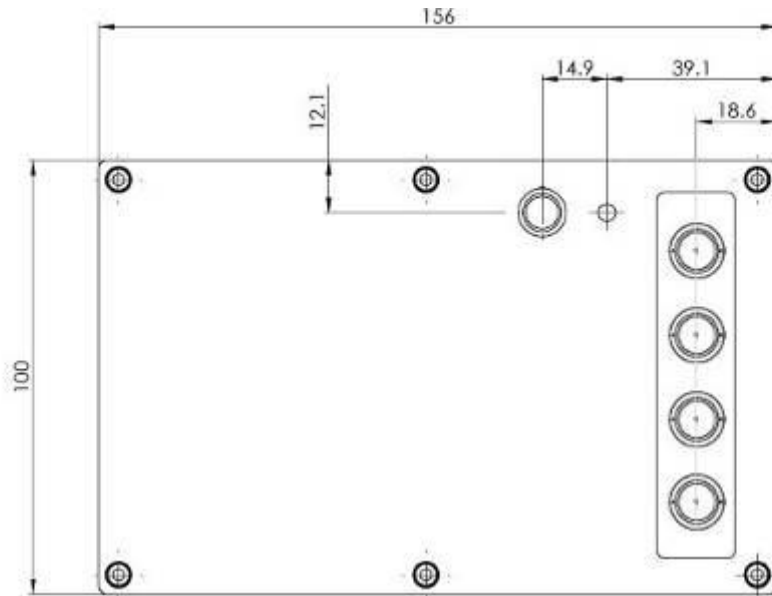


Binning Modes : 1SB, 2SB



3 CAMERA HARDWARE INTERFACE

3.1 Mechanical Drawings



The Step file is available on
the web :
www.e2v.com/cameras

Sensor alignment	
Z = -9.4 mm	±100µm
X = 9 mm	±100 µm
Y = 50mm	±100 µm
Flatness	±50 µm
Rotation (X,Y plan)	±0,1°
Tilt (versus lens mounting plane)	50µm

3.2 Input/output Connectors and LED



3.2.1 Power Over CoaXPress

The ELIIXA+ CXP is compliant with the Power Over CoaXPress : There is no Power connector as the power is delivered through the Coaxial Connectors 1 and 2.

In the Standard, the Power Over CoaXPress allows to deliver 13W (under 24V) per Channel.

The ELIIXA+ CXP requires 18W then two connectors are required for the power : The two first are used for this purpose.










If you want to Power ON the Camera you have to connect the Coaxial connector output 1 of the camera to the coaxial connector 1 of the Frame Grabber.

Note 1 : Only the connector 1 position is mandatory. The 3 others connectors can be inverted but the camera still needs the 2 first connectors to get it power and be able to start up.

Note 2 : With some frame grabber you have access to a specific command (from the Frame Grabber interface) for shutting down/up the power of the CoaxPress : This solution, with the complete reboot, is the better solution to ensure a complete power On of the Camera.

3.2.2 Status LED Behaviour

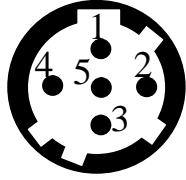
The Power LED behavior detail is the following :

Colour and State		Meaning
Off		No power
Solid orange		System booting
Fast flash green Shown for a minimum of 1s even if the link detection is faster		Link detection in progress
Slow flash alternate red / green		Device / Host incompatible
Slow pulse green		Device / Host connected, but no data being transferred
Slow pulse orange		Device / Host connected, waiting for event (e.g. trigger, exposure pulse)
Solid green whenever data transferred (i.e. blinks synchronously with data)		Device / Host connected, data being transferred
500ms red pulse In case of multiple errors, there shall be at least 200ms green before the next error is indicated		Error during data transfer (e.g. CRC error, single bit error detected)
Fast flash red		System error (e.g. internal error)

3.2.3 Trigger Connector

Camera connector type: Hirose HR10A-7R-5SB or compliant

Cable connector type: Hirose HR10A-7P-5P (male) or compliant, Provided with the Camera

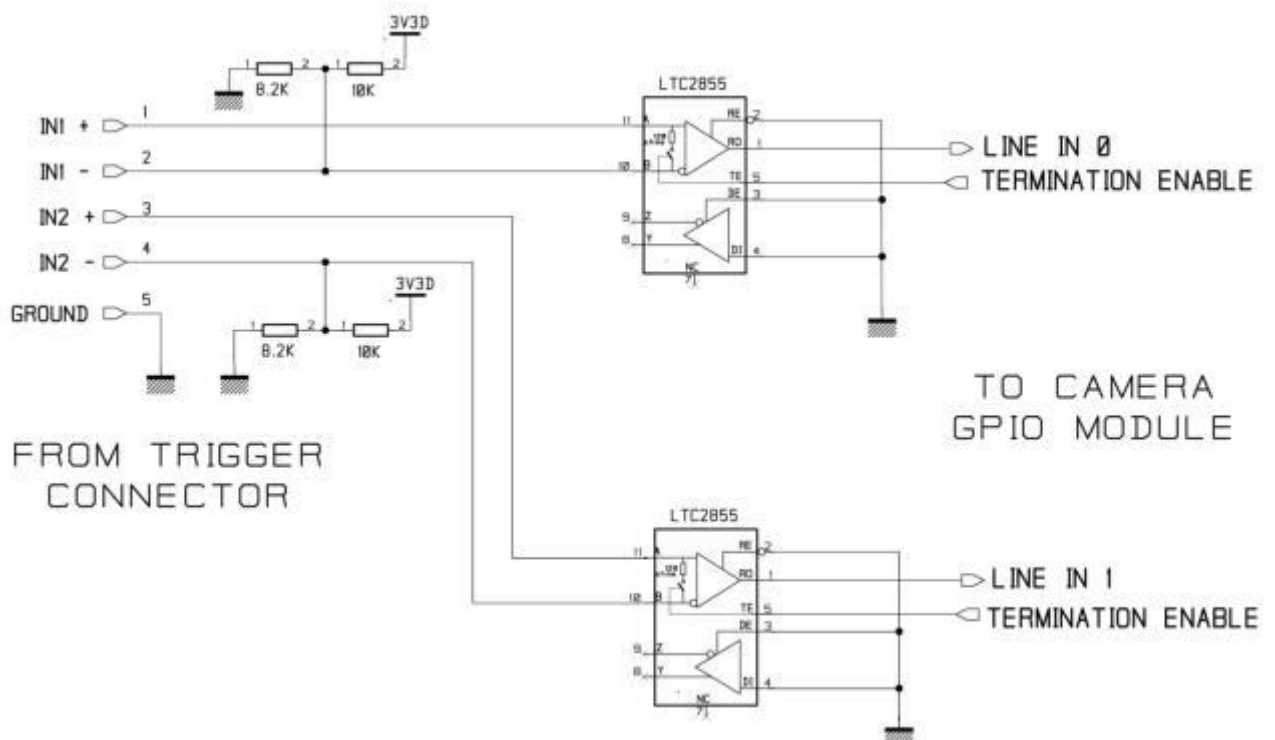


Receptacle viewed from camera back

Signal	Pin
LVDS IN1+ / TTL IN1	1
LVDS IN1-	2
LVDS IN2+ / TTL IN2	3
LVDS IN2-	4
GND	5

IN1/IN2 are connected respectively to Line0/Line1 and allow to get external line triggers or the forward/Reverse “Live” indication.

On the Connector side, the 120Ω termination is validated only if the input is switched in LVDS or RS422. The electrical schematic is detailed below :



4 STANDARD CONFORMITY

The ELIIXA+ cameras have been tested using the following equipment:

- A shielded Trigger cable
- A 10m CoaXPRESS Cable for the data transfer, certified at 6Gb/s

e2v recommends using the same configuration to ensure the compliance with the following standards.

4.1 CE Conformity

The ELIIXA+ cameras comply with the requirements of the EMC (European) directive 2004/108/CE (EN50081-2, EN 61000-6-2) (see next page).

4.2 FCC Conformity

The ELIIXA+ cameras further comply with Part 15 of the FCC rules, which states that: Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation

This equipment has been tested and found to comply with the limits for Class A digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

4.3 RoHS Conformity

ELIIXA+ cameras comply with the requirements of the RoHS directive 2011/65/EU.

5 GETTING STARTED

5.1 Out of the box

The contains of the Camera box is the following :

- One Camera ELIIXA+
- Trigger connector (Hirose HR10A-7P-5P-male or compliant)

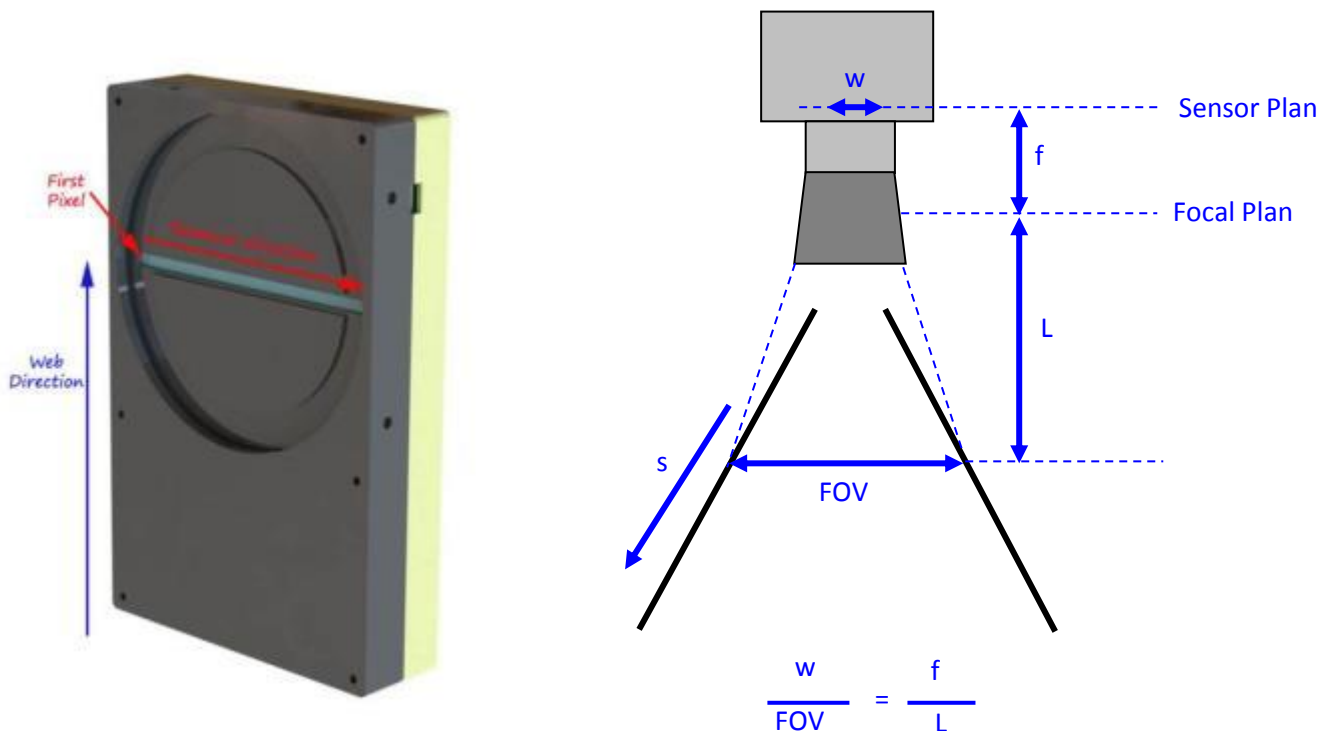


There is no CDROM delivered with the Camera : This User Manual , and any other corresponding documents can be dowlaoded on the Web site.

Main Camera page : www.e2v.com/cameras

Select the appropriate Camera Page (ELIIXA+)

5.2 Setting up in the system



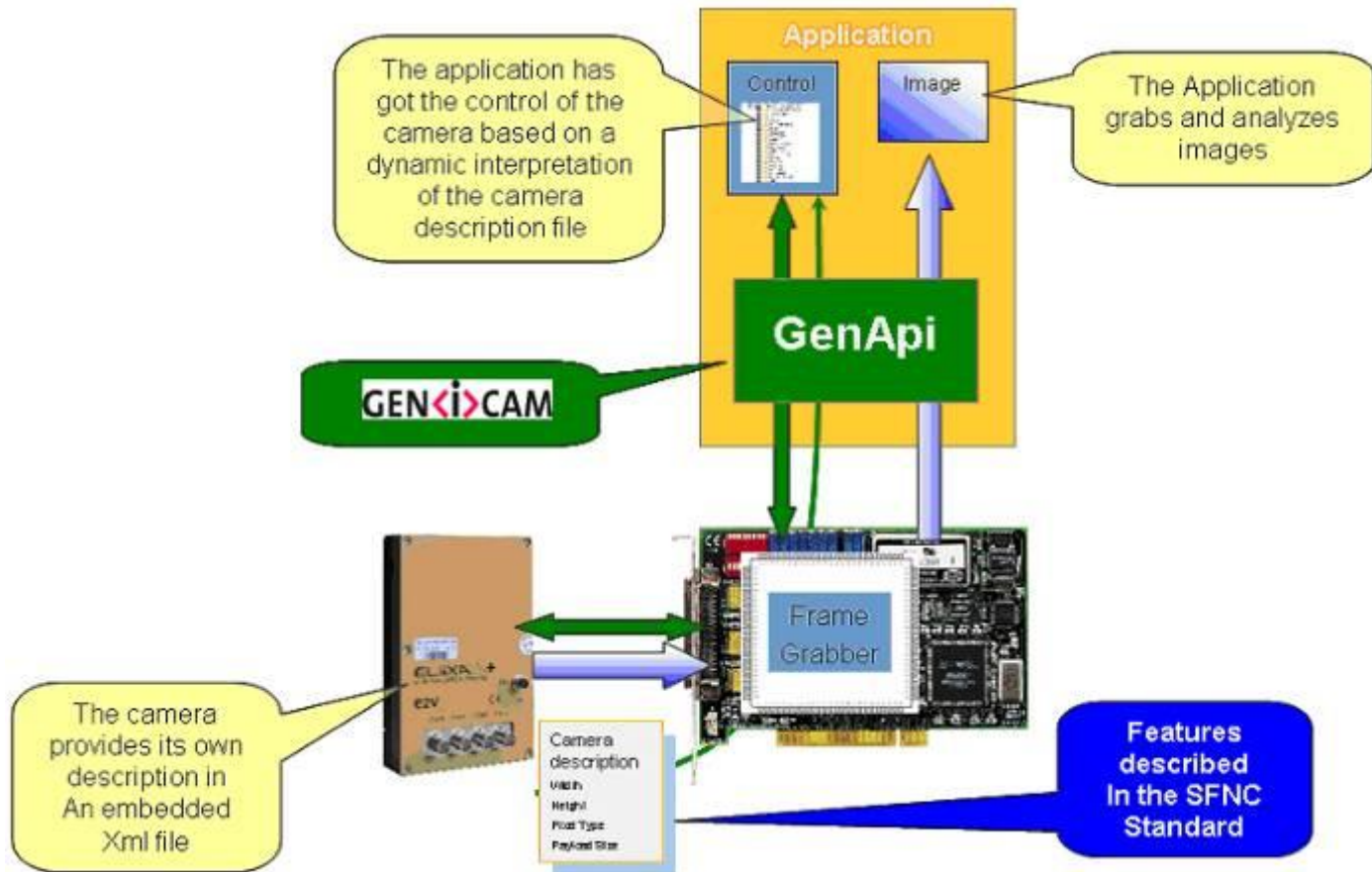
The Compliant Lenses and their accessories are detailed in Appendix E

6 CAMERA SOFTWARE INTERFACE

The ELIXA+ CoaxPress Camera is compliant with **GenICam 2.1 and the SFNC 1.5** standards.

This means that the Camera embeds its own definition and parameter description in an xml file.

Most of these Parameters are compliant with the SNFC. The specific parameters (non SNFC) are still compliant with GenICam and can be detailed through the GenICam API process to the application.



The Frame Grabber software is supposed to propose a feature Brother, based on GenICam, which lists and allows the modification of the parameters of the Camera.

This feature brother based on GenICam API uploads the xml file of the parameters description embedded in the Camera.

Then the following description of the parameters and commands is based on the GenICam name of these parameters. Behind each parameter is a register address in the Camera memory.

The mapping of these registers is not given in this manual because it can change from one version or the firmware to the next one.

7 Camera Commands

7.1 Device Control

These are Identification values of the Camera. They can be accessed in the “Device Control” section

Feature	CXP @	Size in bytes	R/W	Description
DeviceVendorName	0x02000 Bootstrap	32	RO	Get camera vendor name as a string (including '\0')
DeviceModelName	0x02020 Bootstrap	32	RO	Get camera model name as a string (including '\0')
DeviceManufacturerInfo	0x02040 Bootstrap	48	RO	Get camera ID as a string (including '\0')
DeviceVersion	0x02070 Bootstrap	32	RO	Get camera version as a string (hardware version) (including '\0')
DeviceFirmwareVersion	0x02090 Bootstrap	32	RO	Get camera synthetic firmware version (PKG version) as a string (including '\0')
DeviceSFNCVersionMajor	Xml		RO	
DeviceSFNCVersionMinor	Xml		RO	
DeviceSFNCVersionSubMinor	Xml		RO	
DeviceID	0x020B0 Bootstrap	16	RO	Read Serial Nb
DeviceUserID	0x020C0 Bootstrap	16	RW	Get device user identifier as a string (including '\0')
ElectronicBoardID	0x08000	32	RO	Read Electronic Board ID
ElectronicBoardTestStatus	0x08020	16	RO	Read Electronic board status
DeviceFirmwareVersion	0x02090 Bootstrap	32	RO	Get camera synthetic firmware version (PKG version) as a string (including '\0')
DeviceTemperature	0x08E04	4	RO	Read Main board internal temperature (format signed Q10.2 = signed 8 bits, plus 2 bits below comma. Value from -512 to +511) in °C
DeviceTemperatureSelector	Xml		RO	Device Temperature selector
Standby	0x08E08	4	RW	0 :Disable standby mode (“False”) 1 :Enable standby mode (“True”), no more video available but save power and temperature
STATUS REGISTER	0x08E0C	4	RO	
StatusWaitForTrigger				Bit 0: true if camera waits for a trigger during more than 1s
Status trigger too fast				Bit 1: true if camera trigger is too fast
StatusSensorConnexion				Bit 2: true if sensor pattern checking has failed
Status3V7				Bit 3: true if 3V7 failure
Status3V3				Bit 4: true if 3V3 failure
Status1V0				Bit 5: true if 1V0 failure
Status1V8				Bit 6: true if 1V8 failure
Status1V8ANA				Bit 7: true if 1V8ANA failure
StatusWarningOverflow				Bit 8: true if a an overflow occurs during FFC calibration

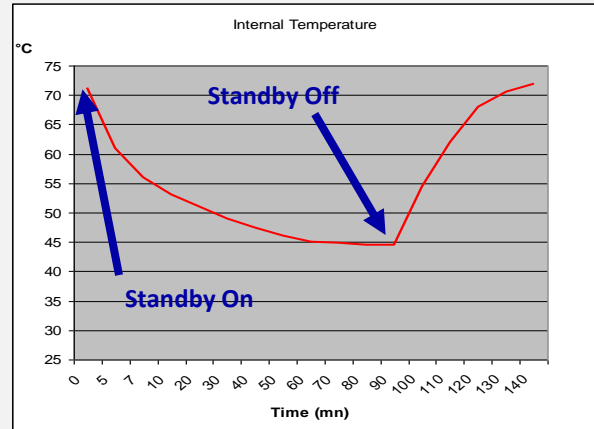
				or Tap balance (available only for integrator/user mode)
StatusWarningUnderflow				Bit 9: true if a an underflow occurs during FFC calibration or Tap balance (available only for integrator/user mode)
Status2V5				Bit 10: true if 2V5 failure
CC3 Scrolling direction				Bit 11: 0 : forward, 1: reverse
StatusErrorHardware				Bit 16 : true if hardware error detected



A standby mode, what for ?

The Standby mode stops all activity on the sensor level. The power dissipation drops down to about **6W**. During the standby mode, **the grab is stopped**

Once the Standby mode turned off, the Camera recovers in less than **1ms** to send images again from the sensor.



7.2 Image Format

Feature	CXP @	Size in bytes	R/W	Description
Width	0x07000	4	RO	Mapped on SensorWidth : 16384 or 8192 in binning mode
Height	0x07004	4	RO	
AcquisitionMode	0x07008		RW	1: Continuous
AcquisitionStart	0x0700C		WO	0: Start the acquisition
AcquisitionStop	0x07010		WO	0: Stop the acquisition
PixelFormat	0x07014	4	RW	0x0101: Mono8 0x0102: Mono10 0x0103: Mono12
PixelCoding	NA	-	RO	Mono
PixelSize	NA	-	RO	Bpp8, Bpp10 or Bpp12 depending on PixelFormat
PixelColorFilter	NA	-	RO	None
PixelDynamicRangeMin	NA	-	RO	0
PixelDynamicRangeMax	NA	-	RO	255, 1023 or 4095 depending on PixelFormat
SensorWidth	0x08200	4	RO	Get sensor physical width.
SensorHeight	Xml		RO	
WidthMax	-		RO	Mapped on SensorWidth : 16384 or 8192 in binning mode
HeightMax	Xml		RO	
SensorMode	0x08204	4	RW	0: Set sensor mode to DualLine "1S" 1: sensor mode to MultiLine "2S" 2: Set sensor mode to QuadriLine "4S" 3: Set sensor mode to Binning MonoLine "1SB" 4: Set sensor mode to Binning DualLine "2SB" 5 : Set in HDR Mode
MultiLineGain	0x08208	4	RW	0: Set MultiLine gain to "x1" 1: Set MultiLine gain to "x1/2" : not available if SensorMode = 0 ("1S" mode)
ReverseReading	0x08210	4	RW	0: Set reverse reading to "disable" 1: Set reverse reading to "enable"
TestImageSelector	0x08214	4	RW	0: Set test (output FPGA) image pattern to "Off", processing chain activated 1: Set test (output FPGA) image pattern to "GreyHorizontalRamp", processing chain disabled 2: Set test (output FPGA) image pattern to "White pattern", processing chain disabled 3: Set test (output FPGA) image pattern to "gray pattern", processing chain disabled 4: Set test (output FPGA) image pattern to "Black pattern", processing chain disabled 5: Set test (output FPGA) image pattern to "GreyVerticalRampMoving", processing chain disabled
InputSource	0x08218	4	RW	0: Set signal source to CMOS sensor, processing chain activated
HDRMode	0x08234	4	RW	Set The Output in HDR Mode (when SensorMode = HDR) Only available on "BH0" Models 0: Bottom Line Only 1: Top Line Only 2: HDR Line (Top + Bottom Combined)
HDR Ratio	0x08238	4	RW	Set The Output in HDR Ratio (when SensorMode = HDR) Only available on "BH0" Models

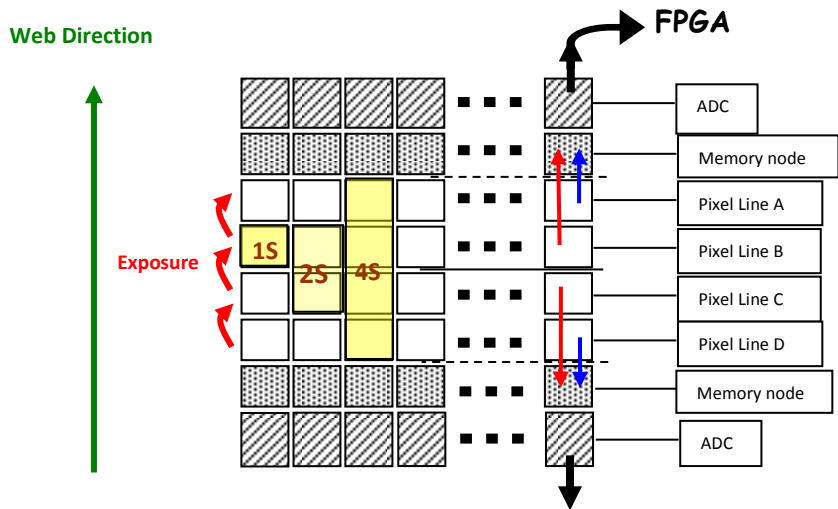
Feature	CXP @	Size in bytes	R/W	Description
				0: HDR Ratio 1 (or x2) 1: HDR Ratio 2 (or x4) 2: HDR Ratio 4 (or x8) 2: HDR Ratio 8 (or x16)

7.2.1 Structure of the Sensor

In 2S Mode, the summation of the two lines is done in the FPGA : **B+C**

In 4S Mode, the summation of the two double lines is done in the FPGA : **(AB)+ (BC)**

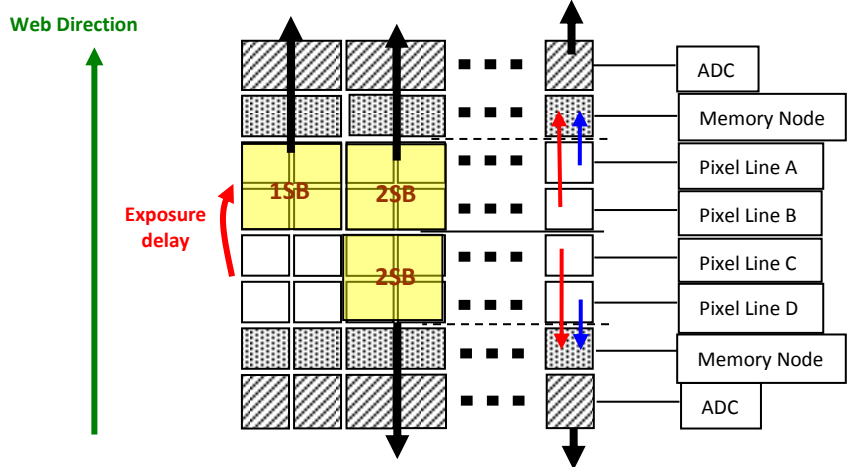
Eventually if the MultiLine Gain is set to $\frac{1}{2}$ (see below), this calculation will be : $\frac{1}{2} (AB) + \frac{1}{2}(BC)$



7.2.2 Binning modes


The two binning modes give an output of 8k pixels 10x10 μ m.

As for the 2S mode, the sensor manages the delay between the exposure necessary for a good acquisition when the double binning (2SB) mode is used.




7.2.3 Multi-Line Gain

The Multi-Line Gain is a feature that can be used only when the Top and the Bottom of the Sensor are used and summed in the FPGA to increase the sensitivity (2S, 4S and 2SB Modes)
 The Multi-Line Gain of x1/2 is applied in the FPAG just before the summation of the Top and Bottom Information of the Sensor.




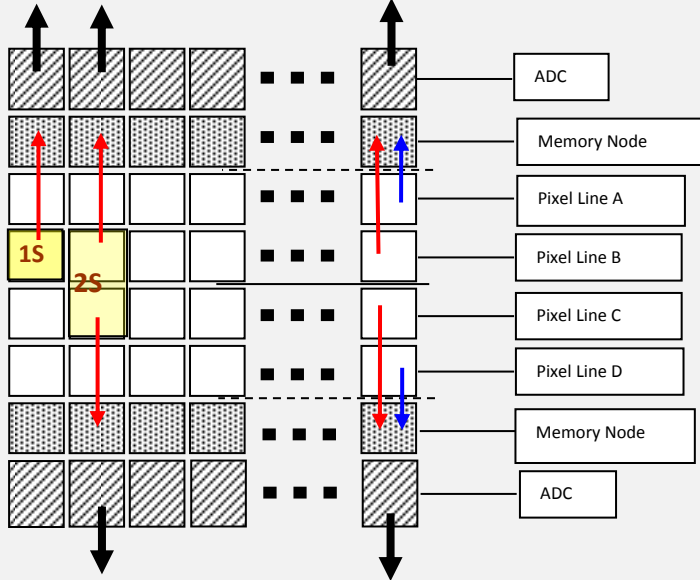
Why Using a Multi-Line Gain of x0,5 ?

Web Direction



Exposure delays



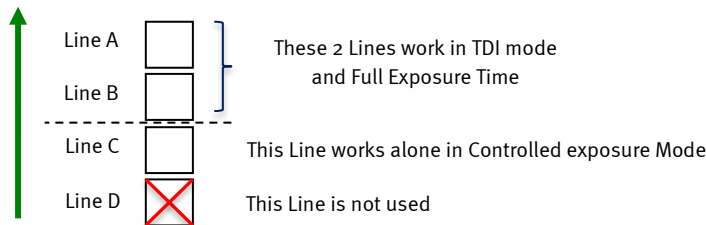


When the Light source is enough to use the “1S” mode of the Sensor (one single line), the best is to use 2 lines (“2S” mode) and then to divide the result by two by using the Multi-Line Gain set at “x0,5” :

In this case, the Full Well capacity is multiplied by x2 (two output registers are used) but the noise divided by $\sqrt{2}$ therefore the SNR is improved by a factor of $\sqrt{2}$.

7.2.4 HDR mode (Only available on “BH0” Models)

The High Dynamic Range Mode is using the top and bottom couple of lines of the sensor in a different way in order to get 2 different exposures that can be combined to give a High Dynamic range result :



There are three different possible outputs when the HDR mode is set :

- Single Line Bottom only : Line “C” only is outputted to check the High Levels
- Single Line Top only : Line “A+B” is outputted to check the Low Levels
- Single Line HDR : The Camera outputs the HDR Line reconstructed from “A+B” and “C” Lines in the camera in the “HDR” bloc.

The Exposition of the “C” Line is automatically controlled by setting the HDR Ratio :

- Ratio 1 : Equivalent to x2 ratio between Top and Bottom or 1 bit in the Dynamic
- Ratio 2 : Equivalent to x4 ratio between Top and Bottom or 2 bit in the Dynamic
- Ratio 4 : Equivalent to x8 ratio between Top and Bottom or 3 bit in the Dynamic
- Ratio 8 : Equivalent to x16 ratio between Top and Bottom or 4 bit in the Dynamic



How to Set the HDR Mode

- ⇒ Set The Sensor Mode in “HDR”
- ⇒ Set The HDR Mode in “Single Line HDR” to Output an HDR Line
- ⇒ Select the Ratio of exposure required between the low and the high level Lines.
- ⇒ Set the Camera Synchronization Mode in Full Exposure Mode Preset : The choice of the exposure of the single Line is made in Automatic by selecting the Ratio between High and Low Level Lines.

More details are given in Appendix C

The following HDR Parameters are available only if the Sensor Mode is set to “HDR” :

- **HDR Mode :**
 - “0” : Output Single Line Bottom Only.
 - “1” : Output Single Line Top Only
 - “2” : Output HDR Line
- **HDR Ratio :**
 - “0” : Ratio 1 or x2 between LSB and MSB
 - “1” : Ratio 2 or x4 between LSB and MSB
 - “2” : Ratio 4 or x8 between LSB and MSB
 - “3” : Ratio 8 or x16 between LSB and MSB

7.2.5 Test Image Pattern Selector

This selection Defines if the data comes from the normal Sensor operation and FPGA Chain or from digital patterns generated at the end of the FPGA. This is mainly useful to detect some interfacing or connection issues.

- To switch to Cmos sensor image
- Grey Horizontal Ramp (Fixed) : **See AppendixA**
- White Pattern (Uniform white image : 255 in 8Bits or 4095 in 12bits)
- Grey Pattern (Uniform middle Grey : 128 in 8bits or 2048 in 12 bits)
- Black Pattern (Uniform black : 0 in both 8 and 12 bits)
- Grey vertical Ramp (moving)

When any of the Test pattern is enabled, the whole processing chain of the FPGA is disabled.

7.3 Acquisition Control

The Acquisition Control section describes all features related to image acquisition, including the trigger and exposure control. It describes the basic model for acquisition and the typical behavior of the device.

Feature	CXP @	Size in bytes		Description
LinePeriod	0x08400	4	RW	Set line period, from from 1 (0,1µs) to 65535 (6553,5µs), step 1 (0,1µs)
LinePeriodMin	0x08404	4	RO	Get current line period min (0..65535 step 0,1µs)
AcquisitionLineRate	Xml		RO	= 1 / LinePeriod en Hertz
ExposureTime	0x08408	4	RW	Set exposure time, from 1 (0,1µs) to 65535 (6553,5µs), step 1 (0,1µs)
TriggerPreset	0x0840C	4	WO	0: Set trigger preset mode to Free run timed mode, with exposure time and line period programmable in the camera 1: Set trigger preset mode to Triggered mode with exposure time settings 2: Set trigger preset mode to Triggered mode with maximum exposure time 3: Set trigger preset mode to Triggered mode with exposure time controlled by one signal 4: Set trigger preset mode to Triggered mode with exposure time controlled by two signals 5: Set trigger preset mode to Free run mode, with max exposure time and programmable line period
ScanDirectionMode	0x0820C	4	RW	0: Set scan direction to “forward” 1: Set scan direction to “reverse” 2: Set scan direction to “Externally controlled direction via CC3 Camera Link (CC3=0 forward, CC3=1 reverse)”
ExternalLine (for Scan Direction)	0x08570	4	RW	Set the Line for the External Scan Direction information 0: Line0 1: Line1
TriggerTooSlow	0x08418	4	RW	Set/get trigger too slow value in ms From 1 (1 ms) to 5368 (5368 ms) step 1ms
Full Exposure Control Mode	0x08230	4	RW	0: 4S 2S Switching mode with all lines 1: 4S 2S Switching mode without wrong lines 2: 4S only (Only solution for “BHO” Models)

An **Acquisition** is defined as the capture of a sequence of one or many **Frame(s)**. This Acquisition mode and its command is managed by the Frame Grabber.

A **Frame** is defined as the capture of **Width** pixels x **Height** lines.

As for the Acquisition Mode, the **Frame Management** (Start, stop ...) is also manage by the Frame Grabber.

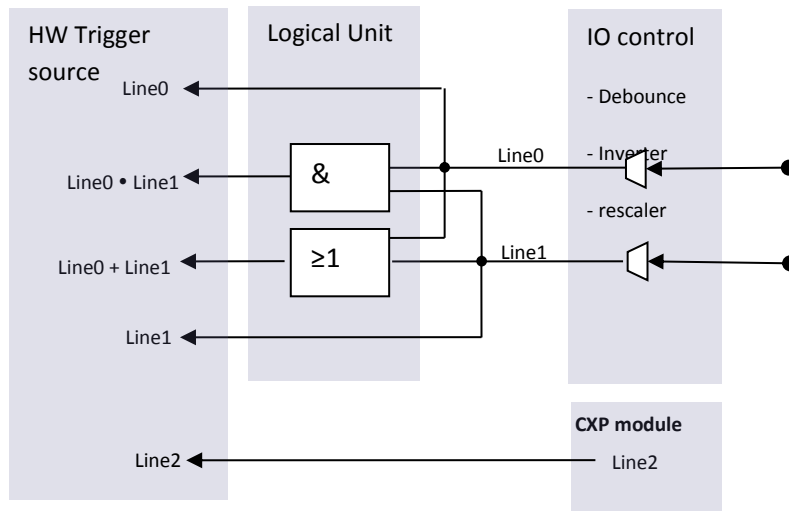
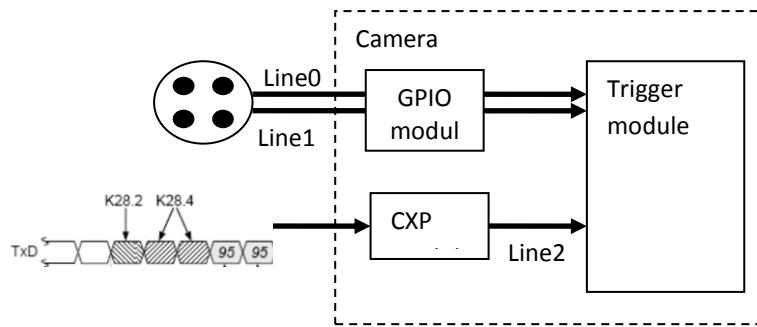
The ELIIXA+ CXP Camera is considered as a LineScan Camera (as in the CameraLink version) then only deals with the Line/Exposure Triggers.

A **Line** starts with an optional **Exposure** period and ends with the completion of the sensor read out.

The Line/Exposure Triggers can be connected :

- Either on the GPIO connector of the Camera (2x Lines Triggers : Line0/1 available if Forward/reverse command is controlled by software)
- Or by the CoaxPess Cable : Only one Trigger available (Line2).

- If the single CoaxPress Trigger is used, the Synchronization mode using 2xTriggers can't be used.

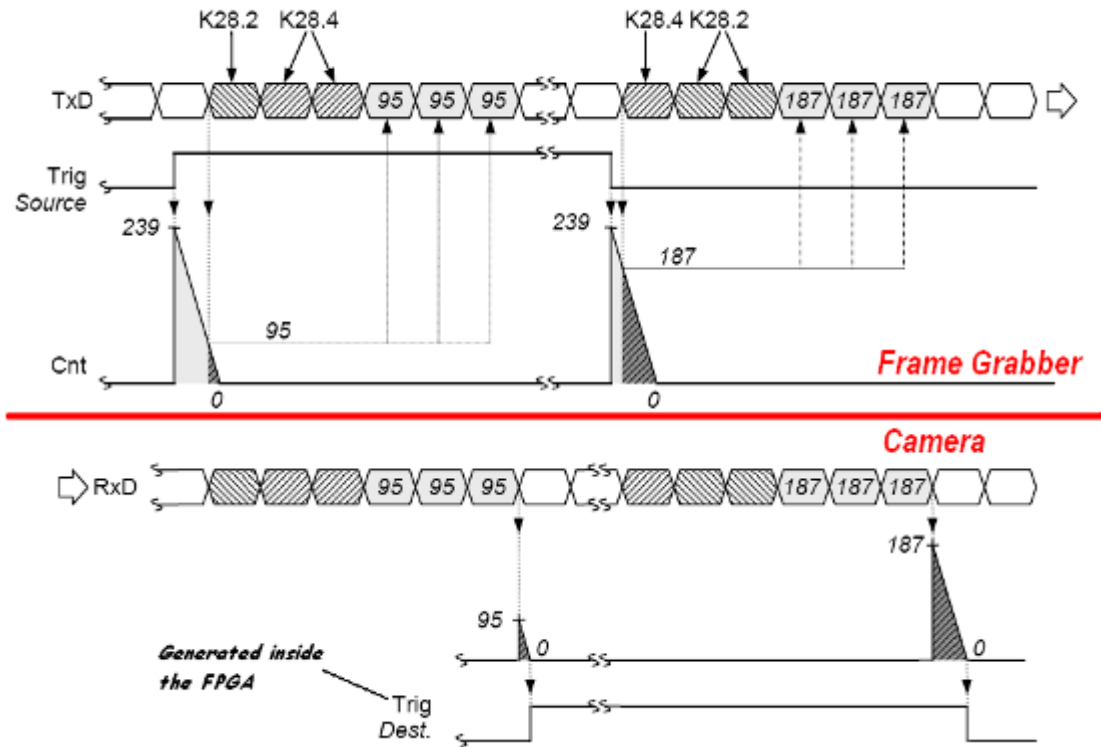


7.3.1 External Triggers on GPIO Connector

An External GPIO connector allows the camera to used 2 lines for triggering (Line0 and Line1)
 The end-user has the responsibility of the definition of the triggering system.
 The mapping describes all features available to define a trigger system

7.3.2 CXP Trigger Line

CXP specification allows the frame grabber to send triggers through the low speed link0 (@20MHz)
 The CXP specification describes the behavior of the trigger, where only the edge of the signal and a timer to limit the latency is described.
 For the camera, the CXP trigger is consider to be the “line2”. The Frame grabber itself can also manage several lines, timers, counter and finally send this single CXP trigger to the camera.



7.3.3 Scan Direction

Forward/reverse information has to be set correctly as soon as one of the following modes : “2S”, “4S” or 2SB of the sensor is set.

In these modes, the sensor/Camera need to know what is the real order of the lines for the exposure delays.

Note : The minimum delay for the Camera to take in account a change in the ScanDirection value is :

Using CC3 (I/O) signal : **120ms**.

Using serial (register) command^(*) : **180ms**

^(*)After reception of the Command on the camera side

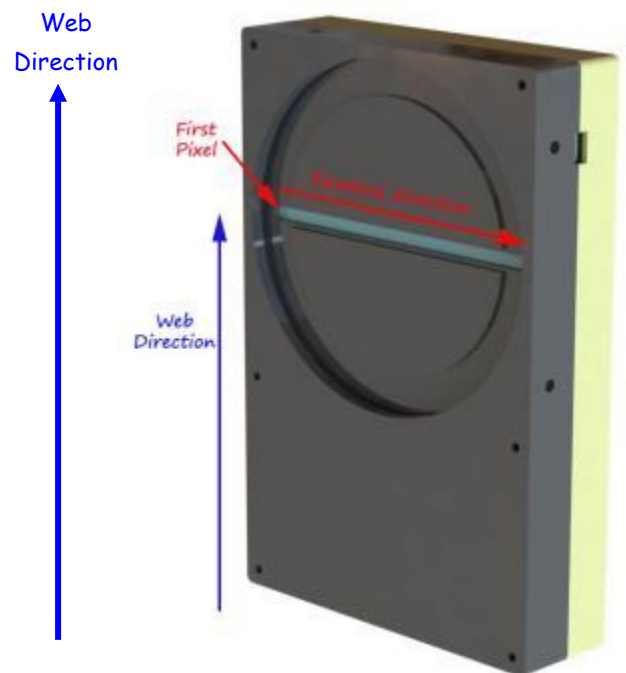
If the Camera is in **4S** Sensor mode, after changing of the scanning direction, the 5 first following triggers will be ignored in order to reinitialize the “Full Exposure Control” mode. Then the 3 following lines acquired will be more or less black because in 4S, 4 lines are required for a complete exposure.

The Forward direction is defined as detailed below :

In **2S** or **2SB** Sensor modes, no Trigger will be lost after the change of scanning direction but the first line acquired will be more or less black as in 2S, 2 lines are required for a complete exposure.

In **1S** or **1SB** modes, nothing is lost and all lines received after the delay are correct.

This positioning takes also in account that the mode “Reverse X” is “Off” (Normal readout direction)



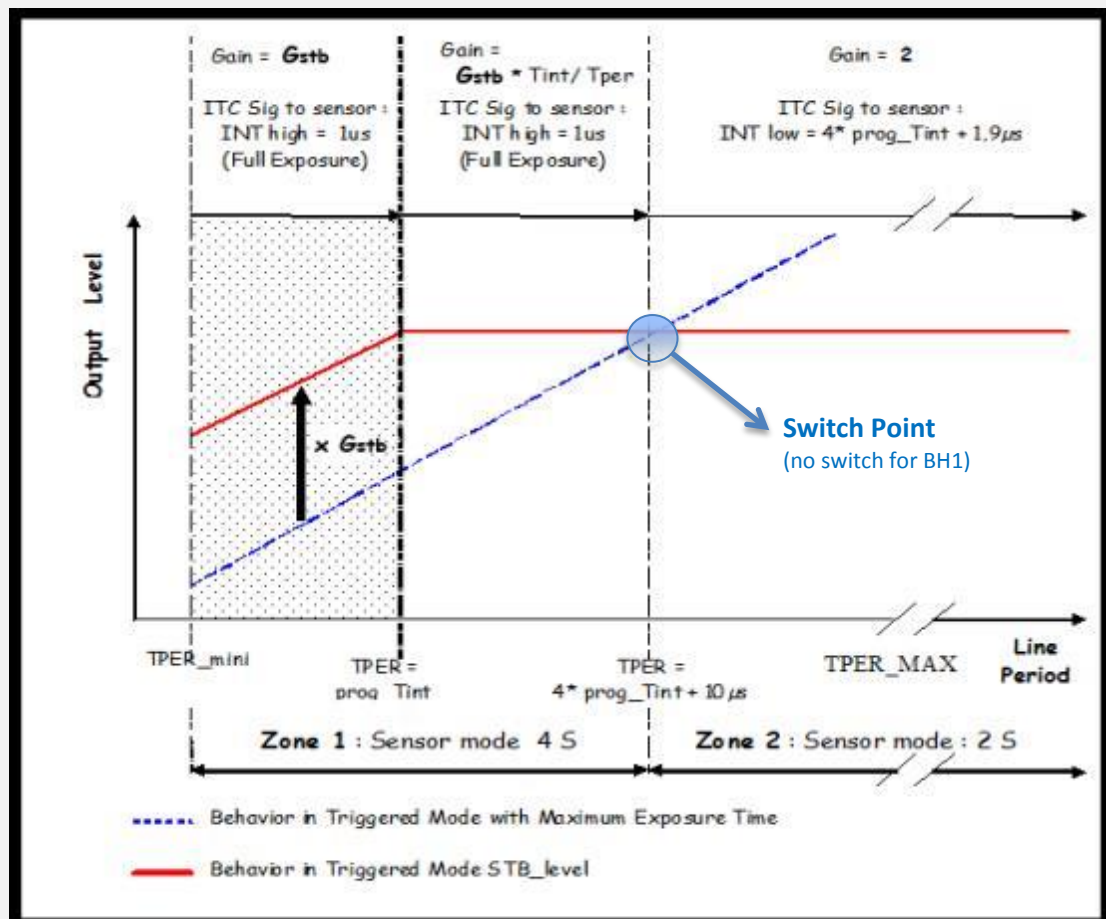
7.3.4 Full Exposure Control Mode



The Full Exposure Control

In 4S Sensor Mode, the Sensor is working as a double TDI (Time Integration Delay) : The two Top Pixels and the two bottom Pixels are working together in TDI with a delay between their exposure and outputting by the same Memory node and ADC. The summation of the pixels is done in the “charge domain” before the Digital Conversion.

In TDI, control of the exposure is not possible: Only the full Exposure during the Line Period is possible. In order to allow the User to control the exposure in this 4S Sensor mode (Synchronization Modes 1 and 3, described in the Acquisition control chapter), The ELIIXA+ Camera implement a “Full Exposure Control Mode” :



When the User selects a synchronization mode which requires the control of the exposure, the camera enters a specific mode:

The Line Period (measured) is **Tper**, its minimum value is **TPer_{mini}** ($10\mu s$ on this camera) and the exposure time set by the User is **Prog_Tint**.

If Tper < Prog_Tint

Not relevant. **Prog_Tint** has to be smaller than **Tper**.

The sensor is in full exposure and the gain applied on the output is **fixed** by the User = G_{stb} (max. x4)

If $Tper < 4 \times \text{Max}(TPer_{min}, Prog_Tint) + 10\mu s$

The Sensor works in Full Exposure during the whole Line Period (LP) and the gain applied on the output is variable (max x 4), set by User = G_{stb}

The Output is multiplied by the following Gain = $G_{stb} \times Prog_Tint / Tper$

If $Tper \geq 4 \times \text{Max}(TPer_{min}, Prog_Tint) + 10\mu s$

The Sensor Switches in a specific 2S mode (equivalent) : **Not possible for "BH0" models**

The exposure is now controlled as the sensor doesn't work in "TDI" mode.

The Exposure applied is = $4 \times Prog_Tint + 1.9\mu s$

A fixed Gain of **x2** is applied on the output to ensure the continuity with the output before the switch

During the 4S => 2S transition and the 2S => 4S transition (passing at the switch point) two "bad" lines appear (either too dark or too bright). You can remove these lines by using the following parameter:

4S Only : The sensor doesn't switch in 2S. The result is that , maybe after a short saturation, the level decreases as the Line Period increases. This mode is the best one if the Line period varies but doesn't increase that much after the switch point ($4 \times \text{Max}(TPer_{min}, Prog_Tint) + 10\mu s$)

This is the only possible mode for the BH1 Models

"Without all Lines" : The Switch 4s \leftrightarrow 2S is made in the conditions described above. All the lines are sent, even the double dark or double white at the transition (depending on the direction of the transition).

"Without Incorrect Lines" : The Switch 4s \leftrightarrow 2S is made in the conditions described above. The double dark or double white lines at the transition (depending on the direction of the transition) are removed (not sent) : Two lines triggered will miss in the LVAL signal.

Gain for the "Full Exposure Control Mode" (set in Gain & Offset Section)

G_{stb} : The User Can set this Gain with a value up to x4 (Gain Section). The value recommended is the one which allows to cover the variation of the line period : 10% of variation requires a Gain at least of x1.2 (+/- 10%).

By default this value is set at x4.



Trigger too Slow

By default, the trigger is considered too slow after 1000ms of missing Incoming Trigger.

This limit can be tuned now by the User. This tuning is particularly important when the camera is in **4S** with the **Exposure control active** and the Control Exposure mode set in **"4S Only"** : In this mode the incoming Line Period is delayed from one line to be reproduced in the camera after an exact measurement of the Line Period. If the trigger stops for a period of time below the limit, this will be considered as a "long time Line" and not a stop : Then the next line will be delayed from the same value with the risk to lose new incoming triggers.

The Trigger too Slow limit has to be set at a value which is considered in the Application as the minimum value for a real stop in the incoming trigger.

7.3.5 GenICam Triggers

Feature Name	CXP @	Size bytes	R/W	Bit field	Description
ExposureMode	0x08414	4	RW	[31-30]	Operation mode for the exposure control: 0: Off 1: Timed 2: TriggerWidth 3: TriggerControlled
TriggerSelector	-	-	RW	-	Select the trigger to control : , ExposureStart, ExposureStop, ExposureActive
TriggerSelector = ExposureActive					
TriggerMode	0x08420	4	RW	[31]	Specifies the operation mode of the trigger for the acquisition : 0: Off 1: On
TriggerSource			RW	[30-26]	Specifies the source for the trigger : 0: Software 1: Line0 2: Line1 3: Line2 4: TimerStart1 5: TimerStart2 6: TimerEnd1 7: TimerEnd2 8: CounterStart1 9: CounterStart2 10: CounterEnd1 11: CounterEnd2 17: Line0 OR line1 18: Line0 AND Line1 19: RescalerLine
TriggerActivation			RW	[25-23]	Specifies the activation mode of the trigger : 0: RisingEdge 1: FallingEdge 2: AnyEdge, 3: LevelHigh 4: LevelLow
Reserved			-	[22-21]	Set to 0
TriggerDelayAbs			RW	[20-16]	Specifies the absolute delay in μ s to apply after the trigger reception before effectively activating it (0,31/30MHz,step 1/30MHz μ s)
Reserved			-	[15-0]	Set to 0
TriggerSoftware			0x08424	4	RW
TriggerSelector = ExposureEnd					
TriggerMode, ...	0x08430	4	RW		Same as above
TriggerSoftware	0x08434	4	RW		Same as above
TriggerSelector = ExposureStart					
TriggerMode, ...	0x08440	4	RW		Same as above
TriggerSoftware	0x08444	4	RW		

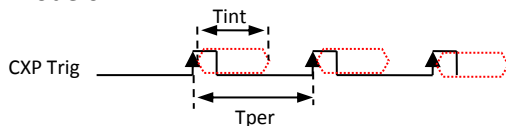
7.3.6 Trigger Presets

Several triggers are pre-defined to help the user to define its trigger configuration.
 For external trigger, 5 modes are available (Same than in the Camera Link version) :

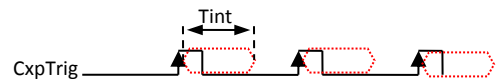
	Exposure Mode	Acquisition Mode	TriggerSelector					
			ExposureActive		ExposureStart		ExposureStop	
Mode 0	Timed	Continuous	TriggerMode	Off	TriggerMode	Off	TriggerMode	Off
			TriggerSource	NA	TriggerSource	NA	TriggerSource	NA
			TriggerActivation	NA	TriggerActivation	NA	TriggerActivation	NA
Mode 1	Timed	Continuous	TriggerMode	Off	TriggerMode	On	TriggerMode	Off
			TriggerSource	NA	TriggerSource	Line0	TriggerSource	NA
			TriggerActivation	NA	TriggerActivation	RisingEdge	TriggerActivation	NA
Mode 2	Off	Continuous	TriggerMode	Off	TriggerMode	On	TriggerMode	Off
			TriggerSource	NA	TriggerSource	Line0	TriggerSource	NA
			TriggerActivation	NA	TriggerActivation	RisingEdge	TriggerActivation	NA
Mode 3	TriggerWidth	Continuous	TriggerMode	On	TriggerMode	Off	TriggerMode	Off
			TriggerSource	Line0	TriggerSource	NA	TriggerSource	NA
			TriggerActivation	LevelLow	TriggerActivation	NA	TriggerActivation	NA
Mode 4	TriggerControlled	Continuous	TriggerMode	Off	TriggerMode	On	TriggerMode	On
			TriggerSource	NA	TriggerSource	Line0	TriggerSource	Line1
			TriggerActivation	NA	TriggerActivation	RisingEdge	TriggerActivation	RisingEdge
Mode 5	Off	Continuous	TriggerMode	Off	TriggerMode	Off	TriggerMode	Off
			TriggerSource	NA	TriggerSource	NA	TriggerSource	NA
			TriggerActivation	NA	TriggerActivation	NA	TriggerActivation	NA

For CXP triggers, only one line is available where only the rising and falling edge is defined.

■ Mode 0 :



Mode 1 :



■ Mode 2 :



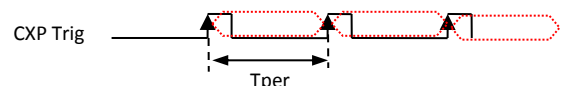
Mode 3 :



■ Mode 4 :

Not available because only 1 Trigger CXP

Mode 5 :

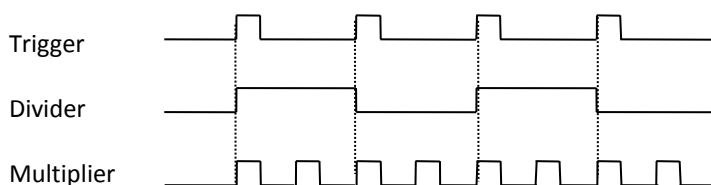


The Timing diagrams associated to each Synchronization mode and the Timing values associated are detailed in the APPENDIX B of this document.

7.3.7 Rescaler

Feature Name	CXP @	Size bytes	R/W	Bit field	Description
TriggerRescalerSource	0x08540	4	RW	[31-30]	RescalerSize (see 7.3.7) Bit0: 0: line0 selected for rescaler 1: line1 selected for rescaler Bit1: Bypass Rescaler
TriggerRescalerMultiplier			RW	[29-18]	mult factor for rescaler function Rescaler will create "mult" pulse between input trig
TriggerRescalerDivider			RW	[17-6]	div factor for rescaler function Rescaler will take 1 pulse each "div" pulse
TriggerRescalerGranularity			RW	[5-4]	0: 1 *20 = 20 ns 1: 4 *20 = 80 ns 2: 16 *20 = 320 ns 3: 256 *20 = 5120 ns
TriggerRescalerAverage			RW	[3-1]	Number of previous Triggers taken for the averaging/filtering : 0 : 1 (not activated) 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128
TriggerRescalerCountInt	0x08544		RO	[31-16]	count_int counter of rescaler bloc count between 2 input trig
TriggerRescalerCountIntOverflow			RO	[15]	count_int Overflow

The camera has two registers per line which can define a rescaler: a multiplier and a divider. With these two registers, the end-user can change the frequency of the line.



The generated line has always a 50% duty cycle. With the combination of a multiplier and divider, the system can generate any frequency

The system must sample the input signal to compute its frequency.

Two parameters define the sample settings:

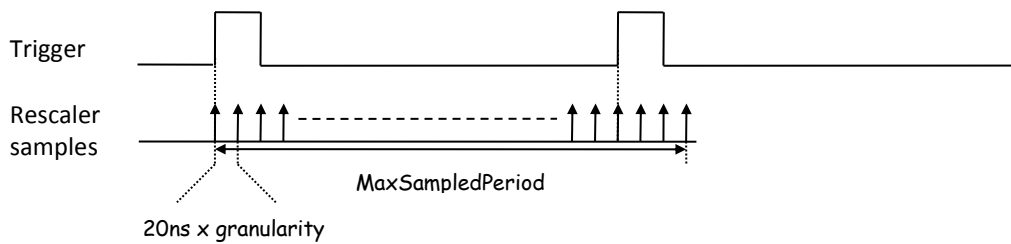
- RescalerSize
- Granularity

The Rescaler Size defines the maximum number of samples. Two values are possible: 12bit (4096 samples) or 16bit (65536 samples).

The Granularity allows the rescaler to generate the sample periodicity. Four values are possible: 1, 4, 16 or 256 system clock cycles.

The system clock period is 20ns. So the time between samples is (Granularity x 20ns)

With these two parameters, the user must determine the best sample range. It is the user responsibility to configure the rescaler.



The MaxSampledPeriod must be as close as possible to the trigger period while still being longer

$$\text{MaxSampledPeriod} = 20\text{ns} \times \text{granularity} \times 2^{\text{rescalerSize}}$$

The array below gives the MaxSampledPeriod in millisecond :

granularity	Precision (ns)	Max Sample Period (ms)
1	20	1.31
4	80	5.24
16	320	20.97
256	5120	335.54

The trigger frequency is calculated at each Trigger pulse.

7.4 Digital I/O Control

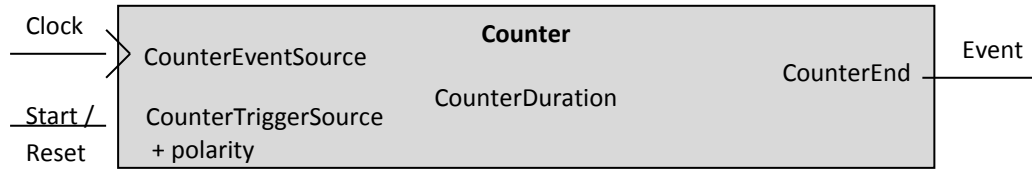
Feature Name	CXP @	Size bytes	R/W	Bit field	Description
LineStatusAll	0x08460	4	RO		Return the current status of all lines (bit0 for Line0, bit1 for Line1, bit2 for Line2)
LineSelector	Not a register		-		Select which physical line of the external device connector to configure {Line0, Line1, Line2 }
LineSelector = Line0					
LineMode	0x08470	4	RW	[31]	Define the physical line as input {Input} 0: Input 1: Output
LineInverter			RW	[30]	Define the signal inversion: 0: False 1: True
LineDebounceFilter			RW	[29]	Activate debounce filter {True, False}
LineStatus			RO	[28]	Return the current status of the selected : 0: False 1: True
LineFormat			RW	[25-24]	Select the electrical format of the selected line (line0 or line1): 0: TTL 1: LVDS 2: RS422
LineSelector = Line1					
LineMode	0x08480	4	RW		Same as above
LineInverter			RW		Same as above
LineDebounceFilter			RW		Same as above
LineStatus			RW		Same as above
LineFormat			RW		Same as above
LineSelector = Line2					
LineMode	0x08490	4	RW		Same as above

Feature Name	CXP @	Size bytes	R/W	Bit field	Description
LineInverter			RW		Same as above
LineDebounceFilter			RW		Same as above
LineStatus			RW		Same as above
LineFormat			RW		Same as above

7.5 Counters & Timers Control

7.5.1 Counters

Here is a following description of the counters :

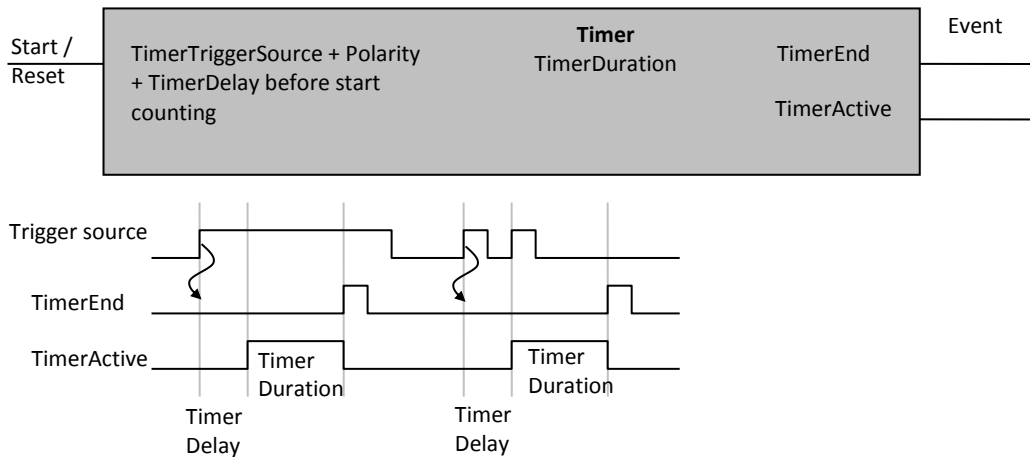


Feature Name	CXP @	Size bytes	R/W	Bit field	Description
CounterSelector	Not a register	-	-	-	Select which counter to configure {Counter1, Counter2}
CounterSelector = Counter1					
CounterTriggerSource	0x084B0	4	RW	[31-27]	Select the signal that start (reset) the counter: 0: Off 9: ExposureStart 10: ExposureEnd 11: Line0 12: Line1 13: Line2 16: Counter1End 17: Counter2End 18: Timer1End 19: Timer2End
CounterTriggerActivation			RW	[26-24]	Select the type of activation for the trigger to start (reset) the counter : 0: RisingEdge 1: FallingEdge 2: AnyEdge, 3: LevelHigh 4: LevelLow
CounterEventSource			RW	[23-19]	Select the event that will be the source to increment the counter : 0: Off 9: ExposureStart 10: ExposureEnd 11: Line0 12: Line1 13: Line2 16: Counter1End 17: Counter2End 18: Timer1End 19: Timer2End 20: TimeStampTick 21: MissedTrigger
CounterEventActivation			RW	[18-16]	Select the type of activation for the event that increment the counter : 0: RisingEdge 1: FallingEdge 2: AnyEdge,

Feature Name	CXP @	Size bytes	R/W	Bit field	Description
					3: LevelHigh 4: LevelLow
CounterStatus			RO	[15-13]	Get counter status : 0: CounterIdle 1: CounterTriggerWait 2: CounterActive, 3: CounterCompleted 4: CounterOverflow
CounterDuration	0x084B4	4	RW	[31-0]	Set the counter duration (or number of events) before CounterEnd event is generated
CounterReset	0x084B8	4	RW		Reset the selected counter
CounterValue	0x084BC	4	RO	[31-0]	Read the current value of the selected counter
CounterValueAtReset	0x084C0	4	RO	[31-0]	Read the value of the selected counter, when the counter was reset by a trigger or by an explicit CounterReset.
CounterResetSource	0x084C4	4	RW	[31-27]	Select the signal that reset the counter: 0: Off 1: Software 2: Line0, 3: Line1 4: Line2
CounterResetActivation			RW	[26-24]	Select the type of activation for the counter reset source : 0: RisingEdge 1: FallingEdge 2: AnyEdge, 3: LevelHigh 4: LevelLow
CounterSelector = Counter2					
CounterTriggerSource	0x084D0	4	RW		Same as above
CounterTriggerActivation			RW		Same as above
CounterEventSource			RW		Same as above
CounterEventActivation			RW		Same as above
CounterStatus			RO		Same as above
CounterDuration	0x084D4	4	RW		Same as above
CounterReset	0x084D8	4	RW		Same as above
CounterValue	0x084DC	4	RO		Same as above
CounterValueAtReset	0x084E0	4	RO		Same as above
CounterResetSource	0x084E4	4	RW		Same as above
CounterResetActivation			RW		Same as above

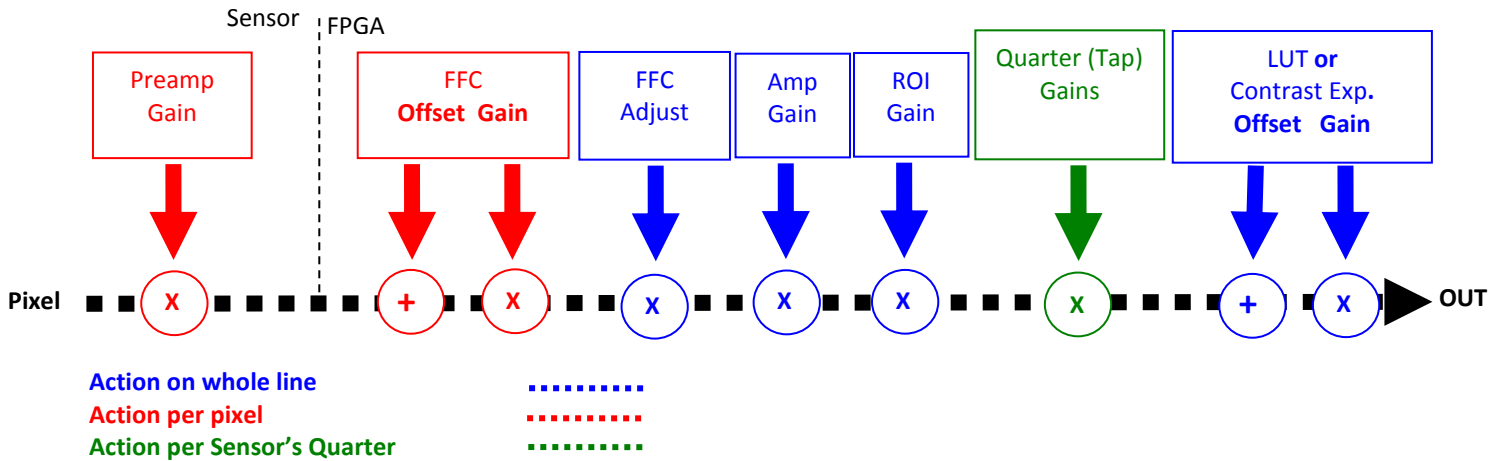
7.5.2 Timers

Here is a following description of the Timers :



Feature Name	CXP @	Size	R/W	Bit field	Description
TimerSelector	Not a register	-	-	-	Select which timer to configure {Timer1, Timer2}
TimerSelector = Timer1					
TimerTriggerSource	0x08500	4	RW	[31-27]	Select which internal signal will trigger the timer: 0: Off 9: ExposureStart 10: ExposureEnd 11: Line0 12: Line1 13: Line2 16: Counter1End 17: Counter2End 18: Timer1End 19: Timer2End
TimerTriggerActivation			RW	[26-24]	Select the type of signal that will trig the timer: 0: RisingEdge 1: FallingEdge 2: AnyEdge, 3: LevelHigh 4: LevelLow
TimerDelay			RW	[23-19]	Set the delay in μ s from the TimerTrigger to the actual Timer pulse output (0,31/30MHz, step 1/30MHz)
TimerStatus			RO	[18-17]	Get counter status 0: TimerIdle 1: TimerTriggerWait 2: TimerActive, 3: TimerCompleted
TimerDuration	0x08504	4	RW	[31-0]	Set the length of the ouput pulse in μ s (0,6553.5, step 0.1)
TimerValue	0x08508	4	RO	[31-0]	Return the actual value of the selected timer (0,65535/30MHz, step 1/30MHz)
TimerSelector = Timer2					
TimerTriggerSource	0x08510	4	RW		Same as above
TimerTriggerActivation			RW		Same as above
TimerDelay			RW		Same as above
TimerStatus			RO		Same as above
TimerDuration	0x08514	4	RW		Same as above
TimerValue	0x08518	4	RO		Same as above

7.6 Gain and Offset

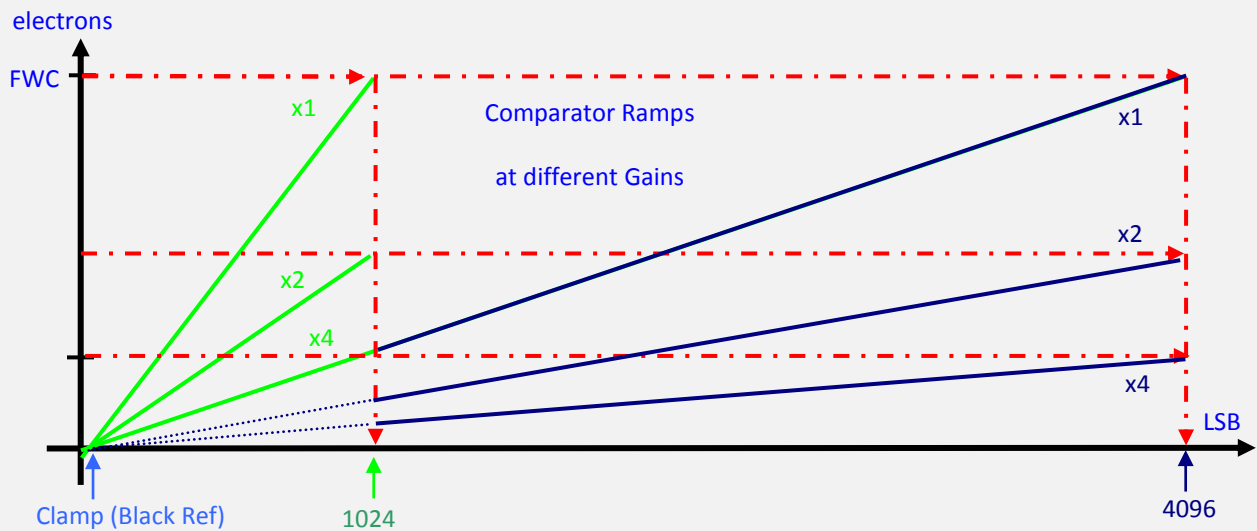


Analog Gain in the ADC

The only analog Gain available in the ELIIXA+ is located at the sensor level, in the ADC converter.

This "Preamp Gain" is in fact a variation of the ramp of the comparator of the ADC.

Then 3 Values are available : x1, x2 and x4. A gain x1 in a 12 bits conversion is equivalent to x4 in 10 bits.



The Contrast Expansion (both Digital Gain & Offset) will be automatically disabled if the LUT is enabled.

Feature	CXP @	Size in bytes	R/W	Description
GainAbs GainSelector= AnalogAll	0x08600	4	RW	Set pre amplifier gain to: 0: (-12dB) 1: (-6dB) 2: (0dB) (analog gain) Change balances and compensation
GainAbs GainSelector= gainAll	0x08604	4	RW	Set gain from 0dB(0) to +8 dB (6193)
Gain Abs GainSelector=DigitalAll	0x08608	4	RW	Set contrast expansion digital gain from 0 (0 dB) to 255 (+14 dB), step 1 (TBD dB)
BlackLevelRaw BlackLevelSelector=All	0x0860C	4	RW	Set common black from -4096 to 4095, step 1
GainAbs GainSelector=QuarterGain<j>	0x08610 to 0x0861C	4 * 4	RW	tap<j> digital gain from -128 to 127 by step 1 (0.0021dB). Dynamically updated on AnalogAll gain changes
Quarter Gain enable	0x08620	4	RW	Enable the QuarterGain<j>
ROIgainR	0x08624	4	WO	Set the value of the gain for the define ROI Value from 0 to 1024 (0 to 6dB) Not readable (one shot function)
ROIgainR	0x08628	4	WO	Defines the ROI for ROI Gain an applies it : XXXX: start ROI (from 0 to 3FFF in hexa) YYYY: Stop ROI (from 0 to 3FFF in hexa) Parameter : "XXXXYYYY" Not readable (one shot function)
Full Exposure Gain	0x0A100	4	RW	Set Adjust Full Exposure Gain 0 to 49151 : $(1 + \langle val \rangle / 16384) = x1$ to $x4$

The Full Exposure Gain is part of the "Amp Gain" Block detailed above.



ROI Gain : How does it works ?

The ROI Gain feature comes in addition with the FFC (it's applied and calculated after).
 The maximum complementary Gain is $\times 2$.

It can be applied in 2 commands :

- > First set the ROI Gain value : command address is : 0x8624
- > Second, set the ROI (Region of Interest) : Command address is 0x8628

This second command applies the Gain on the ROI in memory and this is immediately activated.

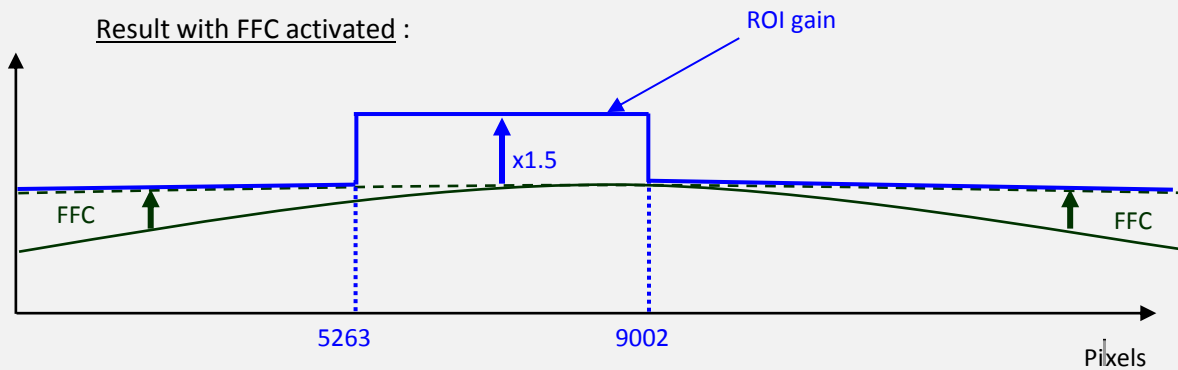
The ROI Gain is a "online" function that can be overlapped but can't be saved.

Here is an example to apply a complementary gain of $\times 1,5$ between the pixels #5263 and #9002 (pixels are included). The two commands are :

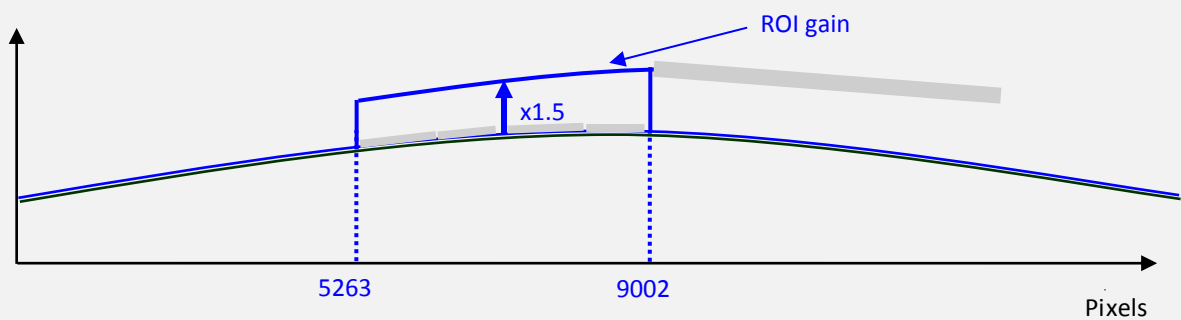
"w 0x8624 512"

"w 0x8628 0x148F232A"

Result with FFC activated :



Result with FFC not activated :



7.7 Flat Field Correction

Feature	CXP @	Size in bytes	R/W	Description
FFCEnable	0x08800	4	RW	0 : Disable Flat Field Correction ("False") - In user/integrator mode : the factory FFC bank is written into the FPGA and the FFC stays enabled 1 : Enable Flat Field Correction ("True")
FPNReset	0x08804	4	WO	0 : Reset FPN coefficients
PRNUReset	0x08808	4	WO	0 : Reset PRNU coefficients
FPNValueAll	0x10000	32K	RW	Memory containing FPN Format: 9bits signed coded on 16bits each Value S9.1 => -256..+255.5 step ½ Size=CCDSize*2
FPNValueSize	Xml	2	RO	Integer providing FPN value size in byte
PRNUValueAll	0x20000	32K	RW	Memory containing PRNU Format: 12bits unsigned coded on 16bits each value : U.2.12 => 0-4095 : (1+Value/1024) => x1..x4.999 by step of 1/1024 Size=CCDSize*2
PRNUValueSize	Xml	2	RO	Integer providing PRNU value size in byte
FFCCalibrationCtrl	0x0880C	4	RW	FFC calibration - In Read Mode: 0 = finished 1 = running - In Write Mode: 0 = Abort PRNU calibration by setting it to "Off" (no effect if already stopped) 1 = Launch PRNU calibration by setting it to "Once" (no effect if already launched)
FPNCalibrationCtrl	0x08810	4	RW	FPN calibration - In Read Mode: 0 = finished 1 = running - In Write Mode: 0 = Abort FPN calibration by setting it to "Off" (no effect if already stopped) 1 = Launch FPN calibration by setting it to "Once" (no effect if already launched)
FFCAdjust	0x08814	4	RW	0 : Disable ffc adjust 1 : Enable ffc adjust
FFCAutoTargetLevel	0x08818	4	RW	Set FFC target adjust level, from 0 to 4095, step 1
FFCGainAdjust	0x0881C	4	RW	FFC Gain Adjust
LowFrequencyFilterWidth	0x8820	4	RW	Configure windows (width) around the pixel (+/- val) 0 : filter is disable 1-255 : nb pixels around the pixel to filter



How is performed the Flat Field Correction ?

What is the Flat Field correction (FFC) ?

The Flat Field Correction is a digital correction on each pixel which allows :

- To correct the Pixel PRNU (Pixel Response Non Uniformity) and DSNU (Dark Signal Non Uniformity)
- To Correct the shading due to the lens
- To correct the Light source non uniformity



How is calculated / Applied the FFC ?

The FFC is a digital correction on the pixel level for both Gain and Offset.

Each Pixel is corrected with :

An Offset on 10 bits (Signed Int S9.1). They cover a dynamic of ± 256 LSB in 12bits with a resolution of 1/2 LSB 12bits. Offset : the MSB is the sign, the rest of 9bits is from 0 .. 256 with precision of 1/2

A Gain on 12 bits (Unsigned Int U2.12) with a max gain value of $\times 5^{(*)}$

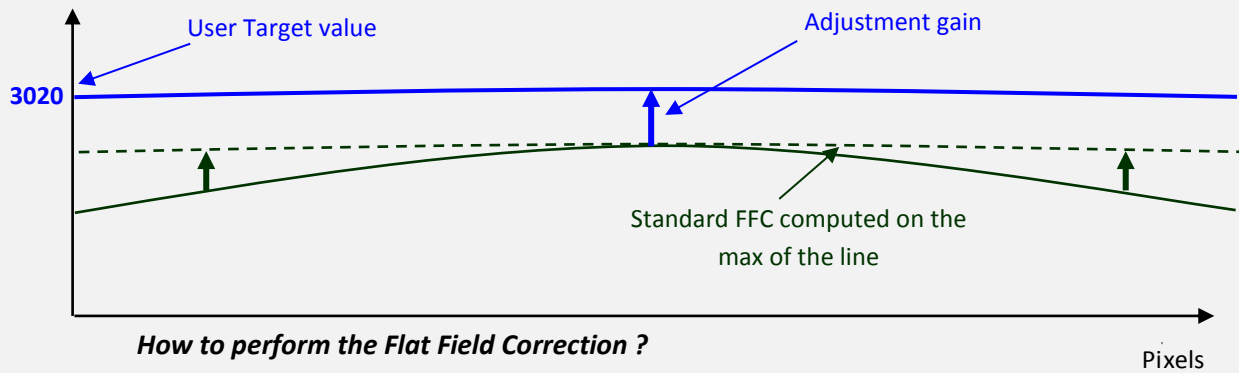
The calculation of the new pixel value is : $P' = (P + \text{Off}) \cdot (1 + \text{Gain}/1024^{(*)})$. Gain : 0 to 4095

The FFC processing can be completed with an automatic adjustment to a global target. This function is designed as “**FFC Adjust**”. This adjustment to a User target is done by an internal hidden gain which is re-calculated each time the FFC is processed while the FFC adjust function is enabled.

The FFC is always processed with the max pixel value of the line as reference. If enabled, the FFC adjust module (located at the output of the FFC module) calculates the adjustment gain to reach the target defined by the User.

When the FFC result is saved in memory, the adjust gain and target are saved in the same time in order to associate this gain value with the FFC result.

() : Before the firmware version 1.0.15B, the Gain resolution was : $1 + \text{Gain}/8192$ with a range limited at $\times 3$*



FPN/DSNU Calibration

- > Cover the lens
- > Launch the FPN Calibration : Grab and calculation is performed in few seconds

PRNU Calibration

The User must propose a white/gray uniform target to the Camera (not a fixed paper).

The Gain/Light conditions must give a non saturated image in any Line.

The Camera must be set in the final conditions of Light/ Gain and in the final position in the System.

If required, set a user target for the FFC adjust and enable it.

White uniform (moving) target. Use The FFC Low Band Filter if the Target can't move.

This will remove the defects of the target itself

- > Launch the FFC
- > Enable the FFC
- > You can save the FFC result (both FPN+PRNU in the same time) in one of the 4 x FFC User Banks.

The user target and Gain are saved with the associated FFC in the same memory.

Advices

The AVIIVA+ Cameras have 8 x FFC Banks to save 8 x different FFC calibrations. You can use this feature if your system needs some different conditions of lightning and/or Gain because of the inspection of different objects : You can perform one FFC to be associated with one condition of Gain/setting of the Camera (4 Max) and recall one of the four global settings (Camera Configuration + FFC + Line Quarters Balance) when required.



FFC Adjust : A good usage.

When there are several Cameras to set up in a system on a single line, the most difficult is to have a uniform lighting whole along the line.

If each Camera performs its own Flat field correction, relative to the max of each pixel line, the result will be a succession of Camera lines at different levels.

The FFC Adjust function allows to set the same target value for all the Cameras in the system and then to get a perfect uniform line whole along the system with a precision of 1 LSB to the Target.

The Maximum correction is x2 the highest value of the line.

The reasonable value for the User Target is not more than around 20% of the max value of the line.

7.7.1 Automatic Calibration



Some Warnings can be issued from the PRNU/FPN Calibration Process as “pixel Overflow” of “Pixel Underflow” because some pixels have been detected as too high or too low in the source image to be corrected efficiently.

The Calculation result will be proposed anyway as it's just a warning message.

The Status Register is the changed and displayed in Device Control Status section.

7.7.2 Manual Flat Field Correction

The FFC Coefficients can also be processed outside of the Camera or changed manually by accessing directly their values in the Camera : This is the “Manual” FFC.

This will allow the user to upload/download out/in the Camera the FFC coefficients in/from a binary or text file that can be processed externally.

The new-processed FFC values can be saved or restored in/from 8 x User banks.

Both Gains and Offsets in the same time but also the FFC Adjust User target and associated gain.

These functions are available in the Flat Field correction/Save & Restore FFC section

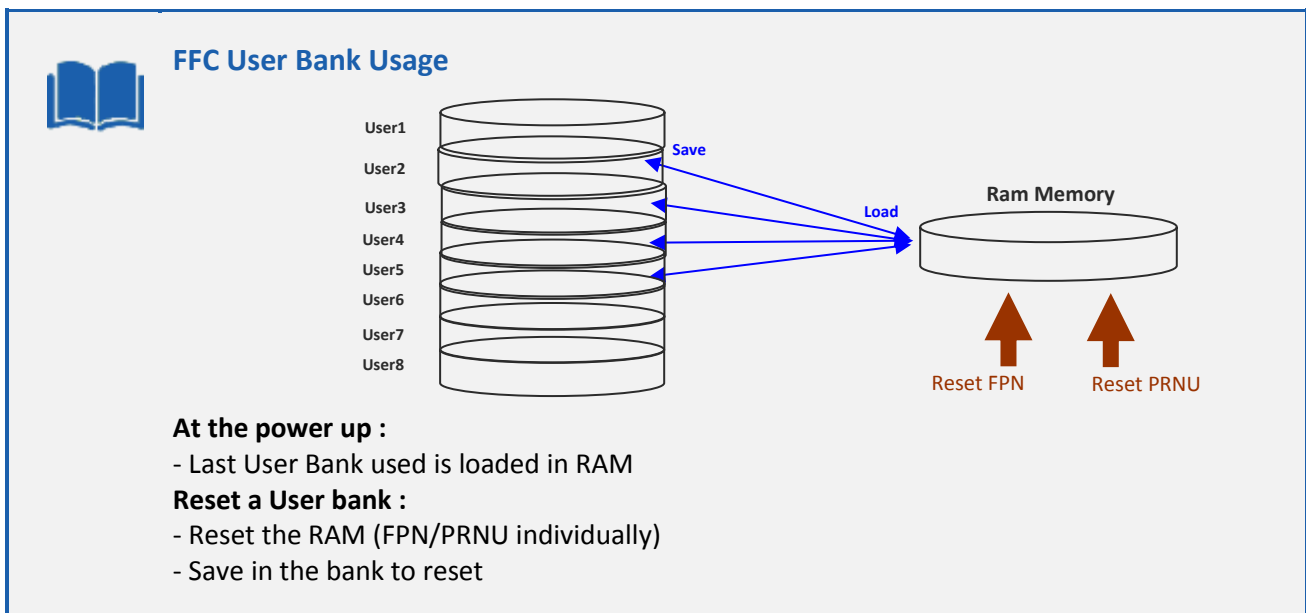


There is no software or interface provided even through GenICam to Upload/Download the FFC Table in the Camera.

GenICam just provides an access to the corresponding Memory area in the Camera for both Gains and Offsets (PRNUValueAll and FPNValueAll in the Register table above)

7.7.3 Save & Restore FFC in User Memory Banks

Feature	CXP @	Size in bytes	R/W	Description
RestoreFFCFromBank	0x08C10	4	RW	Restore current FFC (including FPN and FFCGain) from FFC bank number <val>, from 1 to 8; <val> comes from FFC SetSelector 1,2,3,4,5,6,7,8: User Banks
SaveFFCToBank	0x08C14	4	WO	Save current FFC (including FPN and FFCGain) to FFC bank number <val>, from 1 to 8; <val> comes from FFC SetSelector 1,2,3,4,5,6,7,8: User Banks
FFCSetSelector	Xml		-	FFC bank selector



7.8 Look Up Table

The User can define an upload a LUT in the Camera that can be used at the end of the processing. The LUT is defined as a correspondence between each of the 4096 gray levels (in 12 bits) with another outputted value. For example, a “negative” or “reverse” LUT is the following equivalence :

Real value	Output value
0	4095
1	4094
2	4093
...	

Then the size of each value is 12bits but the exchanges with the Application/PC are done on 16 bits : For 4096 gray levels (from 0 to 4095) the total file size for a LUT is 8Ko.

If this LUT is enables, the “Contrast Expansion” feature (digital Gain and Offset) will be disabled

Feature	CXP @	Size in bytes	R/W	Description
LUTEnable	0x08A00	4	RW	0: Disable LUT (“False”) 1: Enable LUT (“True”)
LUTValueAll	0x30000	8K	RW	Memory containing LUT on 12 bits Size=2 ¹² * 2
LUTValueSize	Xml	2	RO	Integer providing LUT value size in byte



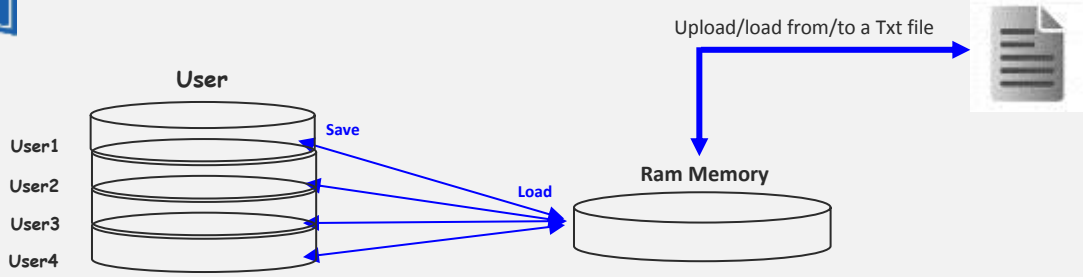
There is no software or interface provided even through GenICam to Upload/Download the Look Up Table in the Camera. GenICam just provides an access to the corresponding Memory area in the Camera (LUTValueAll in the Register table above)

7.8.1 Save & Restore LUT in User Memory Banks

Feature	CXP @	Size in bytes	R/W	Description
RestoreLUTFromBank	0x08C08	4	RW	Restore current LUT from LUT bank number <val>, from 1 to 4; <val> comes from LUTSetSelector 1,2,3,4: User Bank
SaveLUTToBank	0x08C0C	4	WO	Save current LUT to LUT bank number <val>, from 1 to 4; <val> comes from LUTSetSelector 1,2,3,4: User Bank
LUTSetSelector	Xml		-	LUT bank selector



LUT User Bank Usage



At the power up :

- Last User Bank used is loaded in RAM

7.9 Statistics and Line Profile

This function allows the User to get some statistics on a pre-defined ROI. On request, the Camera acquires and then calculates some key values as the min, the max, the average or the standard deviation in this Region of Interest.

The grab and calculation command and also the collection of the results is not performed in real time as it is done through the serial connection.

This function and the results are available in the “Line Profile Average” Section :

The Calculated values are detailed as following :

- **Pixel average Value** (*PixelROIMean*) : Average gray level value calculated on whole Region of interest
- **Pixel Standard deviation** (*PixelROIStandardDeviation*) : standard deviation of all the pixel gray level values of Region of interest
- **Pixel Min value** (*PixelROImin*) : Minimum gray level pixel value on the whole region of interest.
- **Pixel Max Value** (*PixelROIMax*) : Maximum gray level pixel value on the whole region of interest

Feature	CXP @	Size in bytes	R/W	Description
LineAverageProfile	0x09000	4	RW	Camera running privilege level - In Read Mode: 0 = finished 1 = running - In Write Mode: 0 = Abort the Line Average Profile 1 = Run the Line Average Profile
PixelAccessLineNumer	0x09004	4	RW	Set the number of line to accumulate - <val> : 1,256,512,1024
PixelValueAll	0x40000	32K	RW	Pixel Values Size=SensorWidth * 2
PixelRoiStart	0x09008	4	RW	Roi start for pixel statistic computing (0 to SensorWidth - 1-1)
PixelRoiWidth	0x0900C	4	RW	Roi width for pixel statistic computing (1 to SensorWidth)
PixelROIMean	0x09010	4	RO	Get ROI Mean (format U12.4)
PixelROIStandardDeviation	0x09014	4	RO	Get ROI Stand deviation (format U12.4)
PixelROImin	0x09018	4	RO	Get ROI Min (format U12.4)
PixelROIMax	0x0901C	4	RO	Get ROI Max (format U12.4)

7.10 Privilege Level

There are 3 privilege levels for the camera :

- Factory (0) : Reserved for the Factory
- Integrator (1) : Reserved for system integrators
- User (2) : For all Users.

The Cameras are delivered in Integrator mode. They can be locked in User mode and a specific password is required to switch back the Camera in Integrator mode. This password can be generated with a specific tool available from the hotline (hotline-cam@e2v.com)

Feature	CXP @	Size in bytes	R/W	Description
PrivilegeLevel	0x08E00	4	RW	Get camera running privilege level - In Read Mode: 0 = Privilege Factory 1 = Privilege Advanced User 2 = Privilege User - In Write Mode: 1 = Lock camera o “Advanced User” 2 = Lock camera to “User” other values = Unlock camera privilege depending on <val> (min=256; max= $2^{32}-1$)

7.11 Save & Restore Settings in User Memory Banks

The settings (or Main configuration) of the Camera can be saved in 4x different User banks and one Integrator bank. This setting includes also the FFC and LUT enable parameters

This function is available in the User Set Control section :

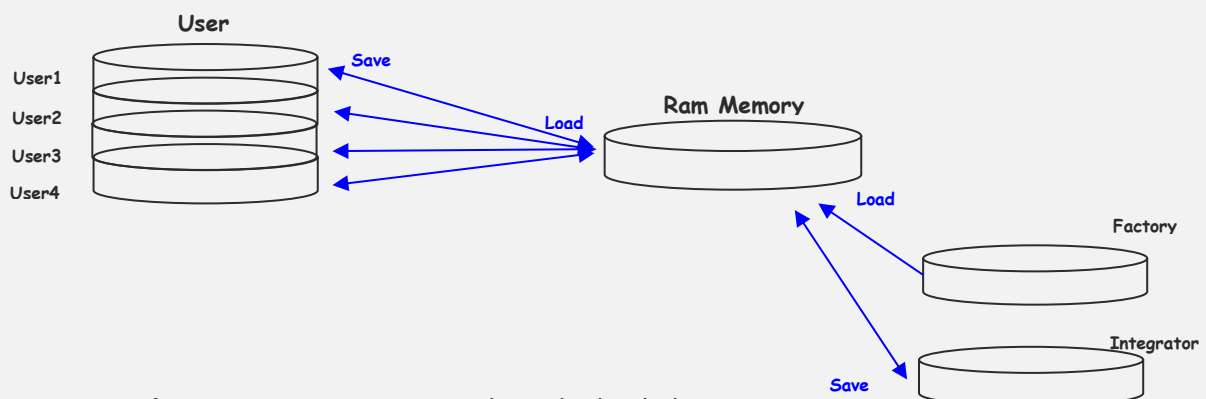
Feature	CXP @	Size in bytes	R/W	Description
UserSetLoad	0x08C00	4	RW	Restore current UserSet from UserSet bank number <val>, from 0 to 5; <val> comes from UserSetSelector 0: Factory Bank 1,2,3,4: User Bank 5: Integrator Bank
UserSetSave	0x08C04	4	WO	Save current UserSet to UserSet bank number <val>, from 1 to 5; <val> comes from UserSetSelector 1,2,3,4: User Bank 5: Integrator Bank (Not available in User Mode)
UserSetControl	Xml	-	-	User bank selector



The integrator bank (User Set5) can be written only if the Camera is set in integrator mode (Privilege level = 1). This integrator bank can be used as a « Factory default » by a system integrator.



Configuration Bank Usage



At the power up : Last User Bank used is loaded in RAM

“Integrator” Bank (5) can be locked by switching the Camera in “User” mode (cf : Privilege feature). Then it can’t be saved any more without switching back the Camera in “Integrator” Mode.

APPENDIX

Appendix A. Test Patterns

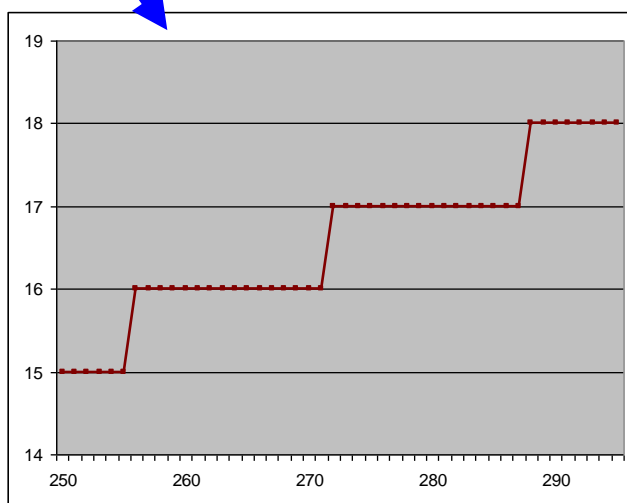
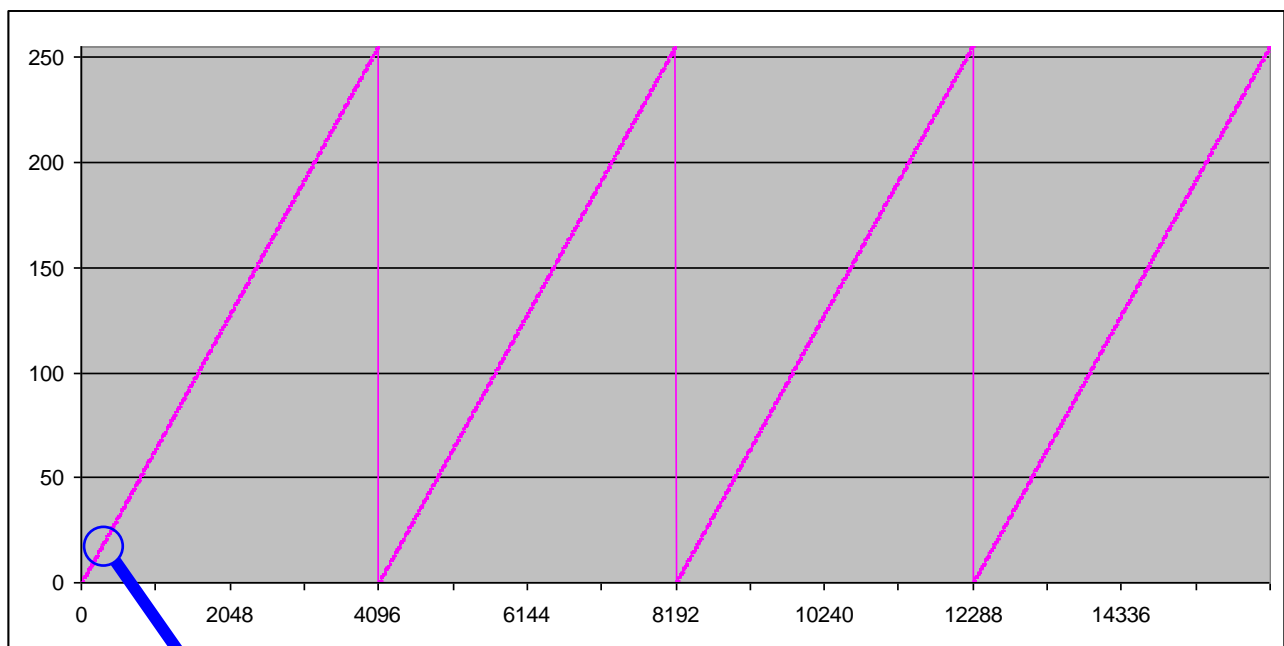
A.1 Test Pattern 1: Vertical wave

The Test pattern 1 is a vertical moving wave : each new line will increment of 1 gray level in regards with the previous one.

- In 12 bits the level reaches 4095 before switching down to 0
- In 8 bits the level reaches 255 before switching down to 0

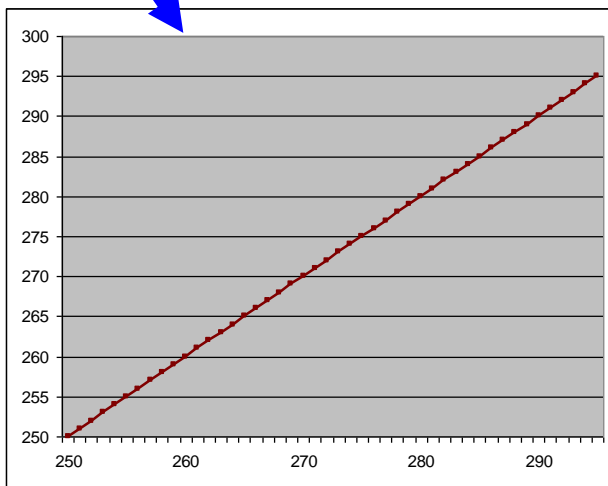
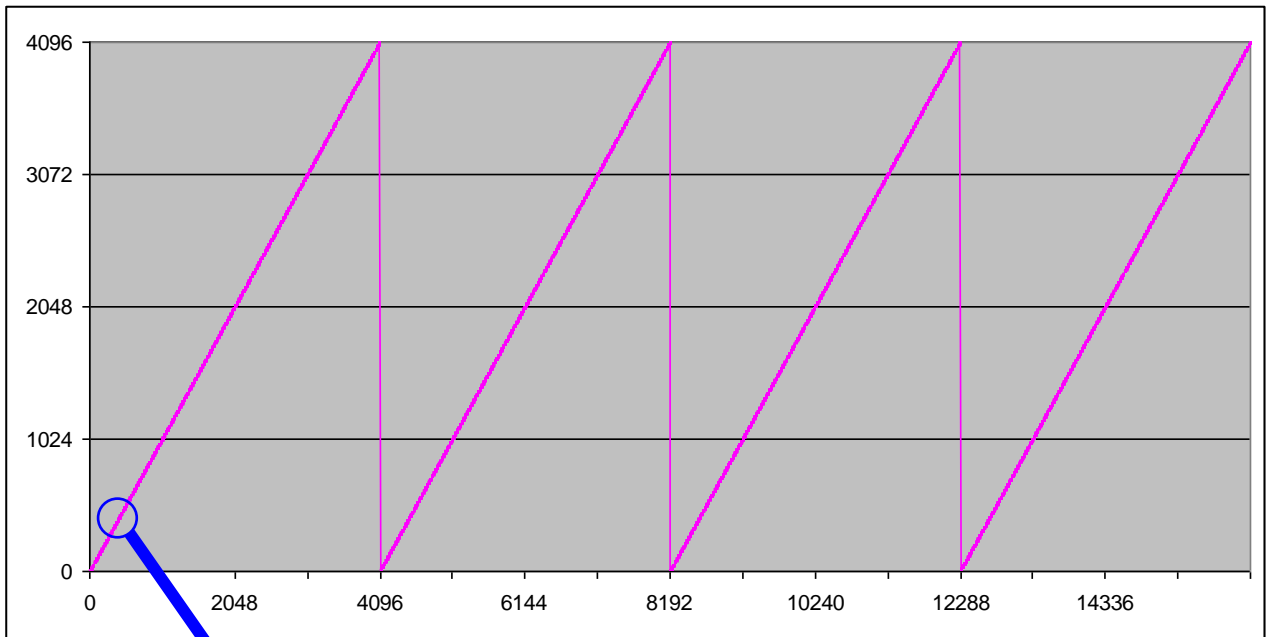
A.2 Test Pattern 2: Fixed Horizontal Ramps

A.1.2 In 8 bits (Full) format – No Binning (16384 pixels)



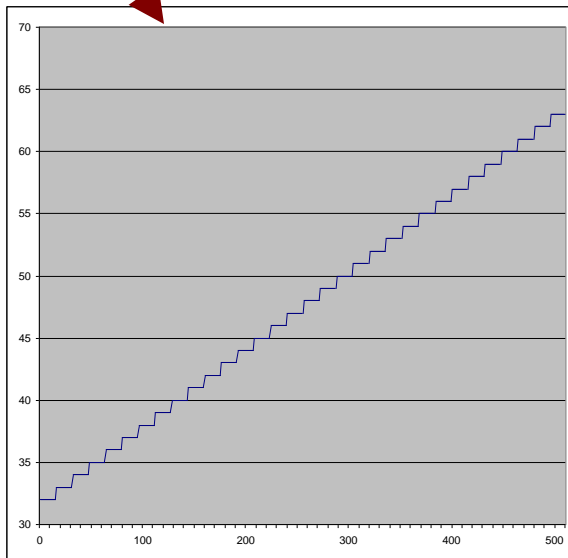
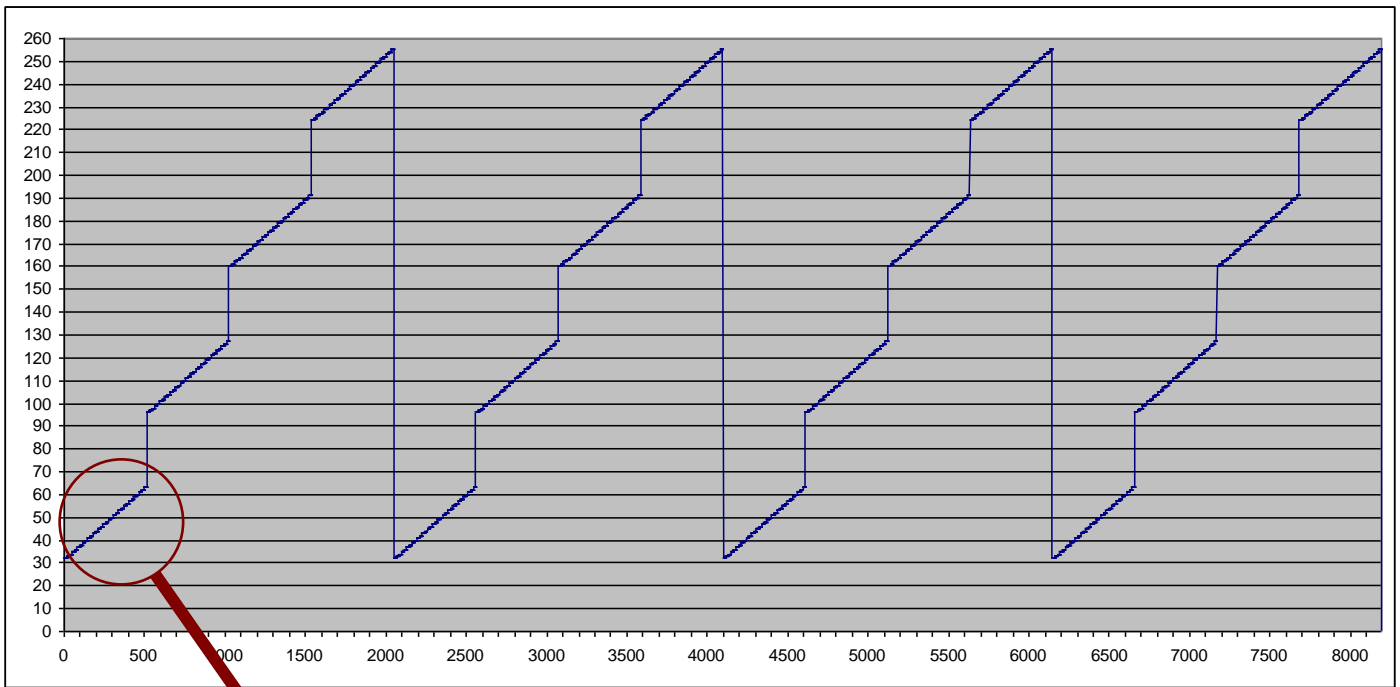
An increment of 1 LSB is made every 16 pixels
 When it reaches 255, turns back to 0 and starts again

A.2.2 In 12 bits (Medium) format – No Binning (16384 pixels)



An increment of 1 LSB is made for each pixel. When it reaches 4095, turns back to 0 and starts again

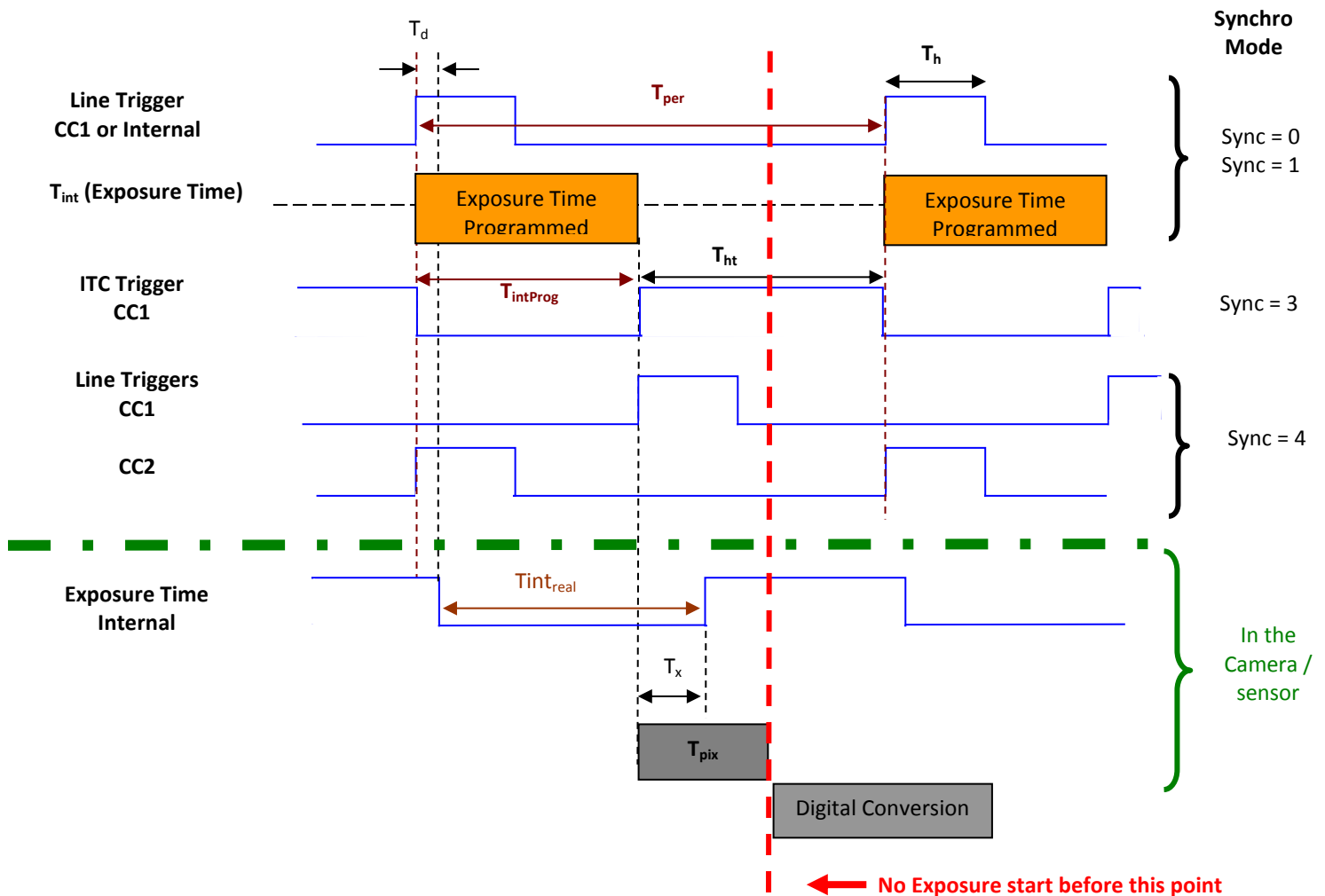
A.3.2 In 8/12 bits Full/Medium format with Binning (8192 Pixels)



Pixel 0 : 32
 Pixel 1 : 32
 ...
 Pixel 15 : 32
 Pixel 16 : 33
 Pixel 17 : 33
 ...
 Pixel 31 : 33
 Pixel 32 : 34
 ...
 Pixel 511 : 63
 Pixel 512 : 96
 Pixel 513 : 96
 ...
 Pixel 2047 : 255
 Pixel 2048 : 32
 ...

Appendix B. Timing Diagrams

B.1 Synchronization Modes with Variable Exposure Time



T_{pix} : Timing Pixel. During this uncompressible period, the pixel and its black reference are read out to the Digital converter. During the first half of this timing pixel (read out of the black reference), we can consider that the exposure is still active.

Digital Conversion : During the conversion, the analog Gain is applied by the gradient of the counting ramp (see next chapter : Gain & Offset). The conversion time depends on the pixel format :

- 8 or 10 bits : **6 μ s**
- 12 bits : **18 μ s**

This conversion is done in masked time, eventually during the next exposure period.

T_d : Delay between the Start exposure required and the real start of the exposure.

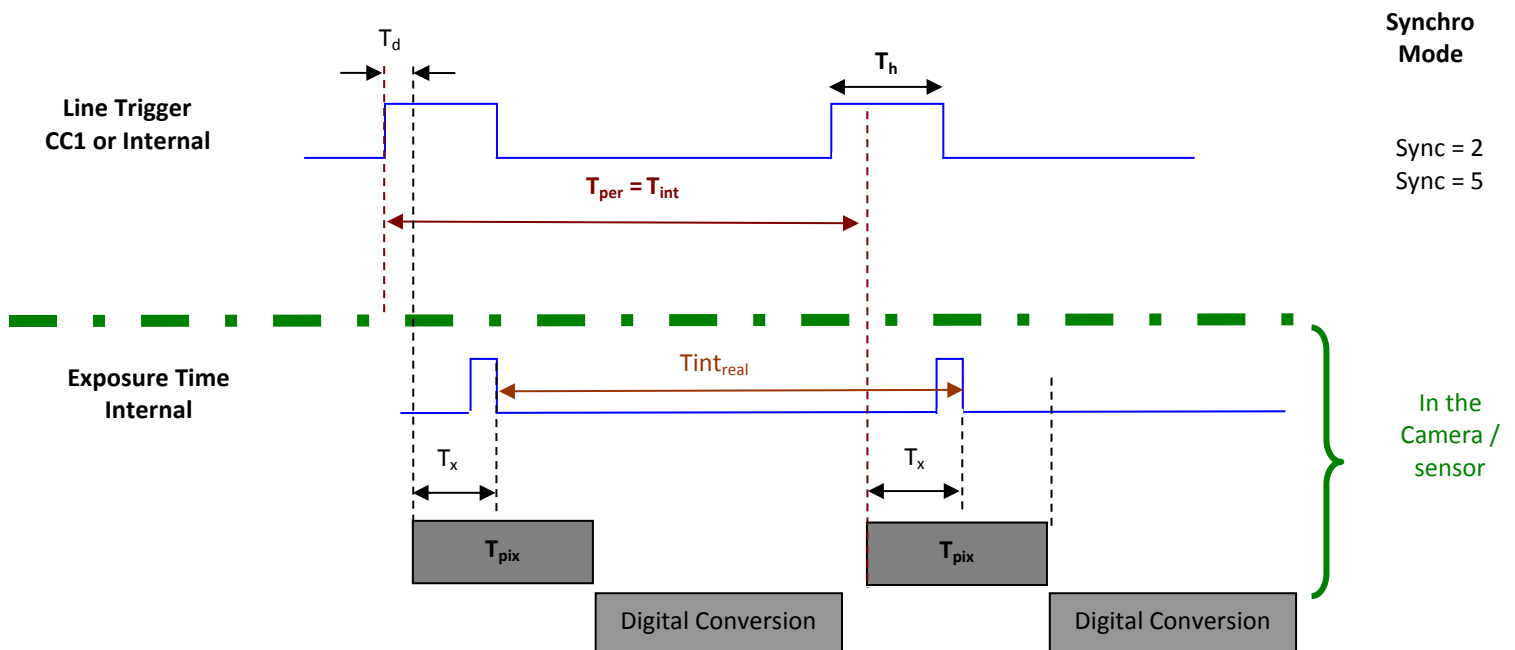


If T_{per} is the Line Period (internal or external coming from the Trigger line), in order to respect this line Period, the Exposure Time as to be set by respecting : $T_{int} + T_{pix} \leq T_{per}$
 Then, the real exposure time is : $T_{int_{real}} = T_{int} + T_x - T_d$
 In the same way, The high level period of the Trig signal in sync=3 mode, $T_{ht} \geq T_{pix}$

For a Line Period of LinePer, the maximum exposure time possible without reduction of line rate

is : $T_{int_{max}} = T_{per} - T_{pix}$ (T_{pix} is defined above) but the effective Exposure Time will be about
 $T_{int_{real}} = T_{int} + T_x - T_d$

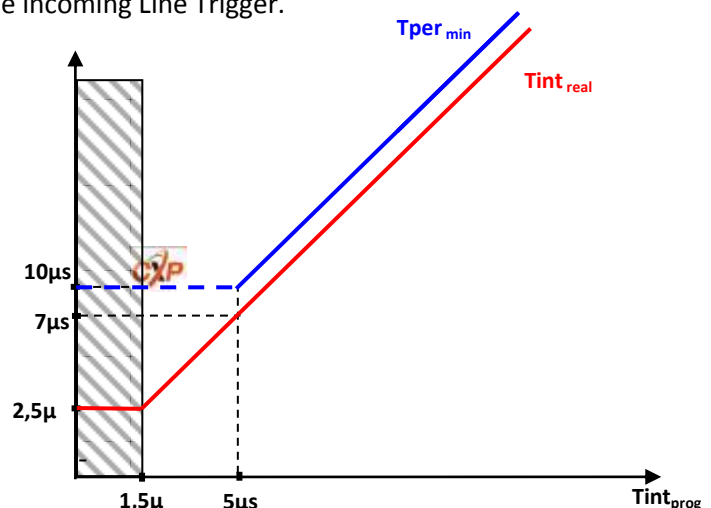
B.2 Synchronisation Modes with Maximum Exposure Time



In these modes, the rising edge of the Trigger (internal or External) starts the readout process (T_{pix}) of the previous integration. The Real exposure time ($T_{int_{real}}$) is finally equal to the Line Period (T_{per}) even if it's delayed from ($T_x + T_d$) from the rising edge of the incoming Line Trigger.

B.3 Timing Values

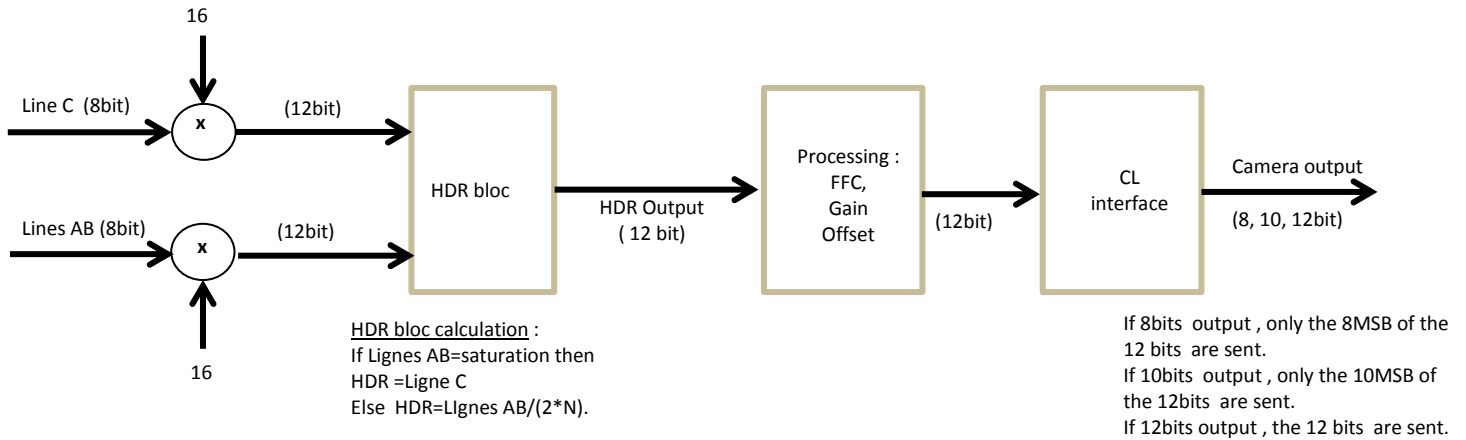
Label	Min	Unit
T_{pix}	5	μs
T_x	3,1	μs
T_h	0,120	μs
T_{ht}	T_{pix}	μsec
T_d	1,1	μs



Appendix C. HDR Mode

C.1 HDR Block

With the HDR Single Line Mode, the “HDR” is calculated in the camera as following :



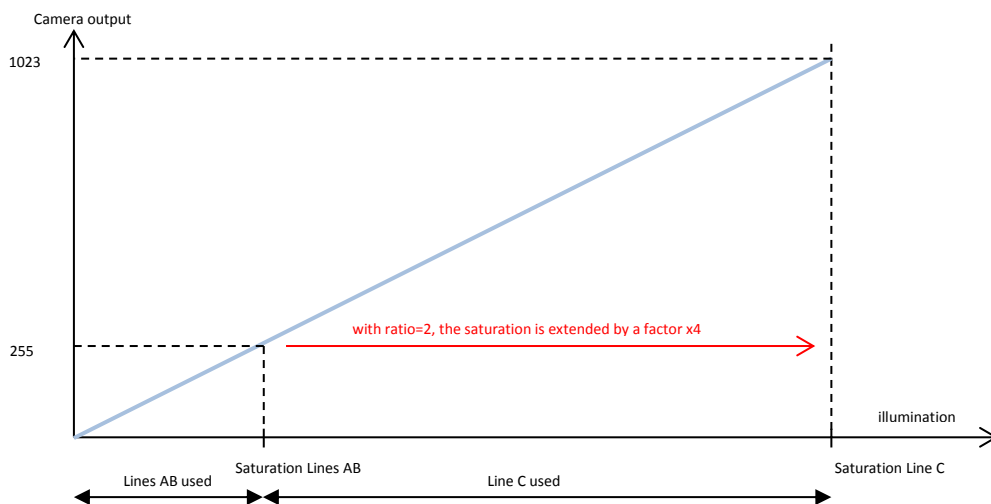
HDR bloc calculation :

If the double Line “AB” is saturating, the information is taken from the single line “C” (Low levels)

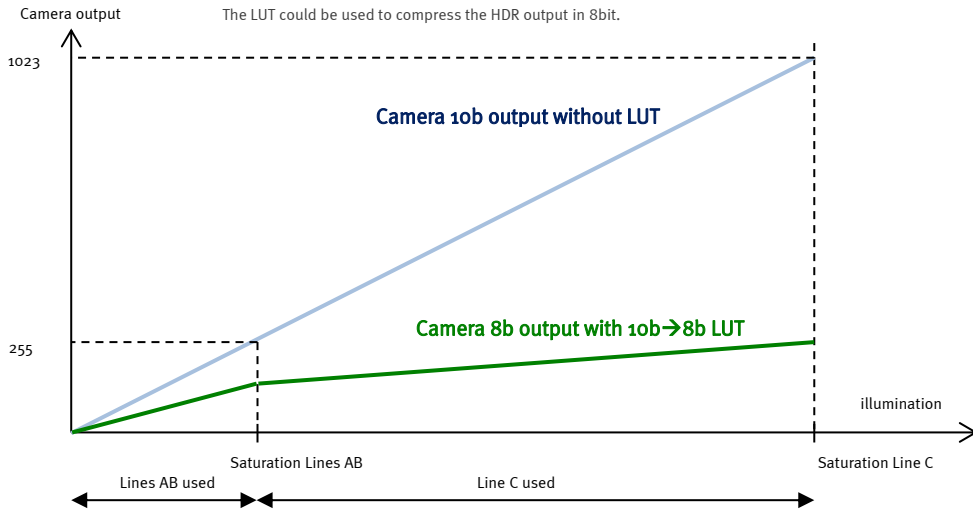
If the double Line “AB” is non saturating, the value taken is issued from these line but divided by $2*N$: N is the ratio set in automatic Exposure mode.

In this case, the maximum dynamic possible is 12 bits : The MSB are taken from the 8bits MSB of the Lines “AB” and divided by 16 max

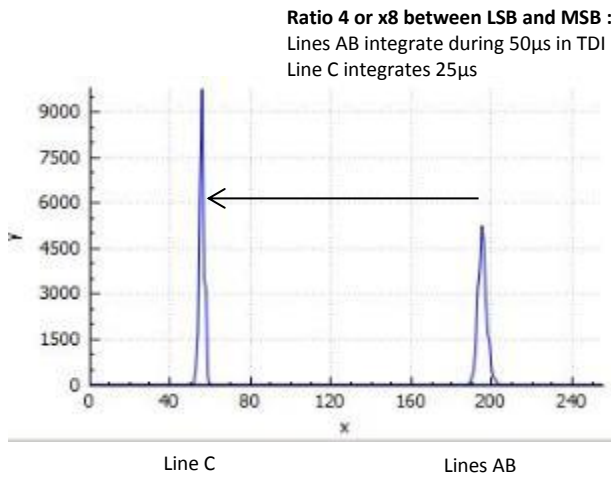
C.2 Example with Ratio 2 and 10bits output



C.3 HDR With LUT 10bits => 8bits



C.4 Example of difference between “AB” and “C” Line :



Appendix D. Data Cables

- CXP cables and the separate lanes of a CXP-multi-cable shall be coaxial with a characteristic impedance of $75\Omega \pm 4\Omega$. When a series connection of CXP-cables is considered, all of the BNC connectors used have to be of the 75Ω type, including any inline couplers.
- A CXP cable and the separate lanes of a CXP-multi-cable shall have a return loss better than or equal to :

Frequency Range	Return Loss
0-500MHz	-20dB
500MHz – 3.2GHz	-15dB

- The maximum length of a CoaXPress cable is the lowest figure from three different requirements: power supply voltage drop, high speed link requirements and low speed link requirements.
 - Power Supply Voltage Drop : A CXP cable and the separate lanes of a CXP multi-cable shall each have a total DC roundtrip resistance of less than 4.98Ω for each of the coax cables.
 - High Speed Link Requirement : A CXP cable and the separate lanes of a CXP-multi-cable that are specified for a given bit rate shall have an attenuation that is less or equal to the following attenuation at its corresponding frequency (example with Belden 1694A Cable) :

Bit Rate (Gbps)	Maximum Attenuation (dB)	@ Frequency (GHz)	Belden 1694A (m)
1.250	-21.2	0.625	130
2.500	-26	1.25	110
3.125	-26.8	1.5625	100
5.000	-20.9	2.5	60
6.250	-15.8	3.125	40

- Low Speed Link Requirement : A CXP cable and the separate lanes of a CXP-multi-cable shall have a signal attenuation at 30 MHz of less than, or equal to, -4.74dB.
- Cable Current Capacity : A CXP cable and the separate lanes of a CXP-multi-cable shall each be designed to carry 1A in normal operation.
- A CXP-cable and the separate lanes of a CXP-multi-cable shall have attenuation versus frequency characteristic exhibiting cable-like behaviour over the frequency ranges as indicated in the table below. A series connection of cables shall also fulfil this requirement as if it is one cable including all of its connectors and inline couplers.

Cable Rating (Gbps)	Frequency Range	
	From	To
1.250	1	0.625
2.500	1	1.25
3.125	1	1.5625
5.000	1	2.5
6.250	-15.8	3.125

Appendix E. Lenses Compatibility

QIOPTICS (LINOS)				
	Nominal Magnification	Magnification Range	M95 Focus tube Reference	Lens Reference Part number
Inspec.x. L 5.6/105	0,33 X	0,25 – 0,45 X	2408-012-000-41	0703-085-000-20
Inspec.x. L 5.6/105	0,5 X	0,4 – 0,65 X	2408-012-000-41	0703-084-000-20
Inspec.x. L 5.6/105	0,87 X	0,6 – 0,9 X	2408-012-000-43	0703-083-000-20
Inspec.x. L 5.6/105	1 X	0,85 – 1,2 X	2408-012-000-43	0703-082-000-20
Inspec.x. L 4/105	3 X	2,8 – 3,3 X	2408-012-000-46	0703-104-000-20
Inspec.x. L 4/105	3,5 X	3,3 – 3,7 X	2408-012-000-44	0703-095-000-21
Inspec.x. L 3.5/105	5 X	4,8 – 5,2 X	2408-012-000-45	0703-102-000-20
SCHNEIDER KREUZNACH				
	Nominal Magnification	Magnification Range	Working Distance (at nom. Mag.)	Reference Part number
SR 5.6/120-0058	1 X	0,88 – 1,13 X	212 mm	1002647
SR 5.6/120-0059	0,75 X	0,63 – 0,88 X	252 mm	1002648
SR 5.6/120-0060	0,5 X	0,38 – 0,63 X	333 mm	1002650
SR 5.6/120-0061	0,33 X	0,26 – 0,38 X	453 mm	1004611
Accessories	V mount 25mm macro-extension tube		Necessary to combine the whole lens system	20179
	V mount to Leica adapter			20054
	Unifoc 76			13048
	Adapter M58x0.75 – M95x1		To be combined to reach the appropriate magnification	1062891
	Extension tube M95x1, 25mm			1062892
	Extension tube M95x1, 50mm			1062893
	Extension tube M95x1, 100mm			1062894
MYUTRON				
	Nominal Magnification	Working Distance	M95 Custom Mount available Aperture (∞) : 4.7	
XLS03-E	x0,3	477mm		
XLS53-E	x0,5	324mm		
XLS75-E	x0,75	246mm		
XLS010-E	x1	197mm		
XLS014-E	x1,4	170mm		
XLS203-E	x2	146mm		
EDMUND OPTICS				
	Nominal Magnification	Working Distance (at nom. Mag.)	Reference Part number	
TechSpec F4	1 X	151 mm	NT68-222	
TechSpec F4	1,33 X	158,5 mm	NT68-223	
TechSpec F4	2,0 X	129 mm	NT68-224	
TechSpec F4	3,0 X	110 mm	NT68-225	
Accessories	Large Format Tip/Tilt Bolt Pattern Adapter, 2X		NT69-235	
	Large Format Focusing Module		NT69-240	
	Large Format Adapter Set		NT69-241	
NAVITAR				
Extension Tubes on request	Extension Tubes on request	Extension Tubes on request	Rayfact ML90mm F4	
NIKON				
Rayfact F4	0,05 X – 0,5 X	1820,4mm – 230,3mm	Rayfact ML90mm F4	

Appendix F. Revision History

Manual Revision	Comments / Details	Firmware version
Rev A	First release	1.0.10A
Rev B	Full Exposure Control Lens compatibility list extension. Cable specifications (Standard)	1.0.13A
Rev C	Quarter Balance Gains	1.0.14C
Rev D	Mode “STB” (Full Exposure control”) adjusted FFC Gains changed from x3 to x5 ROI Gain Feature Detail of the manual Access to FFC area in memory Command List summary with register addresses.	1.0.15B
Rev E	Characterization of the Forward / Reverse feature	1.0.17
Rev F	Documentation details about GenICam Triggers	1.0.17
Rev G	New Documentation Template Low band Filter and 8 memories for FFC	1.2.0
Rev H	Full Exposure Control Mode Parameter Rescaler with embedded Trigger Filter/Averaging Typo errors on documentation. New template	1.3.0
Rev I	New Documentation Template - Trigger too Slow - Average Trigger Filter on Line 2 (CXP Trigger)	1.4.0
Rev J	Full Exposure Control Gain tunable Version BA0 : New Version BH0 with New Sensor and HDR Function :	1.5.0 2.0.1
Rev K	New Teledyne-e2v Chart New Sensor version for BA0 EV71YC4MCP1605-BA0 : EV71YC4MCP1605-BH0 :	2.0.2 2.0.2
Rev L	Typo in Documentation : Rescaler Average function detailed.	-