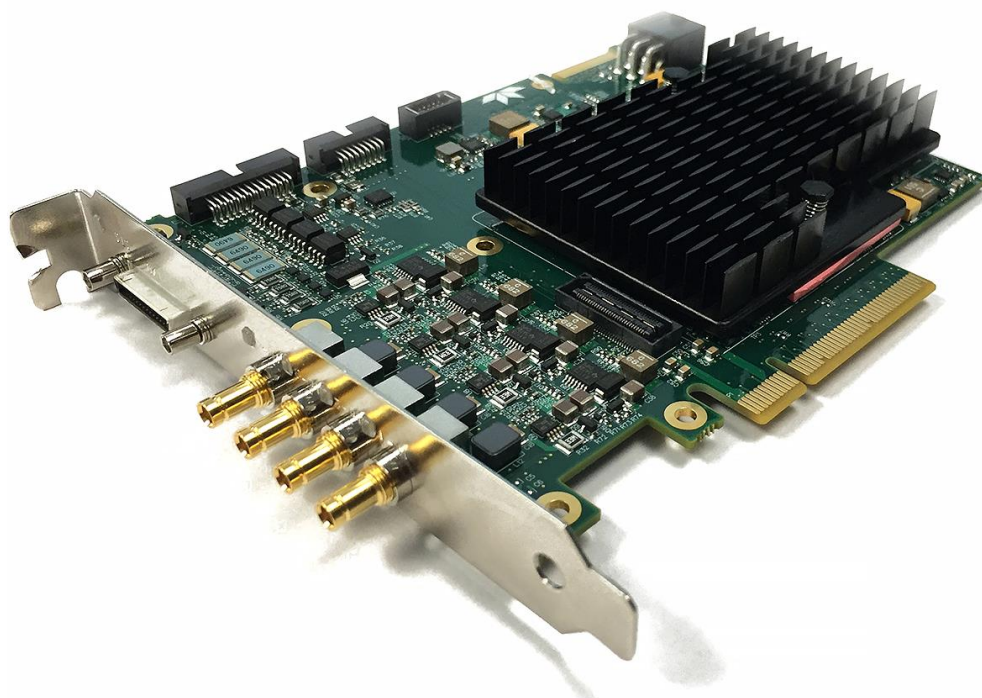


# Xtium-CXP PX8™

User's Manual

Edition 1.30

sensors | cameras | **frame grabbers** | processors | software | vision solutions



P/N: OC-Y8XM-PUSR0  
[www.teledynedalsa.com](http://www.teledynedalsa.com)

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Teledyne Digital Imaging offers the widest range of machine vision components in the world. From industry-leading image sensors through powerful and sophisticated cameras, frame grabbers, vision processors and software to easy-to-use vision appliances and custom vision modules.

# Contents

|   |           |
|---|-----------|
| <b>OVERVIEW .....</b>   | <b>6</b>  |
| PRODUCT PART NUMBERS .....  | 6         |
| ABOUT THE XTIIUM-CXP PX8 FRAME GRABBER .....                                | 7         |
| <i>Series Key Features</i> .....  | 7         |
| <i>User Programmable Configurations</i> .....                               | 7         |
| <i>ACUPlus: Acquisition Control Unit</i> .....                              | 7         |
| <i>DTE: Intelligent Data Transfer Engine</i> .....                          | 8         |
| <i>PCI Express x8 Gen2 Interface</i> .....                                  | 8         |
| <i>Advanced Controls Overview</i> .....                                     | 8         |
| DEVELOPMENT SOFTWARE OVERVIEW .....   | 9         |
| <i>Sapera++ LT Library</i> .....  | 9         |
| <i>Sapera Processing Library</i> .....                                      | 9         |
| <i>About CoaXPress</i> .....  | 9         |
| <br>  |           |
| <b>INSTALLING XTIIUM-CXP PX8 .....</b>                                      | <b>10</b> |
| WARNING! (GROUNDING INSTRUCTIONS) .....                                     | 10        |
| INSTALLATION.....   | 10        |
| <i>Hardware Installation</i> .....  | 10        |
| <i>Sapera LT Library &amp; Xtium-CXP PX8 Driver Installation</i> .....      | 11        |
| <i>Xtium-CXP PX8 Firmware Loader</i> .....                                  | 12        |
| REQUIREMENTS FOR A SILENT INSTALL.....                                      | 15        |
| <i>Silent Mode Installation</i> .....                                       | 15        |
| <i>Silent Mode Uninstall</i> .....  | 16        |
| <i>Silent Mode Installation Return Code</i> .....                           | 16        |
| <i>Installation Setup with CorAppLauncher.exe</i> .....                     | 16        |
| <i>Custom Driver Installation Using install.ini File</i> .....              | 17        |
| UPGRADING SAPERA OR BOARD DRIVER .....                                      | 19        |
| <i>Board Driver Upgrade Only</i> .....                                      | 19        |
| <i>Upgrading both Sapera and Board Driver</i> .....                         | 19        |
| <i>Preserving Board Parameters During Driver Upgrade</i> .....              | 20        |
| PRESERVING BOARD PARAMETERS DURING BOARD REPLACEMENT OR SYSTEM CLONING..... | 21        |
| DISPLAYING XTIIUM-CXP PX8 BOARD INFORMATION .....                           | 22        |
| <i>Device Manager – Board Viewer</i> .....                                  | 22        |
| <i>Information Field Description</i> .....                                  | 23        |
| <i>Device Information Report</i> .....                                      | 25        |
| CONFIGURING SAPERA.....   | 25        |
| <i>Viewing Installed Sapera Servers</i> .....                               | 25        |
| <i>Increasing Contiguous Memory for Sapera Resources</i> .....              | 25        |
| <br>  |           |
| <b>TROUBLESHOOTING PROBLEMS .....</b>                                       | <b>27</b> |
| OVERVIEW .....  | 27        |
| PROBLEM TYPE SUMMARY .....  | 27        |
| <i>First Step: Check the Status LED</i> .....                               | 27        |
| <i>Possible Installation Problems</i> .....                                 | 27        |
| <i>Possible Functional Problems</i> .....                                   | 28        |
| TROUBLESHOOTING PROCEDURES .....  | 28        |
| <i>Diagnostic Tool Overview</i> .....                                       | 28        |
| <i>Checking for PCI Bus Conflicts</i> .....                                 | 31        |
| <i>Windows Device Manager</i> .....   | 33        |
| <i>BSOD (blue screen) Following a Board Reset</i> .....                     | 33        |
| <i>Sapera and Hardware Windows Drivers</i> .....                            | 34        |
| <i>Recovering from a Firmware Update Error</i> .....                        | 34        |

|  |           |
|--|-----------|
| <i>Driver Information via the Device Manager Program</i> .....                                   | 35        |
| <i>Teledyne DALSA Log Viewer</i> .....   | 36        |
| <i>On-board Image Memory Requirements for Acquisitions</i> .....                                 | 36        |
| <i>Symptoms: CamExpert Detects no Boards</i> .....   | 36        |
| <i>Symptoms: Xtium-CXP PX8 Does Not Grab</i> .....   | 37        |
| <i>Symptoms: Card grabs black</i> .....  | 37        |
| <i>Symptoms: Card acquisition bandwidth is less than expected</i> .....                          | 38        |
| <i>Symptoms: PoCXP does not power the camera</i> .....   | 38        |
| <b>CAMEXPERT QUICK START .....</b>   | <b>40</b> |
| INTERFACING CXP CAMERAS WITH CAMEXPERT .....   | 40        |
| <i>CamExpert Example with a Monochrome Camera</i> .....  | 40        |
| CAMEXPERT DEMONSTRATION AND TEST TOOLS .....   | 42        |
| <i>Camera Types &amp; Files</i> .....  | 42        |
| <i>Overview of Sapera Acquisition Parameter Files (*.ccf or *.cca/*.cvi)</i> .....               | 42        |
| <i>Saving a Camera File</i> .....  | 43        |
| <i>Camera Interfacing Check List</i> .....   | 43        |
| USING THE FLAT FIELD CORRECTION TOOL.....  | 44        |
| <i>Xtium-CXP PX8 Flat Field Support</i> .....  | 44        |
| <i>Set up Dark and Bright Acquisitions with the Histogram Tool</i> .....                         | 44        |
| <i>Flat Field Correction Calibration Procedure</i> .....   | 46        |
| <i>Using Flat Field Correction</i> .....   | 47        |
| USING THE BAYER FILTER TOOL .....  | 48        |
| <i>Bayer Filter White Balance Calibration Procedure</i> .....                                    | 48        |
| <b>SAPERA DEMO APPLICATIONS .....</b>  | <b>49</b> |
| GRAB DEMO OVERVIEW .....   | 49        |
| <i>Using the Grab Demo</i> .....   | 50        |
| <b>XTIUM-CXP PX8 REFERENCE .....</b>   | <b>51</b> |
| BLOCK DIAGRAM.....   | 51        |
| XTIUM-CXP FLOW DIAGRAM .....   | 52        |
| LINE TRIGGER SOURCE SELECTION FOR LINE SCAN APPLICATIONS .....                                   | 53        |
| <i>CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE – Parameter Values Specific to the Xtium-CXP PX8</i> ..... | 53        |
| SHAFT ENCODER INTERFACE TIMING .....   | 54        |
| VIRTUAL FRAME TRIGGER FOR LINE SCAN CAMERAS .....  | 56        |
| <i>CVI File (VIC) Parameters Used</i> .....  | 60        |
| SAPERA ACQUISITION METHODS .....   | 61        |
| TRIGGER TO IMAGE RELIABILITY .....   | 62        |
| <i>Supported Events and Transfer Methods</i> .....   | 62        |
| <i>Transfer Events</i> .....   | 64        |
| OUTPUT LUT AVAILABILITY .....  | 66        |
| FLAT FIELD CORRECTION: THEORY OF OPERATION .....   | 67        |
| <i>Flat Field Correction Lists</i> .....   | 67        |
| <i>Flat Field Correction Sets</i> .....  | 68        |
| XTIUM-CXP PX8 SUPPORTED PARAMETERS .....   | 69        |
| <i>Camera Related Capabilities</i> .....   | 69        |
| <i>Camera Related Parameters</i> .....   | 69        |
| <i>VIC Related Parameters</i> .....  | 71        |
| <i>ACQ Related Parameters</i> .....  | 75        |
| <i>Transfer Related Capabilities</i> .....   | 77        |
| <i>Transfer Related Parameters</i> .....   | 77        |
| <i>General Outputs #1: Related Capabilities (for GIO Module #0)</i> .....                        | 77        |
| <i>General Outputs #1: Related Parameters (for GIO Module #0)</i> .....                          | 78        |
| <i>General Inputs #1: Related Capabilities (for GIO Module #1)</i> .....                         | 78        |
| <i>General Inputs #1: Related Parameters (for GIO Module #1)</i> .....                           | 78        |
| <i>Bidirectional General I/Os: Related Capabilities (for GIO Module #2)</i> .....                | 78        |

|   |                |
|---|----------------|
| <i>Bidirectional General I/Os: Related Parameters (for GIO Module #2)</i> ..... | 79             |
| SAPERA SERVERS AND RESOURCES .....  | 80             |
| <b>TECHNICAL SPECIFICATIONS</b> .....   | <b>82</b>      |
| XTIUM-CXP PX8 BOARD SPECIFICATIONS .....  | 82             |
| HOST SYSTEM REQUIREMENTS .....  | 83             |
| EMI CERTIFICATIONS .....  | 84             |
| CONNECTOR AND SWITCH LOCATIONS .....  | 85             |
| <i>Xtium-CXP PX8 Board Layout Drawing</i> .....                                 | 85             |
| <i>Connector / LED Description List</i> .....                                   | 85             |
| CONNECTOR AND SWITCH SPECIFICATIONS .....                                       | 86             |
| <i>Xtium-CXP PX8 End Bracket Detail</i> .....                                   | 86             |
| <i>Status LEDs Functional Descriptions</i> .....                                | 87             |
| <i>J1: External I/O Signals Connector (Female DH60-27P)</i> .....               | 88             |
| <i>J7: Internal I/O Signals Connector (26-pin SHF-113-01-L-D-RA)</i> .....      | 88             |
| <i>J2, J3, J4, J5: CoaXPress Connector</i> .....                                | 97             |
| <i>J9: Multi-Board Sync / Bi-directional General I/Os</i> .....                 | 97             |
| <i>J12: Power Connector</i> .....   | 99             |
| CABLES & ACCESSORIES .....  | 100            |
| <i>CoaXPress Cables</i> .....   | 100            |
| <i>DH40-27S Cable to Blunt End (OR-YXCC-27BE2M1, Rev B1)</i> .....              | 100            |
| <i>DH40-27S Connector Kit for Custom Wiring</i> .....                           | 101            |
| <i>Cable assemblies for I/O connector J7</i> .....                              | 103            |
| <i>Board Sync Cable Assembly OR-YXCC-BSYNC40</i> .....                          | 104            |
| <i>Power Cable Assembly OR-YXCC-PWRY00</i> .....                                | 105            |
| <br><b>COAXPRESS INTERFACE</b> .....  | <br><b>106</b> |
| COAXPRESS OVERVIEW .....  | 106            |
| <br><b>CONTACT INFORMATION</b> .....  | <br><b>107</b> |
| SALES INFORMATION.....  | 107            |
| TECHNICAL SUPPORT.....  | 107            |

# Tables

|  |    |
|--|----|
| Table 1: Xtium-CXP PX8 Board Product Numbers .....                   | 6  |
| Table 2: Xtium-CXP PX8 Software Product Numbers .....                | 6  |
| Table 3: Xtium-CXP PX8 Cables & Accessories .....                    | 6  |
| Table 4: Xtium-CXP PX8 Device Drivers .....                          | 34 |
| Table 5: Grab Demo Workspace Details .....                           | 49 |
| Table 6: CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE – Parameter Values ..... | 53 |
| Table 7: Output LUT Availability .....                               | 66 |
| Table 8: Camera Related Capabilities.....                            | 69 |
| Table 9: Camera Related Parameters.....                              | 69 |
| Table 10: VIC Related Parameters .....                               | 71 |
| Table 11: Acquisition Related Parameters.....                        | 75 |
| Table 12: Transfer Related Capabilities .....                        | 77 |
| Table 13: Transfer Related Parameters .....                          | 77 |
| Table 14: GIO-0 Related Capabilities .....                           | 77 |
| Table 15: GIO-0 Related Parameters .....                             | 78 |
| Table 16: GIO-1 Related Capabilities .....                           | 78 |
| Table 17: GIO-1 Related Parameters .....                             | 78 |
| Table 18: GIO-1 Related Parameters .....                             | 78 |
| Table 19: GIO-2 Related Parameters .....                             | 79 |

|   |     |
|---|-----|
| Table 20: Xtium-CXP PX8 - Servers and Resources.....          | 80  |
| Table 21: Board Specifications .....                          | 82  |
| Table 22: Environment Specifications .....                    | 83  |
| Table 23: Power Specifications.....                           | 83  |
| Table 24: Board Connector List .....                          | 85  |
| Table 25: D1 Boot-up/PCIe Status LED .....                    | 87  |
| Table 26: Camera CXP Status LED.....                          | 87  |
| Table 27: DH60-27P/ SHF-113-01-L-D-RA Connector Signals ..... | 88  |
| Table 28: External Trigger Timing Specifications .....        | 90  |
| Table 29: Input Switching Points and Propagation Delay .....  | 90  |
| Table 30: External Driver Electrical Requirements .....       | 91  |
| Table 31: External Receiver Electrical Requirements .....     | 93  |
| Table 32: CoaXPress Cable Suppliers .....                     | 100 |

# Figures

|  |    |
|--|----|
| Figure 1: Automatic Firmware Update .....  | 12 |
| Figure 2: Manual Firmware Update .....   | 13 |
| Figure 3: Firmware Update Progress .....   | 13 |
| Figure 4: Start Menu Firmware Update Shortcut.....   | 14 |
| Figure 5: Create an install.ini File .....   | 17 |
| Figure 6: INI Configuration.....   | 18 |
| Figure 7: Device Manager Parameter Setting Differences.....                                    | 20 |
| Figure 8: Firmware Update Status .....   | 21 |
| Figure 9: Same Firmware For All Devices Checkbox .....   | 21 |
| Figure 10: Board Information via Device Manager .....  | 22 |
| Figure 11: Device Manager File Menu Save Device Info Command.....                              | 25 |
| Figure 12: Diagnostic Tool Main Window .....   | 29 |
| Figure 13: Diagnostic Tool Main Window .....   | 30 |
| Figure 14: Diagnostic Tool Live Monitoring Window.....   | 31 |
| Figure 15: PCI Diagnostic Program .....  | 32 |
| Figure 16: PCI Diagnostic Program – PCI bus info .....   | 32 |
| Figure 17: Using Windows Device Manager.....   | 33 |
| Figure 18: Board Firmware Version.....   | 35 |
| Figure 19: PCI Diagnostic Tool .....   | 37 |
| Figure 20: CamExpert PoCXP Parameter .....   | 38 |
| Figure 21: CamExpert Video Status Bar .....  | 38 |
| Figure 22: Bad vs. Good CXP Connectors .....   | 39 |
| Figure 23: CamExpert Program .....   | 40 |
| Figure 24: CamExpert Device Tree .....   | 41 |
| Figure 25: CamExpert Histogram of Dark Image .....   | 45 |
| Figure 26: CamExpert Histogram of Bright Image .....   | 46 |
| Figure 27: CamExpert Flat Field Correction Menu Command .....                                  | 46 |
| Figure 28: CamExpert Flat Field Correction Dialog .....  | 47 |
| Figure 29: Xtium-CXP PX8 Block Diagram.....  | 51 |
| Figure 30: Xtium-CXP Flow Diagram.....   | 52 |
| Figure 31: Encoder Input with Pulse-drop Counter.....  | 54 |
| Figure 32: Using Shaft Encoder Direction Parameter .....                                       | 55 |
| Figure 33: Synchronization Signals for a 10 Line Virtual Frame .....                           | 57 |
| Figure 34: Line scan, Fixed Frame, No Trigger .....  | 58 |
| Figure 35: Line scan, Fixed Frame, Edge Trigger .....  | 58 |
| Figure 36: Line scan, Fixed Frame, Level Trigger (Roll-Over to Next Frame) .....               | 59 |
| Figure 37: Line scan, Variable Frame, Edge Trigger (Active High determines Frame Length) ..... | 59 |
| Figure 38: Line scan, Fixed Frame, Level Trigger ( Roll-Over) .....                            | 60 |
| Figure 39: EMI Certifications.....   | 84 |

|  |     |
|--|-----|
| Figure 40: Board Layout.....                                   | 85  |
| Figure 41: End Bracket Details.....                            | 86  |
| Figure 42: General Inputs Electrical Diagram.....              | 89  |
| Figure 43: External Trigger Input Validation & Delay.....      | 90  |
| Figure 44: External Signals Connection Diagram.....            | 91  |
| Figure 45: General Outputs Electrical Diagram.....             | 92  |
| Figure 46: Output Signals Connection Diagram.....              | 93  |
| Figure 47: RS-422 Shaft Encoder Input Electrical Diagram.....  | 94  |
| Figure 48: External RS-422 Signals Connection Diagram.....     | 95  |
| Figure 49: Interfacing TTL to RS-422 Shaft Encoder Inputs..... | 96  |
| Figure 50: Interfacing to a Line Driver Output.....            | 96  |
| Figure 51: Interfacing to an Open Collector Output.....        | 97  |
| Figure 52: DH60-27P Cable No. OR-YXCC-27BE2M1 Detail.....      | 100 |
| Figure 53: Photo of cable OR-YXCC-27BE2M1.....                 | 101 |
| Figure 54: OR-YXCC-H270000 Custom Wiring Kit.....              | 101 |
| Figure 55: OR-YXCC-H270000 Pin Configuration.....              | 102 |
| Figure 56: I/O Cable #OR-YXCC-TIOF120.....                     | 103 |
| Figure 57: Photo of cable OR-YXCC-BSYNC40.....                 | 104 |
| Figure 58: Photo of cable assembly OR-YXCC-PWRY00.....         | 105 |

# Overview

## Product Part Numbers

### Xtium-CXP PX8 Board

Table 1: Xtium-CXP PX8 Board Product Numbers

| Item  | Product Number |
|---|----------------|
| Xtium-CXP PX8 Quad  | OR-Y8X0-XPX400 |
| For OEM clients, this manual in printed form, is available on request | OC-Y8XM-PUSR0  |

### Xtium-CXP PX8 Software

Table 2: Xtium-CXP PX8 Software Product Numbers

| Item  | Product Number  |
|---|---|
| Sapera LT version 8.40 or later for full feature support (required) <ol style="list-style-type: none"> <li>1. Sapera LT:<br/>Provides everything needed to build imaging application</li> <li>2. Current Sapera compliant board hardware drivers</li> <li>3. Sapera documentation:<br/>(compiled HTML help, Adobe Acrobat® (PDF)</li> </ol> | Free download at the <a href="#">Teledyne DALSA website</a> . |
| (optional) Sapera Processing Imaging Development Library includes over 600 optimized image-processing routines.   | Contact Sales at Teledyne DALSA                               |

### Optional Xtium-CXP PX8 Cables & Accessories

Table 3: Xtium-CXP PX8 Cables & Accessories

| Item   | Product Number   |
|--|--|
| <b>DH40-27S cable assembly to blunt end:</b> 6 ft. cable I/O 27 pin Hirose connector to blunt end. This cable assembly connects to J1. | <a href="#">OR-YXCC-27BE2M1</a>                                    |
| Cable set to connect to J7 Internal I/O Signals connector (J7: 26-pin SHF-113-01-L-D-RA)   | <a href="#">see suggested cables</a>                               |
| DH40-27S Connector Kit for Custom Wiring:<br>Comprised of a DH40-27S connector plus screw lock housing kit                             | <a href="#">OR-YXCC-H270000</a>                                    |
| Cable assembly to connect to J9 (Board Sync)<br>Connecting 2 boards<br>Connection 3 or 4 boards  | <a href="#">OR-YXCC-BSYNC20</a><br><a href="#">OR-YXCC-BSYNC40</a> |
| Power interface cable required when supplying power to J1  | <a href="#">OR-YXCC-PWRY00</a>                                     |
| CXP Cable:   | Refer to the CoaXPress Cables section.                             |



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# About the Xtium-CXP PX8 Frame Grabber

## Series Key Features

- Compatible with CoaXPress (CXP) specification version 1.0, 1.1 and 1.1.1 (visit <http://jiiia.org/en/> for details on industry standards)
- Supports up to 4 lanes of 6.250 Gbps each (4 cables gives 25 Gbps)
- The specification defines a device discovery methodology that can be automated and which provides plug and play capability
- CoaXPress cameras implement GenICam and associated GenCP, thus resulting in ease of use for Teledyne DALSA or third party cameras
- Uses a PCIe x8 Gen2 slot to maximize transfers to host computer buffers
- Acquire from Monochrome (8/10/12/14/16 bits per pixel), RGB (8/10/12 bits per pixel) CXP cameras, both area scan and line scan
- Acquire from Bayer (8/10/12 bits per pixel) CXP area scan cameras
- Output lookup tables
- Vertical and Horizontal Flip supported on board
- Flat Field and Flat Line correction: pixel replacement using neighborhood pixels
- External Input Triggers and Shaft Encoder inputs, along with Strobe outputs
- Supports Multi-board Sync for trigger events, to simultaneously acquire from multiple cameras.
- Supports a number of acquisition events in compliance with "Teledyne DALSA's Trigger to Image Reliability"
- RoHS compliant

See Technical Specifications for detailed information.

## User Programmable Configurations

Use the Xtium-CXP PX8 firmware loader function in the Teledyne DALSA Device manager utility to select firmware for one of the supported modes. Firmware selection is made either during driver installation or manually later on (see Firmware Update: Manual Mode).

### Firmware choices are:

- **One CXP Camera** (*installation default*):  
Support for 1 CXP camera of 1, 2 or 4 links (that is, physical CXP cable connections)
- **Two CXP Cameras:**  
Support for 2 independent CXP cameras of 1 or 2 links.
- **Three CXP Cameras:**  
Support for 3 independent CXP cameras of 1 link, or 2 cameras of 1 link and 1 camera of 2 links.
- **Four CXP Cameras:**  
Support for 4 independent CXP cameras of 1 link.

## ACUPlus: Acquisition Control Unit

ACUPlus consists of a grab controller, one pixel packer, and one time base generator per camera input.

ACUPlus acquires variable frame sizes up to 64KB per horizontal line and up to 64K lines per frame. ACUPlus can also capture an infinite number of lines from a line scan camera without losing a single line of data.

## DTE: Intelligent Data Transfer Engine

The Xtium-CXP PX8 intelligent Data Transfer Engine ensures fast image data transfers between the board and the host computer with zero CPU usage. The DTE provides a high degree of data integrity during continuous image acquisition in a non-real time operating system like Windows. DTE consists of intelligent DMA units with auto-loading Scatter-Gather tables.

## PCI Express x8 Gen2 Interface

The Xtium-CXP PX8 is a universal PCI Express x8 Gen2 board, compliant with the PCI Express 2.0 specification. The Xtium-CXP PX8 board achieves transfer rates up to 3.4Gbytes/sec. to host memory. Note that performance can be lower depending on PC and/or programmed configuration.

The Xtium-CXP PX8 board occupies one PCI Express x8 Gen2 expansion slot and one chassis opening.

### Important:

- To obtain the maximum transfer rate to host memory, make sure the Xtium-CXP PX8 is in a computer with a Gen2 slot. The board will work in a Gen1 slot, but only with half the possible transfer performance.
- The system motherboard BIOS should allow setting the PCIe maximum payload size to 256 or higher. Systems with fixed settings of 128 will limit performance for transfers to host memory.
- If the computer only has a PCI Express x16 slot, test directly (use the supplied [diagnostic tool](#)) or review the computer documentation to know if the Xtium-CXP PX8 is supported. Computer motherboards may only support x16 graphic video board products in x16 slots.

## Advanced Controls Overview

### Visual Indicators

Xtium-CXP PX8 features 5 LED indicators to facilitate system installation and setup (see [Status LEDs Functional Descriptions](#)). These indicators provide visual feedback on the board status and camera status.

### External Event Synchronization

Trigger inputs and strobe signals precisely synchronize image captures with external events.

### CoaXPress Communication Port

One Sopera LT Acquisition Device per camera input provides access to the CoaXPress camera configuration via the board device driver. The communication port presents a seamless interface to access GenICam camera features.

### Quadrature Shaft Encoder

An important feature for web scanning applications, the Quadrature Shaft Encoder inputs allow synchronized line captures from external web encoders (see [J1- I/O Connector](#)). The Xtium-CXP PX8 provides a RS-422 input that supports a tick rate of up to 5 MHz.

---

# Development Software Overview

## Sapera++ LT Library

Sapera++ LT is a powerful development library for image acquisition and control. Sapera++ LT provides a single API across all current and future Teledyne DALSA hardware. Sapera++ LT delivers a comprehensive feature set including program portability, versatile camera controls, flexible display functionality and management, plus easy to use application development wizards. Applications are developed using either C++ or .NET frameworks.

Sapera++ LT comes bundled with CamExpert, an easy to use camera configuration utility to create new, or modify existing camera configuration files.

## Sapera Processing Library

Sapera Processing is a comprehensive set of C++ classes or .NET classes for image processing and analysis. Sapera Processing offers highly optimized tools for image processing, blob analysis, search (pattern recognition), OCR and barcode decoding.

## About CoaXPress



Xtium-CXP PX8 frame grabbers are 100% compliant with the CoaXPress 1.1 specification which defines the communication interface protocol used between devices and supports CXP-1 through CXP-6.

For more information see:

<http://www.coaxpress.com/resources/>

CoaXPress (CXP) is an asymmetric high-speed point-to-point serial communication standard for the transmission of video and still images, scalable over single or multiple coaxial cables. It supports cable speeds of up to 6.25 Gbps for video, images and data, plus a lower speed uplink up to 20 Mbps for communications and control. Power is also available over the cable ("Power-over-Coax") and cable lengths of greater than 100m may be achieved.

The standard is hosted by the Japanese Industrial Imaging Association ([JIIA](#)) with working groups from companies around the world.

# Installing Xtium-CXP PX8

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## Warning! (Grounding Instructions)

Static electricity can damage electronic components. Please discharge any static electrical charge by touching a grounded surface, such as the metal computer chassis, before performing any hardware installation. If you do not feel comfortable performing the installation, please consult a qualified computer technician.



**Important:** Never remove or install any hardware component with the computer power on. Disconnect the power cord from the computer to disable the power standby mode. This prevents the case where some computers unexpectedly power up when a board is installed.

---

## Installation

The installation sequence is as follows:

- Install the board hardware into an available PCI Express x8 Gen2 slot.
- Turn on the computer.
- Install the Sapera LT Development Library or only its 'runtime library'.
- Install the Xtium-CXP PX8 Sapera board driver.
- Update the board firmware if required.
- Reboot the computer.
- Connect a CXP camera and test.

## Hardware Installation

- Turn the computer off, disconnect the power cord (disables power standby mode), and open the computer chassis to allow access to the expansion slot area.
- Install the Xtium-CXP PX8 into a free PCI Express x8 Gen2 expansion slot . Note that some computer's x16 slot may support boards such as the Xtium-CXP PX8, not just display adapters.
- Connect a spare power supply connector to [J12](#) for PoCXP cameras or when DC power is required on the external signals connector [J1/J7](#). See Power Cable Assembly OR-YXCC-PWRY00 for information about an adapter for older computers.
- Close the computer chassis and turn the computer on.
- Logon to the computer as administrator or with an account that has administrator privileges.
- [Connect a CXP camera](#) to J2, J3, J4 and J5 after installing Sapera as described below. Test with [CamExpert](#).

## Multi-board Sync & I/O Setup

- For multi-board sync applications, see J9: Multi-Board Sync / Bi-directional General I/Os for information on using two to four Xtium-CXP boards in one computer.

# Sapera LT Library & Xtium-CXP PX8 Driver Installation

**Sapera LT SDK (full version)**, the image acquisition and control SDK for Teledyne DALSA cameras and frame grabbers is available for download from the Teledyne DALSA website:

<http://teledynedalsa.com/imaging/support/downloads/sdks/>

Run-time versions are also available for download at this location.



## Software Development Kits

Access to certain drivers and SDK updates are restricted to Teledyne DALSA customers that have registered their development package (SDK). If you have not yet done so, please [register your software](#) before proceeding.

| Description  | Version | Release Date |
|--|---------|--------------|
| <a href="#">Sapera LT SDK (full version) - Free Download</a> | 8.30    | 05/19/2017   |



The Sapera LT SDK installation includes compiled demo and example programs, along with project source code, in both C++ and .NET languages, for most Microsoft Visual Studio development platforms. The Sapera LT ++ and Sapera LT .NET demo source code are found in the Sapera\Demos directory.

## Teledyne DALSA Device Drivers

All Teledyne DALSA device drivers are available for download from the Teledyne DALSA website:

<https://www.teledynedalsa.com/imaging/support/downloads/drivers/>

### Installation Procedure

- Sapera LT is installed before Teledyne DALSA board drivers.
- Download the Sapera LT SDK from the Teledyne DALSA website and run the executable file; the installation menu is presented.
- The installation program may prompt to reboot the computer. It is not necessary to reboot the computer between the installation of Sapera LT and the board driver.
- Download the Xtium-CXP PX8 device driver from the Teledyne DALSA website and run the executable file; the installation menu is presented.
- During the late stages of the installation, the Xtium-CXP PX8 firmware loader application starts. This is described in detail in the following section.
- Reboot once all the software and board drivers are installed.




If Windows displays any unexpected message concerning the board, power off the system and verify the Xtium-CXP PX8 is installed in the slot properly. You should also note the board's status LED color and compare it to the defined LED states as described in [D1: Boot-up/PCIe Status LED](#).

Refer to *Sapera LT User's Manual* for additional details about Sapera LT.

# Xtium-CXP PX8 Firmware Loader

The Device Manager-Firmware Loader program automatically executes at the end of the driver installation and on every subsequent reboot of the computer. It will determine if the Xtium-CXP PX8 requires a firmware update. If firmware is required, a dialog displays. This dialog also allows the user to load alternative firmware if available for the Xtium-CXP PX8.

Note: Administrator rights are required to update the device information and/or firmware.

|   |  |
|---|--|
|  | <b>Important:</b> In the rare case of firmware loader errors please see Recovering from a Firmware Update Error. |
|---|--|

## Firmware Update: Automatic Mode

Click **Automatic** to update the Xtium-CXP PX8 firmware. The **Xtium-CXP PX8** supports various firmware configurations where the default can acquire from a 1, 2 or 4 lane CXP camera.

See User Programmable Configurations for details on all supported modes, selected via a manual update of alternative firmware.

With multiple Xtium-CXP PX8 boards in the system, all are updated with new firmware. If any installed Xtium-CXP PX8 board installed in a system already has the correct firmware version, an update is not required. In the following screen shot a single Xtium-CXP PX8 board is installed and ready for a firmware upgrade.

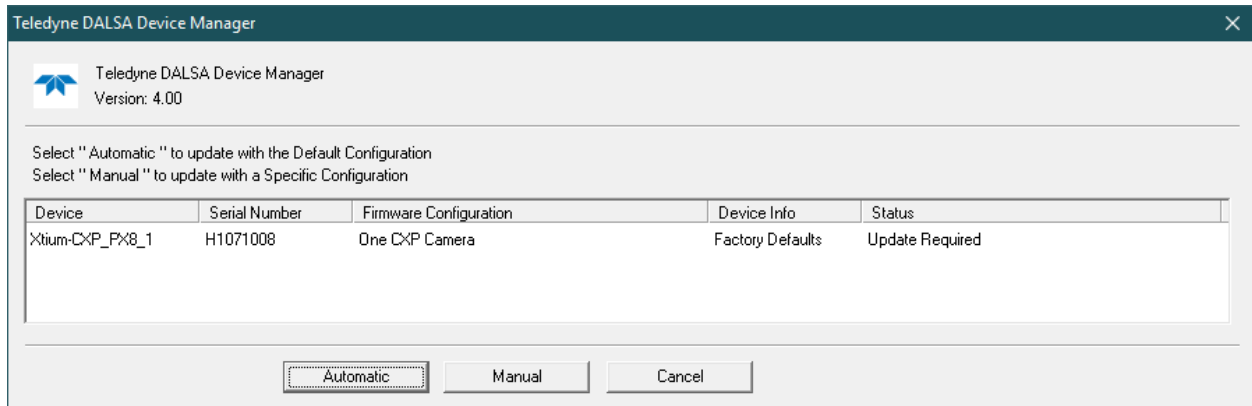


Figure 1: Automatic Firmware Update

## Firmware Update: Manual Mode

Select **Manual** mode to load firmware other than the default version or when, in the case of multiple Xtium-CXP PX8 boards in the same system, if each requires different firmware.

The following figure shows the Device Manager manual firmware screen. Displayed is information on all installed Xtium-CXP PX8 boards, their serial numbers, and their firmware components.

### Do a manual firmware update as follows:

- Select the Xtium-CXP PX8 to update via the board selection box (if there are multiple boards in the system).
- From the Configuration field drop menu select the firmware version required (typical required or offered to support different CXP cameras).
- Click on the Start Update button.

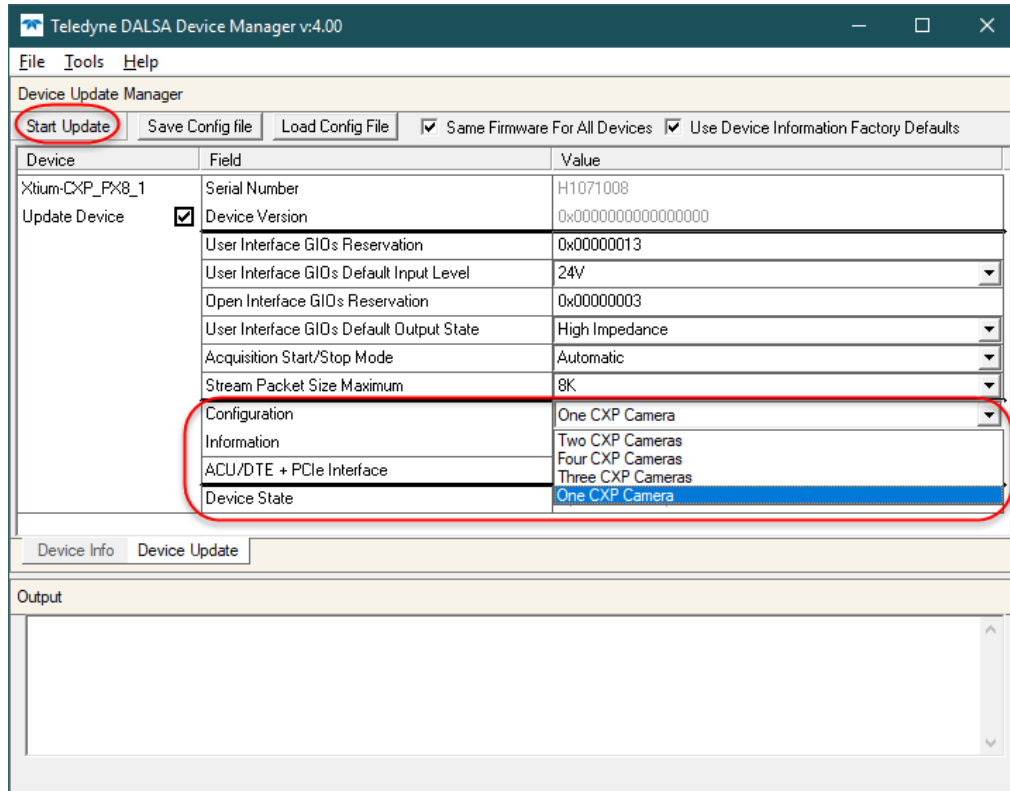


Figure 2: Manual Firmware Update

- Observe the firmware update progress in the message output window.

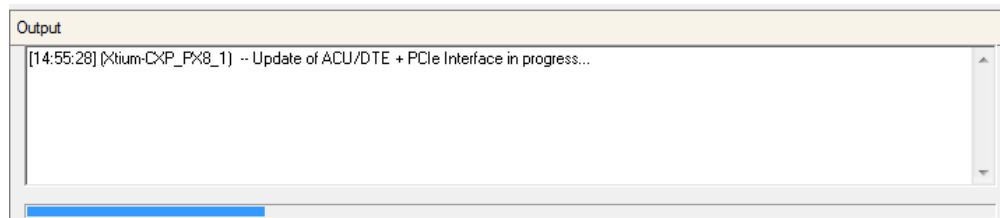
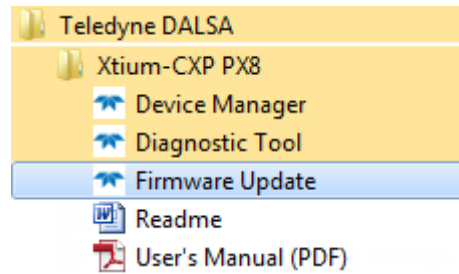


Figure 3: Firmware Update Progress

- Close the Device manager program when the device reset complete message is shown.

### ***Executing the Firmware Loader from the Start Menu***

If required, the Xtium-CXP PX8 Firmware Loader program is executed via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • Xtium-CXP PX8 • Firmware Update**. A firmware change after installation would be required to select a different configuration mode. See User Programmable Configurations.



*Figure 4: Start Menu Firmware Update Shortcut*



---

# Requirements for a Silent Install

Both Sapera LT and the Xtium-CXP PX8 driver installations share the same installer technology. When the installations of Teledyne DALSA products are embedded within a third party's product installation, the mode can either have user interaction or be completely silent. The following installation mode descriptions apply to both Sapera and the hardware driver.



**Note:** You must reboot after the installation of Sapera LT. However, to streamline the installation process, Sapera LT can be installed without rebooting before installing the board hardware device drivers. The installations then complete with a single final system reboot.

Perform Teledyne DALSA embedded installations in either of these two ways:

- **Normal Mode**  
The default mode is interactive. This is identical to running the setup.exe program manually from Windows (either run from Windows Explorer or the Windows command line).
- **Silent Mode**  
This mode requires no user interaction. A preconfigured "response" file provides the user input. The installer displays nothing.

## Silent Mode Installation

A Silent Mode installation is recommended when integrating Teledyne DALSA products into your software installation. The silent installation mode allows the device driver installation to proceed without the need for mouse clicks or other input from a user.

Preparing a Silent Mode Installation requires two steps:

- Prepare the response file, which emulates a user.
- Invoke the device driver installer with command options to use the prepared response file.

### *Creating a Response File*

Create the installer response file by performing a device driver installation with a command line switch "-r". The response file is automatically named `setup.iss` and is saved in the \windows folder. If a specific directory is desired, the switch `-f1` is used.

As an example, to save a response file in the same directory as the installation executable of the Xtium-CXP PX8, the command line would be:

```
Xtium-CXP_PX8_1.00.00.0000 -r -f1".\setup.iss"
```

### *Running a Silent Mode Installation*

A device driver silent installation, whether done alone or within a larger software installation requires the device driver executable and the generated response file `setup.iss`.

Execute the device driver installer with the following command line:

```
Xtium-CXP_PX8_1.00.00.0000 -s -f1".\setup.iss"
```

Where the `-s` switch specifies the silent mode and the `-f1` switch specifies the location of the response file. In this example, the switch `-f1".\setup.iss"` specifies that the `setup.iss` file be in the same folder as the device driver installer.



**Note:** On Windows 7, 8, and 10, the Windows Security dialog box will appear unless one has already notified Windows to 'Always trust software from "Teledyne DALSA Inc."' during a previous installation of a driver.

## Silent Mode Uninstall

Similar to a silent installation, a response file must be prepared first as follows.

### *Creating a Response File*

The installer response file is created by performing a device driver un-installation with a command line switch "-r". The response file is automatically named `setup_uninstall.iss` which is saved in the \windows folder. If a specific directory is desired, the switch "-f1" is used.

As an example, to save a response file in the same directory as the installation executable of the Xtium-CXP PX8, the command line would be:

```
Xtium-CXP_PX8_1.00.00.0000 -r -f1".\setup_uninstall.iss"
```

### *Running a Silent Mode Uninstall*

Similar to the device driver silent mode installation, the un-installation requires the device driver executable and the generated response file `setup.iss`.

Execute the device driver installer with the following command line:

```
Xtium-CXP_PX8_1.00.00.0000 -s -f1".\setup_uninstall.iss"
```

Where the **-s** switch specifies the silent mode and the **-f1** switch specifies the location of the response file. In this example, the switch `-f1".\setup_uninstall.iss"` specifies that the `setup_uninstall.iss` file be in the same folder as the device driver installer.

## Silent Mode Installation Return Code

A silent mode installation creates a file "corinstall.ini" in the Windows directory. A section called [SetupResult] contains the 'status' of the installation. A value of **1** indicates that the installation has started and a value of **2** indicates that the installation has terminated.

A silent mode installation also creates a log file "setup.log" which by default is created in the same directory and with the same name (except for the extension) as the response file. The /f2 option enables you to specify an alternative log file location and file name, as in `Setup.exe /s /f2"C:\Setup.log"`.

The "setup.log" file contains three sections. The first section, [InstallShield Silent], identifies the version of InstallShield used in the silent installation. It also identifies the file as a log file. The second section, [Application], identifies the installed application name, version, and the company name. The third section, [ResponseResult], contains the 'ResultCode' indicating whether the silent installation succeeded. A value of **0** means the installation was successful.

## Installation Setup with CorAppLauncher.exe

The installation setup can be run with the CorAppLauncher.exe tool provided with the driver.

- Install the board driver and get CorAppLauncher.exe from the \bin directory of the installation.
- When running the installation, CorAppLauncher.exe will return only when the installation is finished.
- When run from within a batch file, obtain the installation exit code from the ERRORLEVEL value.
- The arguments to CorAppLauncher.exe are
  - l: Launch application
  - f: Application to launch. Specify a fully qualified path.

### **As an example:**

- `CorAppLauncher -l -f"c:\driver_install\Xtium-CXP_PX8_1.00.00.0000.exe"`
- `IF %ERRORLEVEL% NEQ 0 goto launch error`

**Note:** There is a 32-bit and 64-bit version of CorAppLauncher.exe. When installing the driver, only the version related to the OS is installed. However, the 32-bit version is usable on either 32-bit or 64-bit Windows.

## Custom Driver Installation Using *install.ini* File

Customize the driver installation by parameters defined in the file "install.ini".

By using this file, the user can:

- Select the user default configuration.
- Select different configurations for systems with multiple boards.
- Assign a standard Serial COM port to board.

### Creating the *install.ini* File

- Install the driver in the target computer. All Xtium-CXP PX8 boards required in the system must be installed.
- Configure each board's acquisition firmware using the Teledyne DALSA Device Manager tool (see Device Manager – Board Viewer).
- When each board setup is complete, using the Teledyne DALSA Device Manager tool, click on the **Save Config File** button. This will create the "install.ini" file.

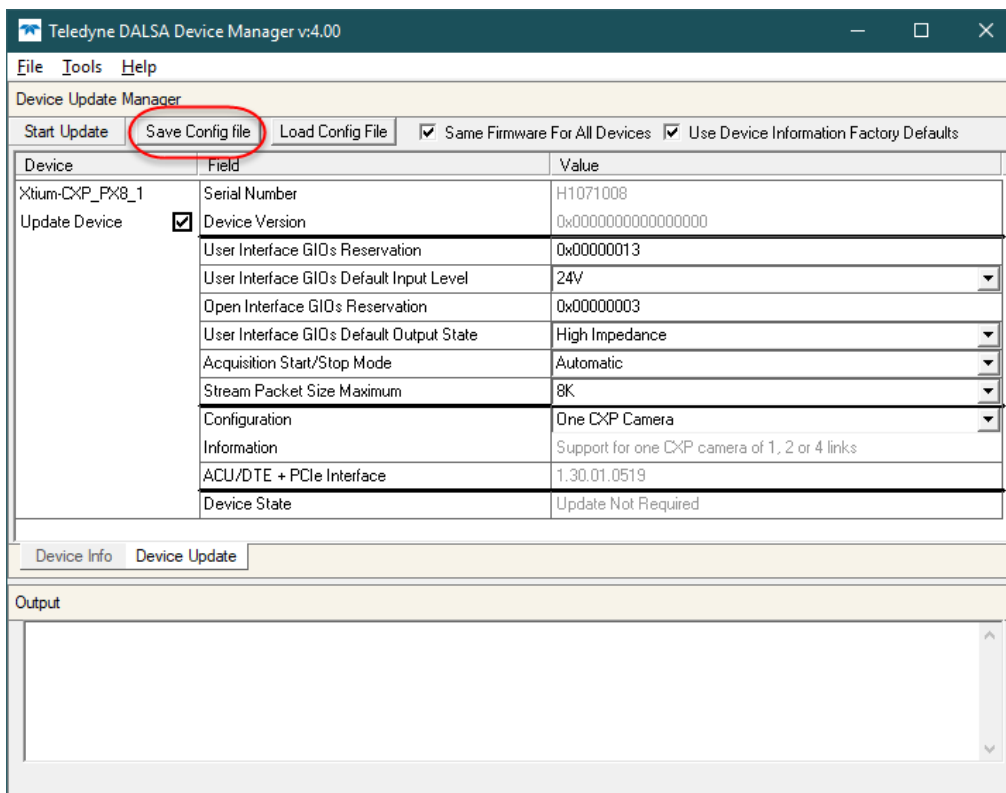


Figure 5: Create an *install.ini* File

### Run the Installation using *install.ini*

Copy the *install.ini* file into the same directory as the setup installation file. Run the setup installation as normal. The installation will automatically check for an *install.ini* file and if found, use the configuration defined in it.

In the Teledyne DALSA Device Manager start-up dialog the use of an *install.ini* is indicated in the INI Configuration column.

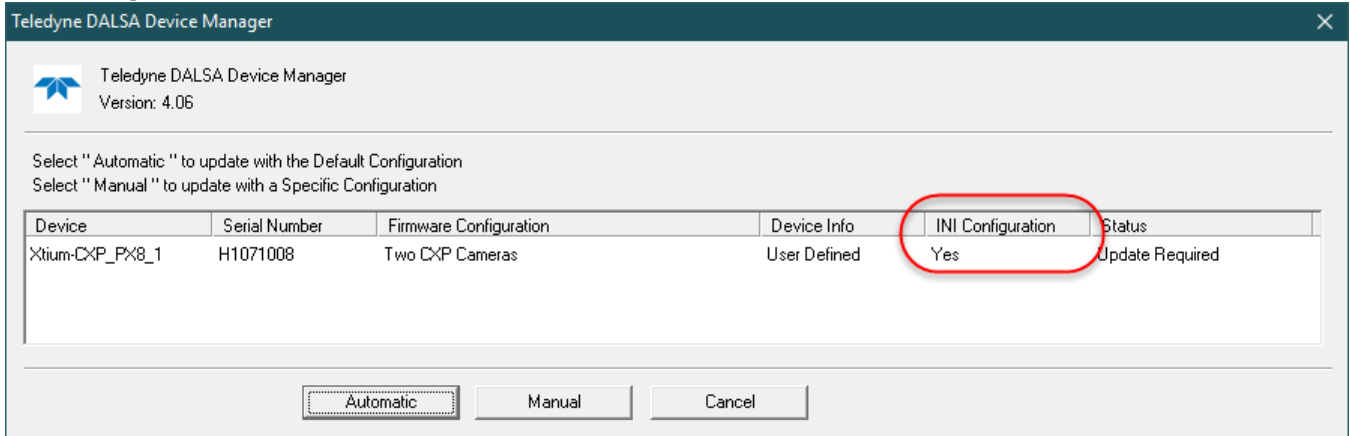


Figure 6: INI Configuration

---

## Upgrading Sapera or Board Driver

When installing a new version of Sapera or a Teledyne DALSA acquisition board driver in a computer with a previous installation, the current version **must** be un-installed first. Described below are two upgrade situations. Note that if the board is installed in a different slot, the new hardware wizard opens. Answer as instructed in the section Installation.

### Board Driver Upgrade Only

Minor upgrades to acquisition board drivers are distributed as ZIP files available in the Teledyne DALSA web site [www.teledynedalsa.com/mv/support](http://www.teledynedalsa.com/mv/support). Board driver revisions are also available on the next release of the Sapera Essential CD-ROM.

Often minor board driver upgrades do not require a new revision of Sapera. To confirm that the current Sapera version will work with the new board driver:

- Check the new board driver ReadMe file before installing, for information on the minimum Sapera version required.
- If the ReadMe file does not specify the Sapera version required, contact Teledyne DALSA Technical Support (see Technical Support).

#### To upgrade the board driver only:

- Logon the computer as an administrator or with an account that has administrator privileges.
- In **Windows 7**, from the start menu select **Start • Settings • Control Panel • Programs and Features**. Double-Click the Teledyne DALSA Xcelera board driver and click **Remove**.
- In **Windows 8 & Windows 10**, just type Control Panel while in the start screen, or click the arrow in the lower left side to bring up the all applications window. Select Programs and Features, then double-click the Teledyne DALSA Xcelera board driver and click **Remove**.
- Install the new board driver. Run **Setup.exe** if installing manually from a downloaded driver file.
- If the new driver is on a Sapera Essential CD-ROM follow the installation procedure described in Sapera LT Library & Xtium-CXP PX8 Driver Installation.



**Important:** You cannot install a Teledyne DALSA board driver without Sapera LT installed on the computer.

### Upgrading both Sapera and Board Driver

When upgrading both Sapera and the acquisition board driver, follow the procedure described below.

- Logon the computer as an administrator or with an account that has administrator privileges.
- In **Windows 7**, from the start menu select **Start • Settings • Control Panel • Programs and Features**. Double-click the Teledyne DALSA Xcelera board driver and click **Remove**. Follow by also removing the older version of Sapera LT.
- In **Windows 8 & Windows 10**, just type Control Panel while in the start screen, or click the arrow in the lower left side to bring up the all applications window. Select Programs and Features, then double-click the Teledyne DALSA Xcelera board driver and click **Remove**. Follow by also removing the older version of Sapera LT.
- Reboot the computer and logon the computer as an administrator again.
- Install the new versions of Sapera and the board driver as if this was a first time installation. See Sapera LT Library & Xtium-CXP PX8 Driver Installation for installation procedures.

## Preserving Board Parameters During Driver Upgrade

User defined parameter settings for previously installed boards can be preserved when upgrading a device driver by using an *install.ini* file as described in the Custom Driver Installation Using *install.ini* File section. Clicking **Automatic** on the Device Manager start-up dialog will apply the settings specified in the *install.ini* file.

To verify the settings specified in the *install.ini* file, click **Manual**; differences between the current device settings are shown in green in both the Device Info and Device Update tabs.

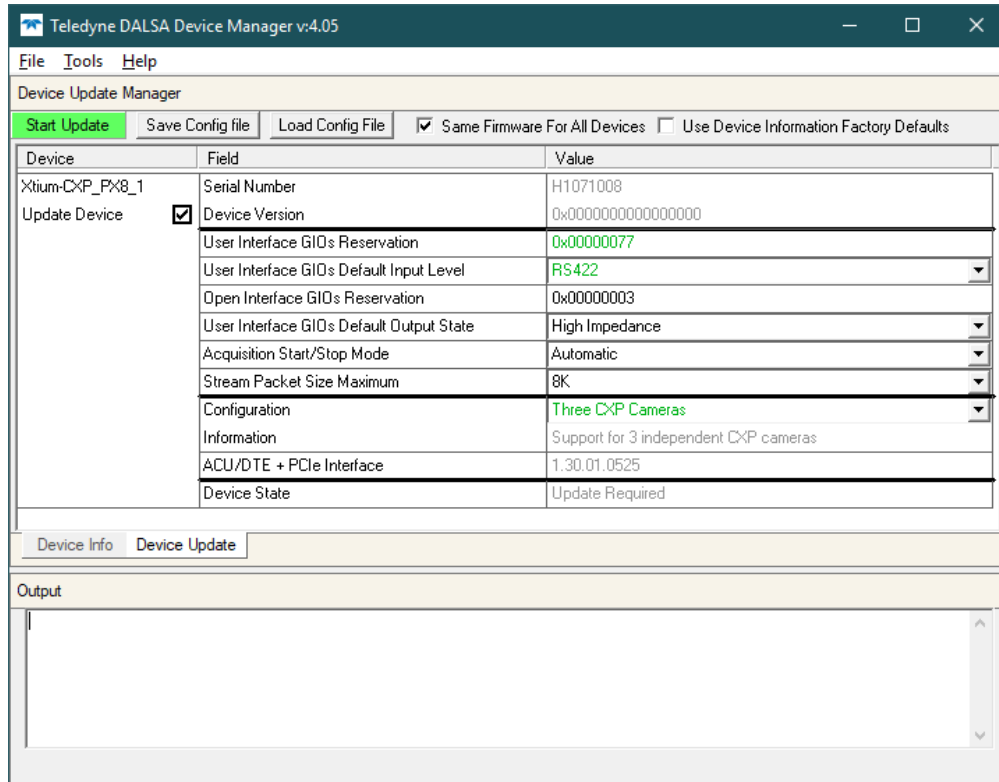


Figure 7: Device Manager Parameter Setting Differences

Upgrading without an *install.ini* file requires selecting **Manual** update on the Device Manager start-up dialog and setting the required parameters manually.



**Note:** Without an *install.ini*, configuration information is not preserved and is always set to factory default (for example, in this case One CXP camera).

# Preserving Board Parameters during Board Replacement or System Cloning

When replacing a board in a system or cloning a system configuration using a harddrive image, if the previous device parameter settings differ from the factory default driver settings it is indicated as "User Defined" or "Manual Configuration" in the Teledyne DALSA Device Manager start-up dialog under the Device Info column. User-defined settings are specific to the PCI Express slot on the system.

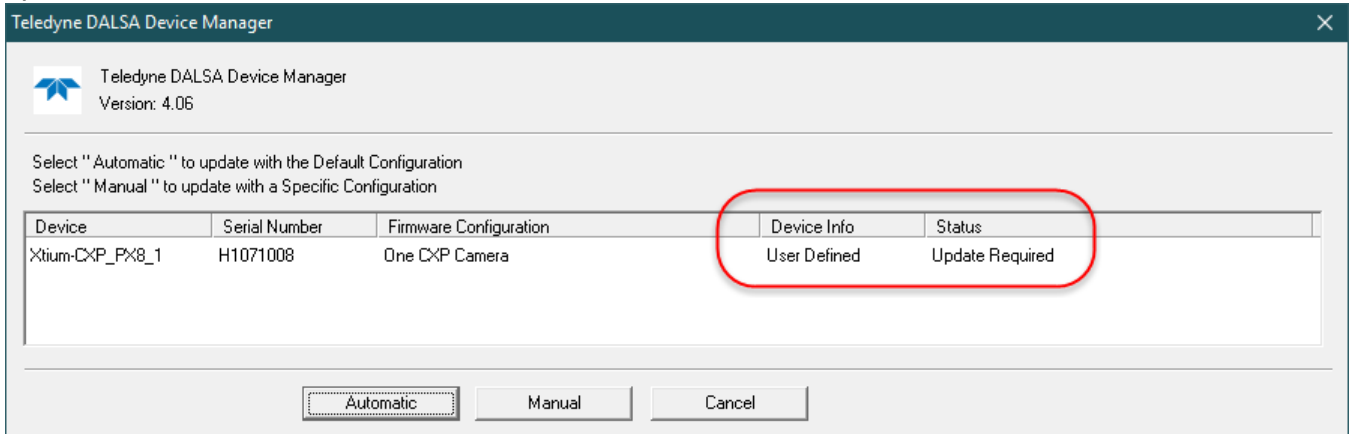


Figure 8: Firmware Update Status

To preserve the user defined parameter settings, select "Manual" and proceed with the update; differences between the current settings are shown in green in both the Device Info and Device Update tabs.

For systems with multiple boards, if boards use different firmware configurations (for example, One CXP camera and Two CXP cameras), disable the **Same Firmware For All Devices** option (otherwise the configuration specified for the first board according to slot position is applied to all boards in the system).

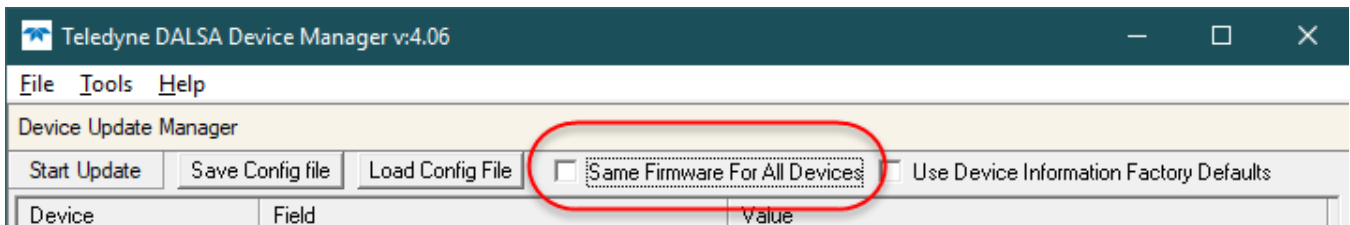
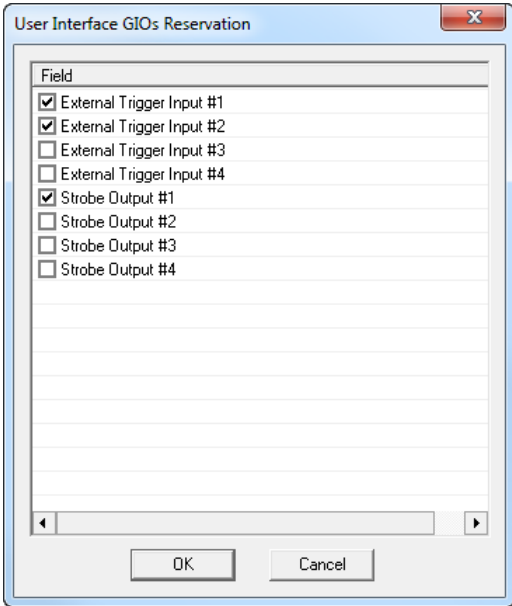


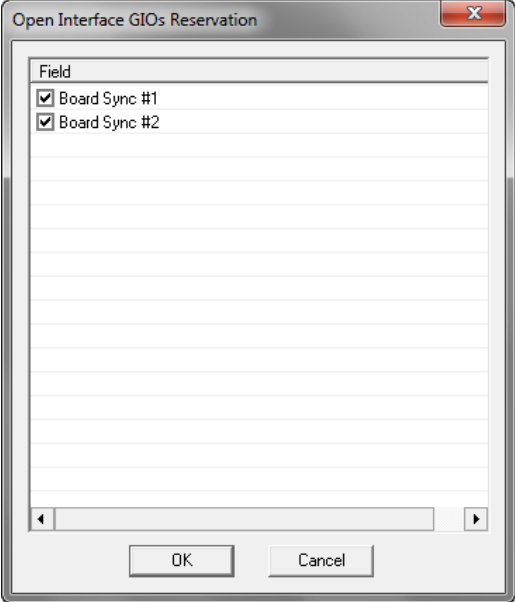
Figure 9: Same Firmware For All Devices Checkbox

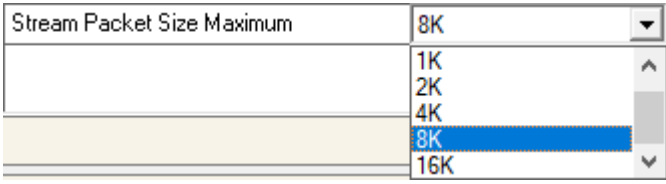




## Information Field Description

| Field                                   | Description   |
|---|---|
| Serial Number                           | [Read-Only]: Serial Number of the board   |
| Hardware ID                             | [Read-Only]: This field identifies future hardware changes affecting the operation of the board. Currently there are no such changes.   |
| Hardware Configuration                  | [Read-Only]: This field states the presence or absence of optional components. Currently there are no optional components available.  |
| Video Lanes                             | [Read-Only]: Indicates the maximum number of video lanes supported by the board. For this board, the value is 4.  |
| User Interface Outputs                  | [Read-Only]: Number of available user interface outputs on the board. For this board, the value is 8.   |
| P/N                                     | [Read-Only]: Indicates the part number of the board.  |
| P/N Revision                            | [Read-Only]: Indicates the revision of the part number.   |
| User Data                               | [Read/Write]: This is a 64 byte general purpose user storage area. For information on how to read/write this field at the application level, contact Teledyne DALSA Technical Support.  |
| User Interface GIOs Reservation         | <p>[Read/Write]: Use this field to reserve User Interface GIOs for use by the acquisition module. By default, boards are shipped with User Interface General Inputs 1 &amp; 2 reserved for External Triggers and User Interface General Output 1 reserved for Strobe Output.</p> <p>Click on the 'Value' field to open the dialog box show below. Disable any GIO reservations that are not required. Click the OK button to update the value field.</p>  |
| User Interface GIOs Default Input Level | <p>[Read/Write]: Use this field to select the default input level of the User Interface GIOs. By default, boards are shipped with inputs set for 24V signaling. Note that the input level can also be modified at the application level.</p> <p>Click on the 'Value' field to open the drop selection box show below. Select the input signal level detection required.</p>   |

|   |  |  |                |                                 |                |  |        |                             |      |  |       |
|---|--|--|----------------|---------------------------------|----------------|--|--------|-----------------------------|------|--|-------|
|   | <table border="1"> <tr> <td>User Interface GIOs Default Input Level</td> <td>24V</td> </tr> <tr> <td>Open Interface GIOs Reservation</td> <td>TTL</td> </tr> <tr> <td>User Interface GIOs Default Output State</td> <td>12V</td> </tr> <tr> <td>Acquisition Start/Stop Mode</td> <td>24V</td> </tr> <tr> <td></td> <td>RS422</td> </tr> </table>   | User Interface GIOs Default Input Level  | 24V            | Open Interface GIOs Reservation | TTL            | User Interface GIOs Default Output State | 12V    | Acquisition Start/Stop Mode | 24V  |  | RS422 |
| User Interface GIOs Default Input Level         | 24V  |  |                |                                 |                |  |        |                             |      |  |       |
| Open Interface GIOs Reservation                 | TTL  |  |                |                                 |                |  |        |                             |      |  |       |
| User Interface GIOs Default Output State        | 12V  |  |                |                                 |                |  |        |                             |      |  |       |
| Acquisition Start/Stop Mode                     | 24V  |  |                |                                 |                |  |        |                             |      |  |       |
|   | RS422  |  |                |                                 |                |  |        |                             |      |  |       |
| <p>Open Interface GIOs Reservation</p>          | <p>[Read/Write]: Use this field to reserve Open Interface GIOs for use by the acquisition module.</p> <p>To specify the open interface GIO reservations, click on the 'Value' field. Disable any GIO reservations that are not required. Click OK to update the value field.</p>  <p>By default, boards are shipped with Open Interface GIOs 1 &amp; 2 reserved for Board Sync 1 &amp;</p>  |  |                |                                 |                |  |        |                             |      |  |       |
| <p>User Interface GIOs Default Output State</p> | <p>[Read/Write]: Use this field to select the default Output State of the User Interface GIOs. Click on the 'Value' field to select the input signal level detection required.</p> <table border="1"> <tr> <td>User Interface GIOs Default Output State</td> <td>High Impedance</td> </tr> <tr> <td>Acquisition Start/Stop Mode</td> <td>High Impedance</td> </tr> <tr> <td>Stream Packet Size Maximum</td> <td>Low</td> </tr> <tr> <td></td> <td>High</td> </tr> </table> <p>By default, boards are shipped with User Interface General Outputs set to High Impedance.</p> <p>Note that the output state can also be modified at the application level.</p> | User Interface GIOs Default Output State | High Impedance | Acquisition Start/Stop Mode     | High Impedance | Stream Packet Size Maximum               | Low    |                             | High |  |       |
| User Interface GIOs Default Output State        | High Impedance   |  |                |                                 |                |  |        |                             |      |  |       |
| Acquisition Start/Stop Mode                     | High Impedance   |  |                |                                 |                |  |        |                             |      |  |       |
| Stream Packet Size Maximum                      | Low  |  |                |                                 |                |  |        |                             |      |  |       |
|   | High   |  |                |                                 |                |  |        |                             |      |  |       |
| <p>Acquisition Start/Stop Mode</p>              | <p>[Read/Write]: Use this field to indicate if frame grabber driver will automatically call the AcquisitionStart/AcquisitionStop camera feature upon connecting/disconnecting the transfer respectively.</p> <p>Click on the 'Value' field to open the dialog box show below.</p> <table border="1"> <tr> <td>Acquisition Start/Stop Mode</td> <td>Automatic</td> </tr> <tr> <td>Stream Packet Size Maximum</td> <td>Automatic</td> </tr> <tr> <td></td> <td>Manual</td> </tr> </table> <p>By default, boards are shipped with this option set to 'Automatic'.</p>   | Acquisition Start/Stop Mode              | Automatic      | Stream Packet Size Maximum      | Automatic      |  | Manual |                             |      |  |       |
| Acquisition Start/Stop Mode                     | Automatic  |  |                |                                 |                |  |        |                             |      |  |       |
| Stream Packet Size Maximum                      | Automatic  |  |                |                                 |                |  |        |                             |      |  |       |
|   | Manual   |  |                |                                 |                |  |        |                             |      |  |       |

|                            |  |
|----------------------------|--|
| Stream Packet Size Maximum | <p>[Read/Write]: Use this field to indicate the maximum stream packet size the frame grabber will allow. A higher value will reduce the overhead of sending video data and can avoid overflow of data. Click on the 'Value' field to open the dialog box show below. By default, boards are shipped with this option set to '8K'.</p>  |
|----------------------------|--|

## Device Information Report

Teledyne DALSA Technical Support may request device information report to aid in troubleshooting installation or operational problems. Generate the Xtium-CL MX4 device manager report file (BoardInfo.txt) by clicking **File • Save Device Info**.

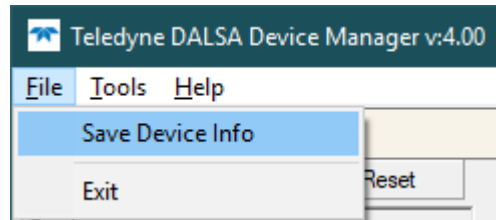


Figure 11: Device Manager File Menu Save Device Info Command

## Configuring Sopera

### Viewing Installed Sopera Servers

The Sopera configuration program (**Start • Programs • Teledyne DALSA • Sopera LT • Sopera Configuration**) allows the user to see all available Sopera servers for the installed Sopera-compatible boards. The **System** entry represents the system server. It corresponds to the host machine (your computer) and is the only server that should always be present.

### Increasing Contiguous Memory for Sopera Resources

The **Contiguous Memory** section lets the user specify the total amount of contiguous memory (a block of physical memory, occupying consecutive addresses) reserved for the resources needed for **Sopera buffers** allocation and **Sopera messaging**. For both items, the **Requested** value dialog box shows the 'CorMem' driver default memory setting while the **Allocated** value displays the amount of contiguous memory allocated successfully. The default values will generally satisfy the needs of most applications.

The **Sopera buffers** value determines the total amount of contiguous memory reserved at boot time for the allocation of dynamic resources used for frame buffer management such as scatter-gather list, DMA descriptor tables plus other kernel needs. Adjust this value higher if your application generates any out-of-memory error while allocating host frame buffers or when connecting the buffers via a transfer object. You can approximate the worst-case scenario amount of contiguous memory required as follows:

- Calculate the total amount of host memory used for one frame buffer  
[number of pixels per line • number of lines • (2 - if buffer is 10/12/14 or 16 bits)].
- Provide 200 bytes per frame buffer for Sopera buffer resources.

- Provide 64 bytes per frame buffer for metadata. Memory for this data is reserved in chunks of 64kB blocks.
- Provide 48 bytes per frame buffer for buffer management. Memory for this data is reserved in chunks of 64kB blocks.
- For each frame buffer DMA table, allocate 24 bytes + 8 bytes for each 4kB of buffer. For example, for a 120x50x8 image:  $120 \times 50 = 6000 = 1.46 \text{ 4kB blocks} \rightarrow \text{roundup to } 2 \text{ 4kB blocks}$ . Therefore  $24 \text{ bytes} + (2 * 8 \text{ bytes}) = 40 \text{ bytes}$  for DMA tables per frame buffer. Memory for this data is reserved in chunks of 64kB blocks. If vertical flipping is enabled, one must add 16 bytes per line per buffer. For example, for an image 4080x3072 image:  $16 \text{ bytes} * 3072 = 49152 \text{ bytes}$ .



Note 1: Sopera LT reserves the 1<sup>st</sup> 5MB for its own resources, which includes the 200 bytes per frame buffer mentioned above.

Note 2: Starting with SoperaLT 8.40, contiguous memory can be allocated anywhere in PC memory using the 'Buffer Allocation (64-bit)' entry in Sopera Configuration Tool. Driver will use this memory 1<sup>st</sup> for frame buffer DMA tables.

- Test for any memory error when allocating host buffers. Simply use the Buffer menu of the Sopera Grab demo program (see Grab Demo Overview) to allocate the number of host buffers required for your acquisition source. Feel free to test the maximum limit of host buffers possible on your host system – the Sopera Grab demo will not crash when the requested number of host frame buffers is not allocated.
- The following calculation is an example of the amount of contiguous memory to reserve beyond 5MB with 80,000 buffers of 2048x1024x8:
  - a)  $(80000 * 64 \text{ bytes})$
  - b)  $(80000 * 48 \text{ bytes})$
  - c)  $(80000 * (24 + (((2048 * 1024) / 4 \text{ kB}) * 8))) = 323 \text{ MB}$
  - d) Total = a (rounded up to nearest 64kB) + b (rounded up to nearest 64kB) + c (rounded up to nearest 64kB).

## Host Computer Frame Buffer Memory Limitations

When planning a Sopera application and its host frame buffers used, plus other Sopera memory resources, do not forget the Windows operating system memory needs.

A Sopera application using the preferred *scatter gather buffers* could consume most of the remaining system memory, with a large allocation of frame buffers. If using frame buffers allocated as a *single contiguous memory block*, Windows will limit the allocation dependent on the installed system memory. Use the Buffer menu of the Sopera Grab demo program to allocate host buffer memory until an error message signals the limit allowed by the operating system used.

### Contiguous Memory for Sopera Messaging

The current value for **Sopera messaging** determines the total amount of contiguous memory reserved at boot time for messages allocation. This memory space stores arguments when a Sopera function is called. Increase this value if you are using functions with large arguments, such as arrays and experience any memory errors.

# Troubleshooting Problems

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## Overview

The Xtium-CXP PX8 (and the Xtium family of products) is tested by Teledyne DALSA in a variety of computers. Although unlikely, installation problems may occur due to the constant changing nature of computer equipment and operating systems. This section describes what the user can verify to determine the problem or the checks to make before contacting Teledyne DALSA Technical Support.

If you require help and need to contact Teledyne DALSA Technical Support, make detailed notes on your installation and/or test results for our technical support to review. See Technical Support for contact information.

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## Problem Type Summary

Xtium-CXP PX8 problems are either installation types where the board hardware is not recognized on the PCIe bus (i.e. trained), or function errors due to camera connections or bandwidth issues. The following links jump to various topics in this troubleshooting section.

### First Step: Check the Status LED

Status LED D1 should be **BLUE** or flashing **BLUE** just after power up. If it remains flashing **RED**, the board firmware did not load correctly. Once the Windows driver is started, LED D1 should be **GREEN** or flashing **GREEN**. If LED D1 remains **BLUE** or flashing **BLUE**, the board is still running from the safe mode load. This could indicate that the normal load in the flash is corrupted or not present.

CXP Link status is indicated by LEDs (D3, D4, D5, and D6)– below the camera connector. The status colors displayed follow industry specifications for CoaXPress.

The complete status LED descriptions are available in the technical reference section, (see [Status LEDs Functional Descriptions](#)).

### Possible Installation Problems

- **Hardware PCI bus conflict:** When a new installation produces PCI bus error messages or the board driver does not install, it is important to verify that there are no conflicts with other PCI or system devices already installed. Use the Teledyne DALSA PCI Diagnostic tool as described in [Checking for PCI Bus Conflicts](#). Also verify the installation via the Windows Device Manager.
- **BSOD (blue screen) following a board reset:** After programming the board with different firmware, the computer displays the BSOD when the board is reset (see BSOD (blue screen) Following a Board Reset).
- **Verify Sopera and Board drivers:** If there are errors when running applications, confirm that all Sopera and board drivers are running. See Sopera and Hardware Windows Drivers for details. In addition, Teledyne DALSA technical support will ask for the log file of messages by Teledyne DALSA drivers. Follow the instructions describe in Teledyne DALSA Log Viewer.
- **Firmware update error:** There was an error during the Xtium-CXP PX8 firmware update procedure. The user can usually easily correct this. Follow the instructions Recovering from a Firmware Update Error.
- Installation went well but the board doesn't work or stopped working. Review these steps described in Symptoms: CamExpert Detects no Boards.

- **Using Windows 8/10 Fast Boot option:** When adding, removing, or moving boards while the PC is shutdown with the Windows Fast Boot option activated, it is possible that the boards don't get mapped properly on the next reboot of the computer. The driver will detect such a situation and the Device Manager launched at startup will display a message indicating that a reboot is required.

## Possible Functional Problems

- **Driver Information:** Use the Teledyne DALSA device manager program to view information about the installed Xtium-CXP PX8 board and driver. See Driver Information via the Device Manager Program.
- **On-Board Image Memory Requirements:** The Xtium-CXP PX8 on-board memory can provide two frame buffers large enough for most imaging situations. See On-board Image Memory Requirements for Acquisitions for details on the on board memory and possible limitations.

Sometimes the problem symptoms are not the result of an installation issue but due to other system issues. Review the sections described below for solutions to various Xtium-CXP PX8 functional problems.

- Symptoms: Xtium-CXP PX8 Does Not Grab
- Symptoms: Card grabs black
- Symptoms: Card acquisition bandwidth is less than expected

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## Troubleshooting Procedures

The following sections provide information and solutions to possible Xtium-CXP PX8 installation and functional problems. The previous section of this manual summarizes these topics.

### Diagnostic Tool Overview

The Xtium-CXP PX8 Board Diagnostic Tool provides a quick method to see board status and health. It additionally provides live monitoring of FPGA temperature and voltages, which may help in identifying problems.

#### *Diagnostic Tool Main Window*

The main window provides a comprehensive view of the installed Xtium board. Toolbar buttons execute the board self-test function and open a FPGA live status window.

Important parameters include the PCI Express bus transfer supported by the host computer and the internal Xtium FPGA temperature. The bus transfer defines the maximum data rate possible in the computer, while an excessive FPGA temperature may explain erratic acquisitions due to poor computer ventilation.



**Note:** The Lane Stats for each camera are aggregated into the lane # detected as master. However 8b/10b error statistics are compiled for each lane independently.

The screenshot shows the Diagnostic Tool interface with several callouts pointing to specific features and data sections:

- Generate Report**: Points to the 'yes!' button in the toolbar.
- Save Report**: Points to the save icon in the toolbar.
- Execute Self-Test**: Points to the self-test icon in the toolbar.
- Live FPGA Monitors**: Points to the FPGA icon in the toolbar.
- Computer Slot Identification**: Points to the PCIInfo section of the Frame Grabber Information table.
- FPGA Monitors**: Points to the FPGA Temperature section of the Frame Grabber Information table.
- Sapera & System Monitors**: Points to the System Resource and Sapera Memory sections.
- PCI Slot Type**: Points to the 'Gen 2' value in the PCIInfo section.
- Data Transfer Performance**: Points to the PCIe Bandwidth section.
- Right click to reset lane stats**: Points to the Lanes Stats table.

**Frame Grabber Information Table:**

| Field/Value           | Value                    | Min    | Max     |
|-----------------------|--------------------------|--------|---------|
| Driver Version        | 1.00.01.0124             |        |         |
| Serial Number         | H0757007                 |        |         |
| PCIInfo               | Bus #                    | 3      |         |
|                       | Slot #                   | 0      |         |
|                       | Function #               | 0      |         |
|                       | Bus Total Lanes          | 8      |         |
|                       | Bus Bit Transfer Rate    | Gen 2  |         |
|                       | Bus Payload Size (bytes) | 128    |         |
|                       | Bus Request Size (bytes) | 512    |         |
| PCIe Bandwidth (MB/s) | Achieved Bandwidth       | 3094   | 3086    |
|                       | Maximum Theoretical      | 3500   | 3095    |
| FPGA Temperature (°C) | Measured                 | 49.462 | 49.462  |
|                       | Operating Range          | 0.000  | 100.000 |
| Voltage Aux (V)       | Measured                 | 1.762  | 1.763   |
|                       | Operating Range          | 1.710  | 1.890   |
| Voltage Int (V)       | Measured                 | 0.998  | 0.998   |
|                       | Operating Range          | 0.970  | 1.030   |

**Lanes Stats Table:**

|        | CRC Error | Video MSG  | Packet Buffer Overflow | Packet Size Error | 8b/10b Error |
|--------|-----------|------------|------------------------|-------------------|--------------|
| Lane 1 | 13        | 3185038328 | 0                      | 0                 | 74053        |
| Lane 2 | 0         | 0          | 0                      | 0                 | 66328        |
| Lane 3 | 0         | 0          | 0                      | 0                 | 66311        |
| Lane 4 | 0         | 0          | 0                      | 0                 | 72373        |

**System Resource Table:**

|                 | Total (MB/KB)       | Free (MB/KB)        | Handles | Process | Thread |
|-----------------|---------------------|---------------------|---------|---------|--------|
| Physical Memory | 6135/ 6282360       | 2820/ 2888296       |         |         |        |
| Page File       | 12268/ 12562860     | 8604/ 8811052       |         |         |        |
| Virtual Memory  | 8388607/ 8589934464 | 8388382/ 8589703576 |         |         |        |
| Total           |                     |                     | 53109   | 131     | 2024   |

**Sapera Memory Table:**

|                | Free (KB/B)   | Used (KB/B) | Free Blocks | Largest Free Block (KB/B) | Used Blocks | Largest Used Block (KB/B) |
|----------------|---------------|-------------|-------------|---------------------------|-------------|---------------------------|
| Message Memory | 6143/ 6291452 | 0/ 4        | 2           | 6111/6258684              | 1           | 0/ 4                      |
| Buffer Memory  | 5111/ 5234168 | 8/ 8712     | 1           | 5111/5234168              | 12          | 2/ 2140                   |

Figure 12: Diagnostic Tool Main Window

## Diagnostic Tool Self-Test Window

Click the Start button to initiate the board memory self-test sequence. A healthy board will pass all memory test patterns.

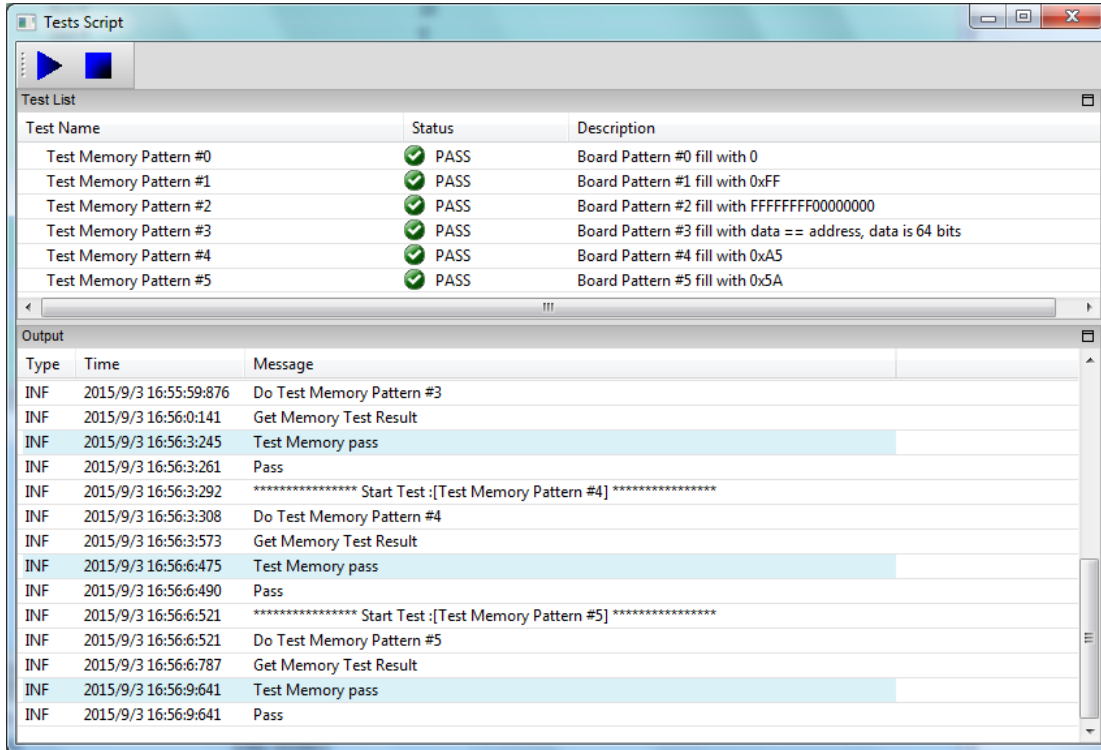


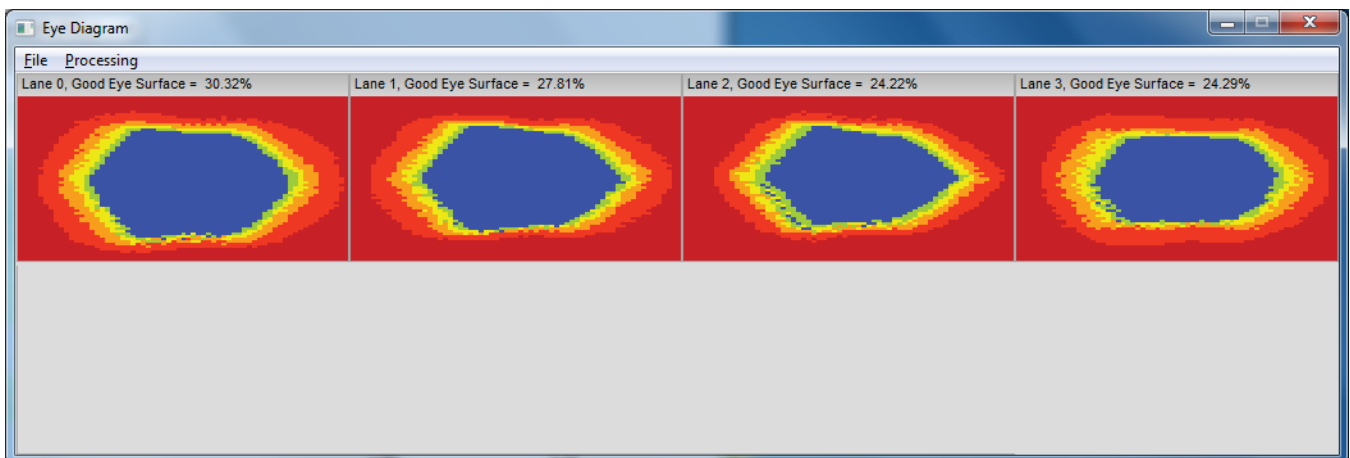
Figure 13: Diagnostic Tool Main Window

## Camera Input Eye Diagram Monitor

Eye Diagrams allow the user to visibly evaluate signal integrity between camera data lanes or between different cable sets. This tool does not provide specific measurements but will help to identify signal noise or jitter issues associated with bad cables or overly long cables.

The screen capture below shows a camera with 4 data lanes, where each digital signal is repetitively sampled and overlaid over itself, showing relative low-high transitions of the differential signal. The blue center area (eye surface) seems similar between each lane, typical for a good cable set.

The closure (collapse or horizontal shortening) of the eye surface would indicate problems such as poor signal to noise, high cable capacitance, multipath interference, among many possible digital transmission faults.





## Diagnostic Tool Live Monitoring Window

The three FPGA parameters listed on the main window can also be monitored in real time. Choosing a parameter puts that graph at the top where the user can select the time unit and time range. Clicking the Output button will open a window displaying any error messages associated with that parameter.



Figure 14: Diagnostic Tool Live Monitoring Window

## Checking for PCI Bus Conflicts

One of the first items to check when there is a problem with any PCI board is to examine the system PCI configuration and ensure that there are no conflicts with other PCI or system devices. The *PCI Diagnostic* program (**cpctdiag.exe**) allows examination of the PCI configuration registers and can save this information to a text file. Run the program via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • Sopera LT • Tools • PCI Diagnostics**.

As shown in the following screen image, use the first drop menu to select the PCI device to examine. Select the device from Teledyne DALSA. Note the bus and slot number of the installed board (this will be unique for each system unless systems are setup identically). Click on the **Diagnostic** button to view an analysis of the system PCI configuration space.

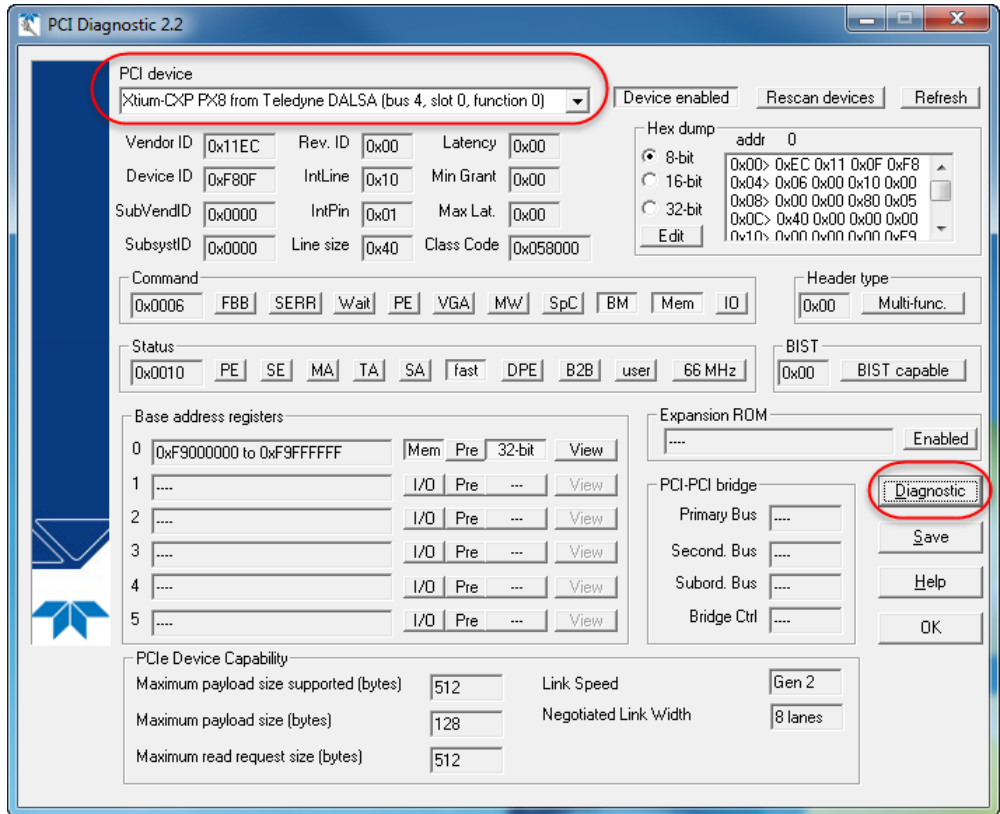


Figure 15: PCI Diagnostic Program

Clicking on the **Diagnostic** button opens a new window with the diagnostic report. From the PCI Bus Number drop menu, select the bus number that the Xtium-CXP PX8 is installed in—in this example the slot is bus 2.

The window now shows the I/O and memory ranges used by each device on the selected PCI bus. The information display box will detail any PCI conflicts. If there is a problem, click on the **Save** button. A file named `'pcidiag.txt'` is created (in the Sapera\bin directory) with a dump of the PCI configuration registers. Email this file when requested by the Teledyne DALSA Technical Support group along with a full description of your computer.

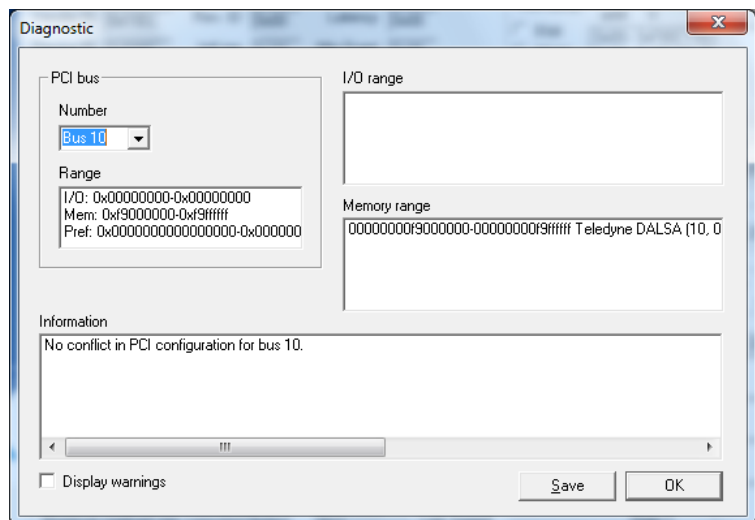


Figure 16: PCI Diagnostic Program – PCI bus info

## Windows Device Manager

An alternative method to confirm the installation of the Xtium-CXP PX8 board and driver is to use the Windows Device manager tool. Use the Start Menu shortcut **Start • Control Panel • System • Device Manager**. As shown in the following screen images, look for *Xtium-CXP PX8* board under "Imaging Devices". Double-click and look at the device status. You should see "This device is working properly." Go to "Resources" tab and make certain that the device has an interrupt assigned to it, without conflicts.

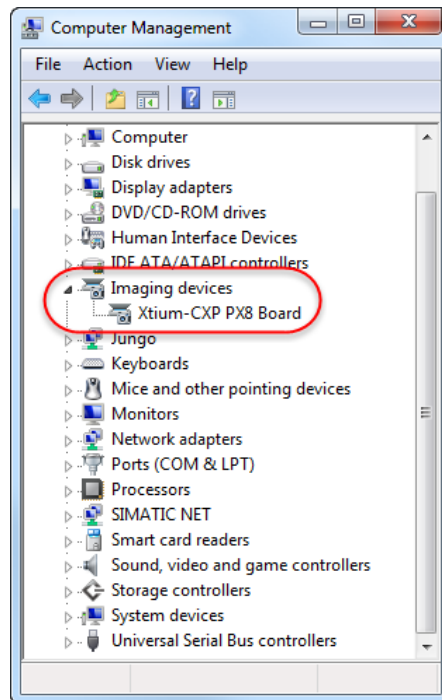


Figure 17: Using Windows Device Manager

## BSOD (blue screen) Following a Board Reset

There are cases where a PC will falsely report a hardware malfunction when the Xtium-CXP PX8 board is reset. Ensure that you are using Sapera LT 7.50 or later.

## Sapera and Hardware Windows Drivers

Any problem seen after installation, such as an error message running CamExpert, first make certain the appropriate Teledyne DALSA drivers have started successfully during the boot sequence. Example, click on the **Start • Programs • Accessories • System Tools • System Information • Software Environment** and click on **System Drivers**. Make certain the following drivers have started for the **Xtium-CXP PX8**.

Table 4: Xtium-CXP PX8 Device Drivers

| Device         | Description                | Type          | Started |
|----------------|----------------------------|---------------|---------|
| CorXtiumCXPPX8 | Xtium-CXP PX8 messaging    | Kernel Driver | Yes     |
| CorLog         | Sapera Log viewer          | Kernel Driver | Yes     |
| CorMem         | Sapera Memory manager      | Kernel Driver | Yes     |
| CorPci         | Sapera PCI configuration   | Kernel Driver | Yes     |
| CorSerial      | Sapera Serial Port manager | Kernel Driver | Yes     |

Teledyne DALSA Technical Support may request that you check the status of these drivers as part of the troubleshooting process.

## Recovering from a Firmware Update Error

This procedure is required if any failure occurred while updating the Xtium-CXP PX8 firmware on installation or during a manual firmware upgrade. If on the case the board has corrupted firmware, any Sapera application such as CamExpert or the grab demo program will not find an installed board to control.

Possible reasons for firmware loading errors or corruption are:

- Computer system mains power failure or deep brown-out
- PCI bus or checksum errors
- PCI bus timeout conditions due to other devices
- User forcing a partial firmware upload using an invalid firmware source file

When the Xtium-CXP PX8 firmware is corrupted, the board will automatically run from the Safe load after a PC reset.

**Solution:** Update the board using the standard method described in section Firmware Update: Automatic Mode.

## Driver Information via the Device Manager Program

The Device Manager program provides a convenient method of collecting information about the installed Xtium-CXP PX8. System information such as operating system, computer CPU, system memory, PCI configuration space, plus Xtium-CXP PX8 firmware information is displayed or written to a text file (default file name – BoardInfo.txt). Note that this program also manually uploads firmware to the Xtium-CXP PX8 (described elsewhere in this manual).

Execute the program via the Windows Start Menu shortcut

**Start • Programs • Teledyne DALSA • Xtium-CXP PX8 • Device Manager.**

If the Device Manager Program does not run, it will exit with a board was not found message. Possible reasons for an error are:

- Board is not in the computer
- Board driver did not start or was terminated
- PCI conflict after some other device was installed

### Information Window

The following figure shows the Device Manager Information screen. Click to highlight one of the board components and its information shows in the right hand window, as described below.

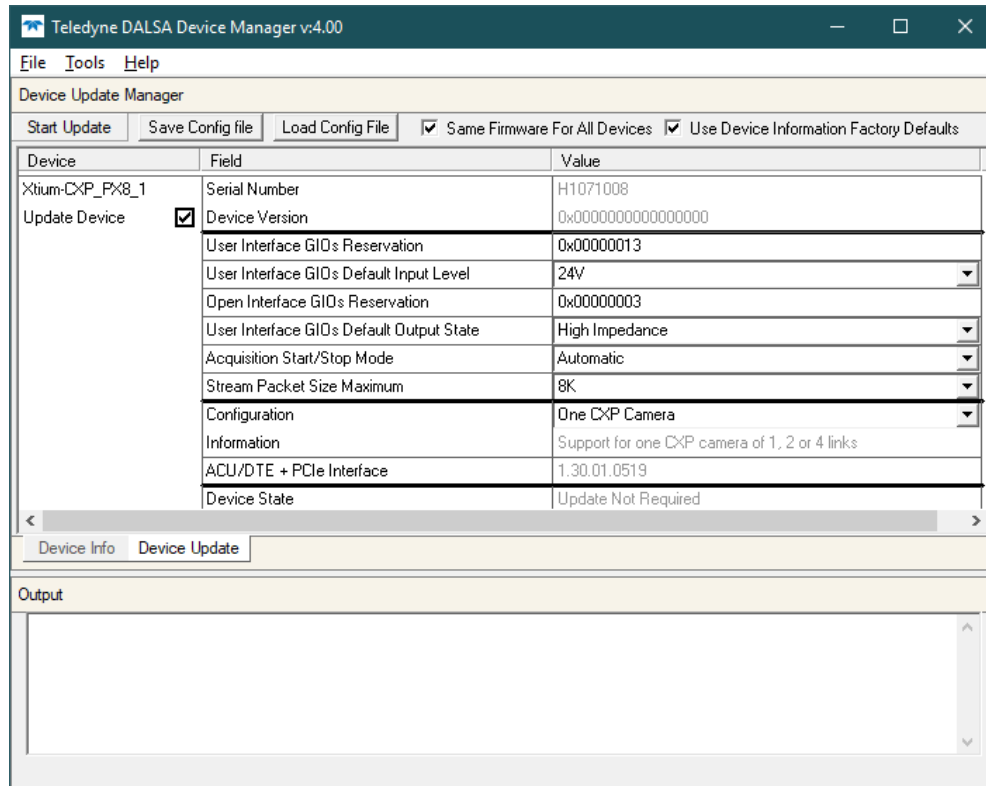


Figure 18: Board Firmware Version

- Select **Information** to display identification and information stored in the Xtium-CXP PX8 firmware.
- Select **Firmware** to display version information for the firmware components.
- Select one of the firmware components to load *custom* firmware when supplied by Teledyne DALSA engineering for a future feature.
- Click on **File • Save Device Info** to save all information to a text file. Email this file when requested by Technical Support.

## Teledyne DALSA Log Viewer

The third step in the verification process is to save in a text file the information collected by the Log Viewer program. Run the program via the Windows Start Menu shortcut

**Start • Programs • Teledyne DALSA • Spera LT • Tools • Log Viewer.**

The Log Viewer lists information about the installed Teledyne DALSA drivers. Click on File • Save and you will be prompted for a text file name to save the Log Viewer contents. Email this text file to Teledyne DALSA Technical Support when requested or as part of your initial contact email.

## On-board Image Memory Requirements for Acquisitions

The Xtium-CXP PX8 by default will allocate the maximum number of buffers that can fit in on-board memory based on the size of the acquired image before cropping, to a maximum of 65535 buffers.



**Note:** Applications can change the default number of on-board frame buffers using the Spera LT API.

Usually two buffers will ensure that the acquired video frame is complete and not corrupted in cases where the image transfer to host system memory may be interrupted and delayed by other host system processes. That is, there is no interruption to the image acquisition of one buffer by any delays in transfer of the other buffer (which contains the previously acquired video frame) to system memory.

If allocation for the requested number of buffers fails, the driver will reduce the number of on-board frame buffers requested until they can all fit. If there is not enough memory for 2 on-board buffers, the driver will reduce the size such that it allocates two partial buffers. This mode is dependent on reading out the image data to the host computer faster than the incoming acquisition.

The maximum number of buffers that can fit in on-board memory can be calculated as follows: (Total On-Board memory / (Buffer Size in Bytes + 256 Bytes used to store the DMA)).



**Note:** When using multi-camera configurations, the total on-board memory is divided evenly between the different inputs.

For example, assuming 1GB of on-board memory and acquiring 1024 x 1024 x 8 bit images, the number of on-board buffers would be:

$1024 \text{ MB} / [(1024 \times 1024) + 256] = 1023.75 \Rightarrow 1023 \text{ on-board buffers.}$

## Symptoms: CamExpert Detects no Boards

- When starting CamExpert, with no Teledyne DALSA board detected, CamExpert will start in offline mode. There is no error message and CamExpert is functional for creating or modifying a camera configuration file. If CamExpert should have detected an installed board frame grabber, troubleshoot the installation problem as described below.

### *Troubleshooting Procedure*

When CamExpert detects no installed Teledyne DALSA board, there could be a hardware problem, a system bus problem, a kernel driver problem, or a software installation problem.

- Make certain that the card is properly seated in PCIe slot.
- Perform all installation checks described in this section before contacting Technical Support.
- Try the board in a different PCIe slot if available.

## Symptoms: Xtium-CXP PX8 Does Not Grab

Sapera CamExpert does start but you do not see an image and the frame rate displayed is 0.

- Verify the camera has power.
- Verify the Camera CXP cable(s) is(are) connected to the camera.
- Verify the camera and timing parameters with the camera in free run mode.
- Verify you can grab with the camera in free run mode.
- Make certain that you provide an external trigger if the camera configuration file requires one. Use the software trigger feature of CamExpert if you do not have a trigger source.
- Make certain that the camera configuration is the required mode. This must match the camera configuration file. Refer to your camera datasheet.
- Try to snap one frame instead of continuous grab.
- Perform all installation checks described in this section before contacting Technical Support.

## Symptoms: Card grabs black

You are able to use Sapera CamExpert, the displayed frame rate is as expected, but the display is always black.

- Set your camera to manual exposure mode and set the exposure to a longer period, plus open the lens iris.
- Try to snap one frame instead of continuous grab.
- Make certain that the input LUT is not programmed to output all '0's.
- A PCIe transfer issue sometimes causes this problem. No PCIe transfer takes place, so the frame rate is above 0 but nevertheless no image is displayed in CamExpert.
- Make certain that BUS MASTER bit in the PCIe configuration space is activated. Look in PCI Diagnostics for **BM** button under "Command" group. Make certain that the **BM** button is activated.

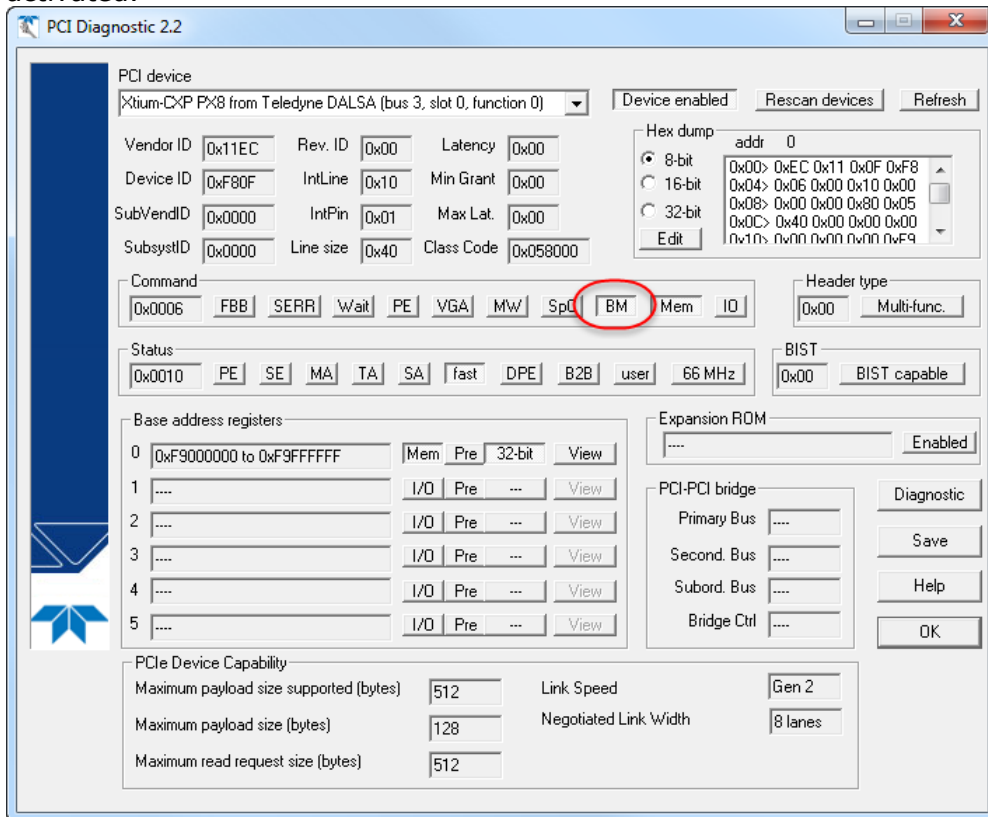


Figure 19: PCI Diagnostic Tool

- Perform all installation checks described in this section before contacting Technical Support.

## Symptoms: Card acquisition bandwidth is less than expected

The Xtium-CXP PX8 acquisition bandwidth is less than expected.

- Review the system for problems or conflicts with other expansion boards or drivers.
- Remove other PCI Express, PCI-32 or PCI-64 boards and check acquisition bandwidth again. Engineering has seen this case where other PCI boards in some systems cause limitations in transfers. Each system, with its combination of system motherboard and PCI boards, will be unique and must be tested for bandwidth limitations affecting the imaging application.
- Is the Xtium-CXP PX8 installed in a PCI Express x16 slot?  
Note that some computer's x16 slot may only support non x16 boards at x1 or not at all. Check the computer documentation or test an Xtium-CXP PX8 installation. The speed at which the board is running can be viewed using the Diagnostic Tool provided with the driver.
- Is the Xtium-CXP PX8 installed in a PCI Express Gen1 slot?  
Some older computers only have PCIe Gen1 slots. The Generation at which the board is running can be viewed using the [Diagnostic Tool](#) provided with the driver.
- Is the PCI maximum payload size smaller than 256 bytes?  
On some computers, this parameter can be changed in the PC's BIOS.

## Symptoms: PoCXP does not power the camera

If the Xtium-CXP PX8 does not power the camera, do the following:

- Ensure that a spare power supply connector from the PC power supply is connected to J12.
- If the camera is powered by means of multiple connectors, make sure all the necessary connections are made between the camera and the frame grabber.
- Ensure that Power-over-CXP (PoCXP) is enabled. CamExpert can be used to verify that the PoCXP parameter, available in the Basic Timing category, is set to Enable.

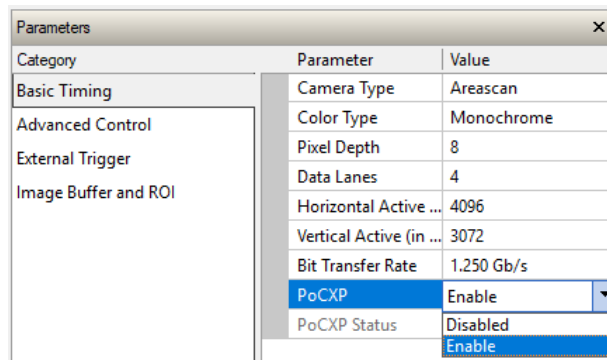


Figure 20: CamExpert PoCXP Parameter

- If PoCXP is enabled in CamExpert, check that the Video status PoCXP of the respective connection is green.

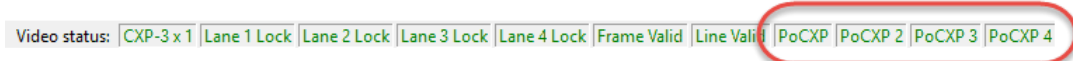


Figure 21: CamExpert Video Status Bar



## Over-current protection circuit is tripped

To identify this condition:

- Ensure a CXP camera is connected to the Xtium-CXP board.
- Use CamExpert and verify that the PoCXP is enabled.
- Verify the Video status PoCXP of the respective connection that requires power; a red status indicates a tripped state of the over-current protection circuit.

To confirm the tripped state, start SaperaLT Logviewer and search for a message similar to the following:

```
"ERR      2017/12/15 11:10:32:307      CorXtiumCXPPX8.SYS: smPoCXP[brd=0, poCxp=0]: 24V TRIP."
```

where:

*brd*: indicates the index of the CXP PX8 board in the system

*poCxp*: indicates the index of the CXP connector

### To clear the TRIP condition of the Xtium-CXP PX8 over-current circuit:

- Open the SaperaLT Logviewer and clear its contents.
- Start CamExpert and set PoCXP to Disable, then change the setting to Enable. This resets the over-current protection circuit for the current acquisition module. If necessary, perform this procedure for any other cameras in this condition connected to the board.
- If over-current condition occurs, the PoCXP Video status remains red and the LogViewer displays a message similar to the one above; verify that the CXP connectors attached to the cables are in good condition:

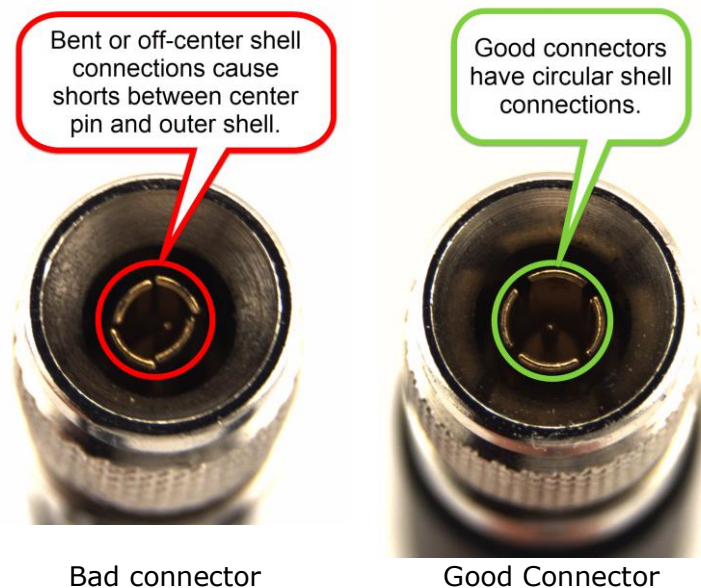


Figure 22: Bad vs. Good CXP Connectors

# CamExpert Quick Start

## Interfacing CXP Cameras with CamExpert

CamExpert is the camera-interfacing tool for Teledyne DALSA frame grabber boards supported by the Sopera library. CamExpert generates the Sopera camera configuration file (*yourcamera.ccf*) based on timing and control parameters entered. For backward compatibility with previous versions of Sopera, CamExpert also reads and writes the \*.cca and \*.cvi camera parameter files.

Every Sopera demo program starts with a dialog window to select a camera configuration file. Even when using the Xtium-CXP PX8 with common video signals, a camera file is required. Therefore, CamExpert is typically the first Sopera application run after an installation. Obviously existing .ccf files can be copied to any new board installations when similar cameras are used.

## CamExpert Example with a Monochrome Camera

The image below shows CamExpert controlling the Xtium-CXP PX8. In this example, the CXP camera has 4 data lanes connected.

After the camera is identified (as per the CXP device discovery protocol), the timing parameters are displayed and the user can test by clicking on *Grab*. Descriptions of the CamExpert sections follow the image.

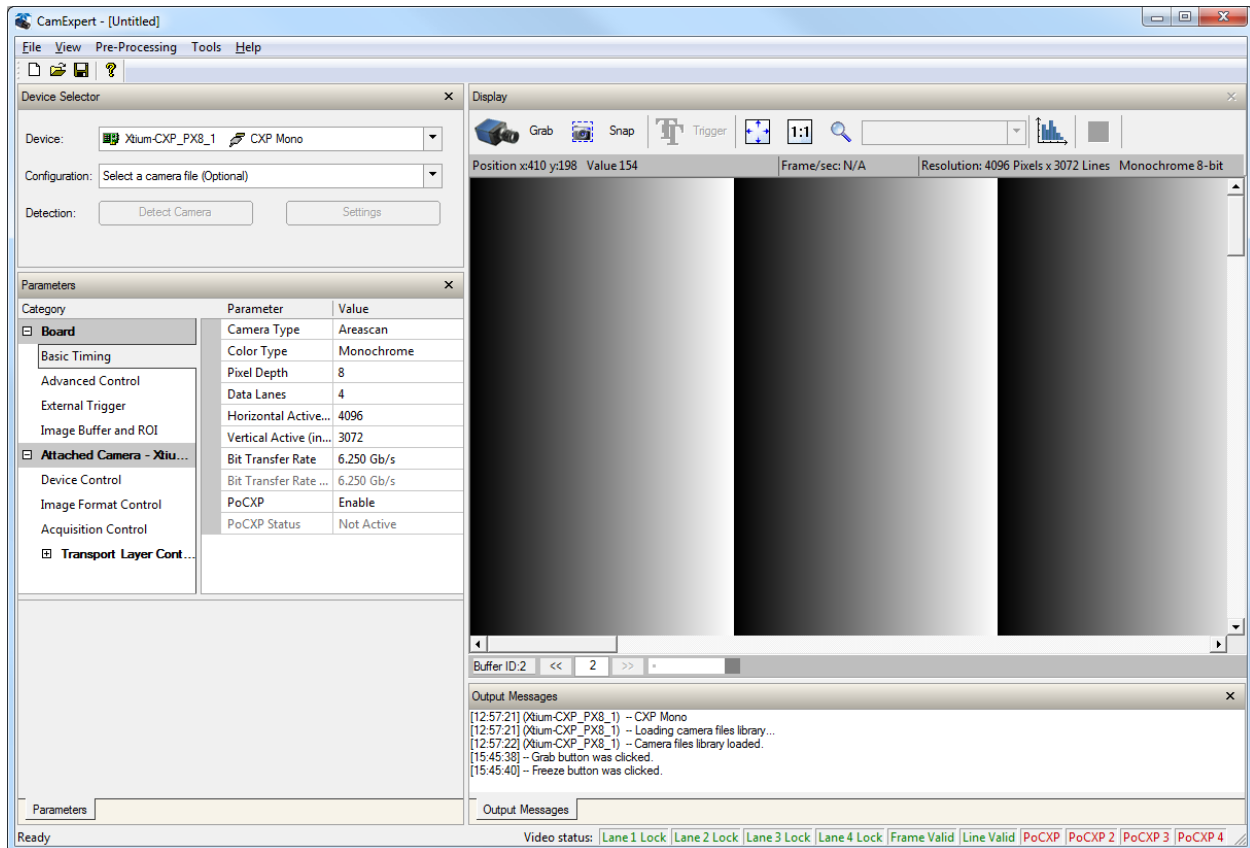


Figure 23: CamExpert Program

CamExpert groups camera features into functional categories. The features shown depend on the frame grabber used and what camera is connected. The values are either the camera defaults or the last stored value when the camera was used. The general descriptions below are not specific to a particular camera.

- **Device Selector:** Two drop menus allow selection of which device and which saved configuration to use.
- **Device:** Select which acquisition device to control and configure a camera file. Required in cases where there are multiple boards in a system and when one board supports multiple acquisition types. Note in this example, the installed Xtium-CXP PX8 has firmware to support a monochrome or color RGB CoaXPress camera.

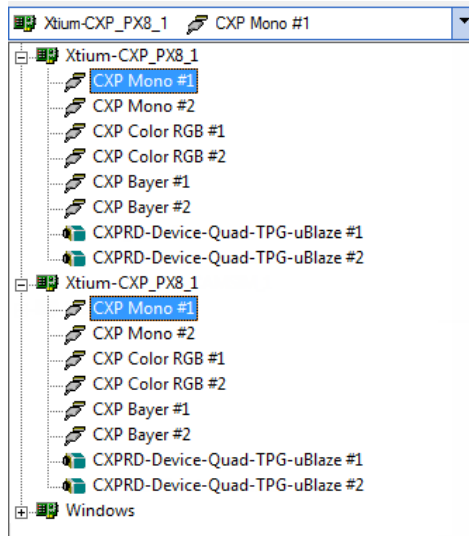


Figure 24: CamExpert Device Tree

- **Configuration:** Select the timing for a specific camera model included with the Sapera installation or a standard video standard. The *User's* subsection is where user created camera files are stored.
- **Parameter Groups:** Select a function category and change parameter values as required. Descriptions for the camera parameters change dependent on the camera.
  - **Basic Timing:** Provides or change static camera parameters.
  - **Advanced Controls:** Advanced parameters used to select various integration methods, frame trigger type, Camera CXP controls, etc.
  - **External Trigger:** Parameters to configure the external trigger characteristics.
  - **Image Buffer and ROI:** Allows control of the host buffer dimension and format.
- **Display:** An important component of CamExpert is its live acquisition display window, which allows immediate verification of timing or control parameters without the need to run a separate acquisition program. **Grab** starts continuous acquisition (button then toggles to **Freeze** to stop). **Snap** is a single frame grab. **Trigger** is a software trigger to emulate an external source.
- **Output Messages and Video Status Bar:** Events and errors are logged for review. Camera connection status is displayed where green indicates connected signals present.

The CamExpert tool is described more fully in the Sapera Getting started and Sapera Introduction manuals.

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# CamExpert Demonstration and Test Tools

The CamExpert utility also includes a number of demonstration features, which make CamExpert the primary tool to configure, test and calibrate your camera and imaging setup. Display tools include, image pixel value readout, image zoom, and line profiler.

Functional tools include support for either hardware based or software Bayer filter camera decoding with auto white balance calibration.

## Camera Types & Files

The Xtium-CXP PX8 supports digital area scan or line scan cameras using the Camera CXP interface standard.

### Camera Files Distributed with Sopera

The Sopera distribution includes camera files for a selection of Xtium-CXP PX8 supported cameras. Using the Sopera CamExpert program, you may use the camera files (CCA) provided to generate a camera configuration file (CCF) that describes the desired camera and frame grabber configuration.

Teledyne DALSA continually updates a camera application library composed of application information and prepared camera files. Camera files are ASCII text, readable with Windows Notepad on any computer without having Sopera installed.

## Overview of Sopera Acquisition Parameter Files (\*.ccf or \*.cca/\*.cvi)

### Concepts and Differences between the Parameter Files

There are two components to the legacy Sopera acquisition parameter file set: CCA files (also called cam-files) and CVI files (also called VIC files, i.e. video input conditioning). The files store video-signal parameters (CCA) and video conditioning parameters (CVI), which in turn simplifies programming the frame-grabber acquisition hardware for the camera in use. **Sopera LT 5.0** introduces a new camera configuration file (**CCF**) that combines the CCA and CVI files into one file.

Typically, a camera application will use a CCF file per camera operating mode (or one CCA file in conjunction with several CVI files, where each CVI file defines a specific camera-operating mode). An application can also have multiple CCA/CCF files to support different image format modes supported by the camera or sensor (such as image binning or variable ROI).

### CCF File Details

A file using the ".CCF" extension, (Camera Configuration files), is the camera (CCA) and frame grabber (CVI) parameters grouped into one file for easier configuration file management. This is the default Camera Configuration file used with Sopera LT 5.0 and the CamExpert utility.

### CCA File Details

Teledyne DALSA distributes camera files using the legacy ".CCA" extension, (CAMERA files), which contain all parameters describing the camera video signal characteristics and operation modes (what the camera outputs). The Sopera parameter groups within the file are:

- Video format and pixel definition
- Video resolution (pixel rate, pixels per line, lines per frame)
- Synchronization source and timing
- Channels/Taps configuration
- Supported camera modes and related parameters
- External signal assignment

## CVI File Details

Legacy files using the “.CVI” extension contain all operating parameters related to the frame grabber board - what the frame grabber can actually do with camera controls or incoming video. The Sapera parameter groups within the file are:

- Activate and set any supported camera control mode or control variable.
- Define the integration mode and duration.
- Define the strobe output control.
- Allocate the frame grabber transfer ROI, the host video buffer size and buffer type (RGB888, RGB101010, MONO8, and MONO16).
- Configuration of line/frame trigger parameters such as source (internal via the frame grabber /external via some outside event), electrical format (TTL, RS-422, OPTO-isolated), and signal active edge or level characterization.

## Saving a Camera File

Use CamExpert to save a camera file (\*.ccf ) usable with any Sapera demo program or user application. An example would be a camera file, which sets up parameters for a free running camera (i.e. internal trigger) with exposure settings for a good image with common lighting conditions.

When CamExpert is setup as required, click on **File•Save As** to save the new .ccf file. The dialog that opens allows adding details such as camera information, mode of operation, and a file name for the .ccf file.

## Camera Interfacing Check List

Before interfacing a camera from scratch with CamExpert:

- Confirm that Teledyne DALSA has not already published an application note with camera files [ [www.teledynedalsa.com](http://www.teledynedalsa.com) ].
- Confirm that the correct version or board revision of Xtium-CXP PX8 is used. Confirm that the required firmware is loaded into the Xtium-CXP PX8.
- Confirm that Sapera does not already have a .cca file for your camera installed on your hard disk. If there is a .cca file supplied with Sapera, then use CamExpert to generate the .ccf file with default parameter values matching the frame grabber capabilities.
- Check if the Sapera installation has a similar type of camera file. A similar .cca file can be loaded into CamExpert and modified to match timing and operating parameters for your camera, and lastly save them as Camera Configuration file (.ccf).
- Finally, if there is no file for your camera, run CamExpert after installing Sapera and the acquisition board driver, select the board acquisition server, and manually enter the camera parameters.

---

# Using the Flat Field Correction Tool

Flat Field Correction is the process of eliminating small gain differences between pixels in a sensor array. That sensor when exposed to a uniformly lit field will have no gray level differences between pixels when calibrated flat field correction is applied to the image. The CamExpert Flat Field tool functions with hardware supporting flat field processing.

## **Xtium-CXP PX8 Flat Field Support**

The Xtium-CXP PX8 supports hardware based real-time Flat Field Correction when used with a monochrome video source. The Xtium-CXP PX8 supports one method for pixel replacement:

- Neighborhood Replacement: a bad pixel is replaced with the average of its 2 neighbors on the same video line.
- Note that the CXP Flat Field algorithm handles all cases of bad pixels being on the frame edge or where neighboring pixels are also bad.

### ***Loading the Required Camera File***

Select the required camera configuration file for the connected camera. Verify the acquisition with the live grab function. Make camera adjustments to get good images.

## **Set up Dark and Bright Acquisitions with the Histogram Tool**

Before performing calibration, verify the acquisition with a live grab. Also at this time make preparations to grab a flat light gray level image, required for the calibration, such as a clean evenly lighted white wall or non-glossy paper with the lens slightly out of focus. Ideally a controlled diffused light source aimed directly at the lens should be used. Note the lens iris position for a bright but not saturated image. Additionally, check that the lens iris closes well or have a lens cover to grab the dark calibration image.

### ***Verify a Dark Acquisition***

Close the camera lens iris and cover the lens with a lens cap. Using CamExpert, click on the grab button and then the histogram button. The following figure shows a typical histogram for a very dark image (8-bit acquisition).

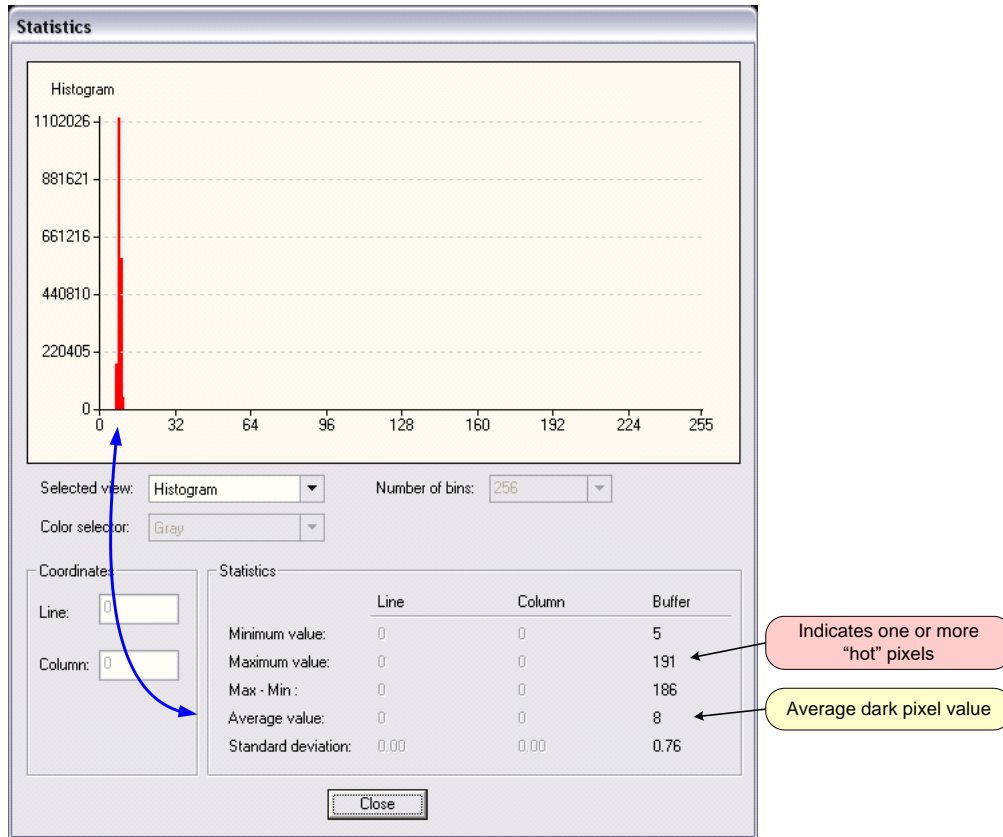


Figure 25: CamExpert Histogram of Dark Image

---

**Important:** In this example, the **average** pixel value for the frame is close to black. Also note that most sensors will show a much higher maximum pixel value due to one or more "hot pixels". The sensor specification accounts for a small number of hot or stuck pixels (pixels that do not react to light over the full dynamic range specified for that sensor).

---

### Verify a Bright Acquisition

Aim the camera at a diffused light source or evenly lit white wall with no shadows falling on it. Using CamExpert, click on the grab button and then the histogram button. Use the lens iris to adjust for a bright gray approximately around a pixel value of 200 (for 8-bit pixels). The following figure shows a typical histogram for a bright gray image.

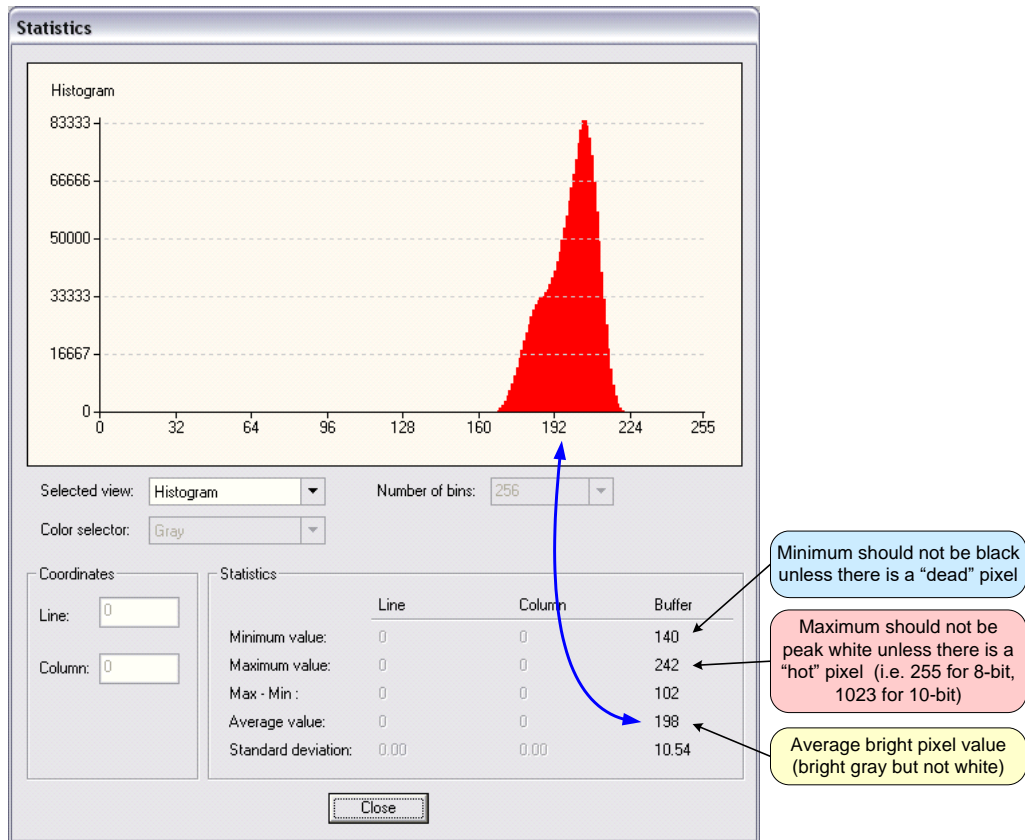


Figure 26: CamExpert Histogram of Bright Image

**Important:** In this example, the **average** pixel value for the frame is bright gray. Also note that sensors may show a much higher maximum or a much lower minimum pixel value due to one or more "hot or dead pixels". The sensor specification accounts for a small number of hot, stuck, or dead pixels (pixels that do not react to light over the full dynamic range specified for that sensor).

Once the bright gray acquisition setup is done, note the camera position and lens iris position so as to be able to repeat it during the calibration procedure.

## Flat Field Correction Calibration Procedure

Calibration is the process of taking two reference images, one of a black field – one of a light gray field (not saturated), to generate correction data for images captured by the CCD. Each CCD pixel data is modified by the correction factor generated by the calibration process, so that each pixel now has an identical response to the same illumination.

Start the Flat Field calibration tool via the CamExpert menu bar:

**Tools • Flat Field Correction • Calibration.**

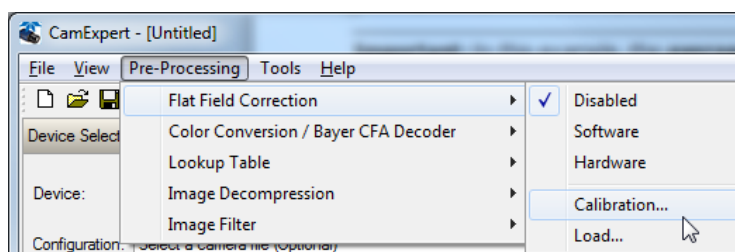


Figure 27: CamExpert Flat Field Correction Menu Command



## Flat Field Correction Dialog

The Flat Field Correction dialog provides a three step process to acquire two reference images and then save the flat field correction data for the camera used. To aid in determining if the reference images are valid, a histogram tool is provided so that the user can review the images used for the correction data.

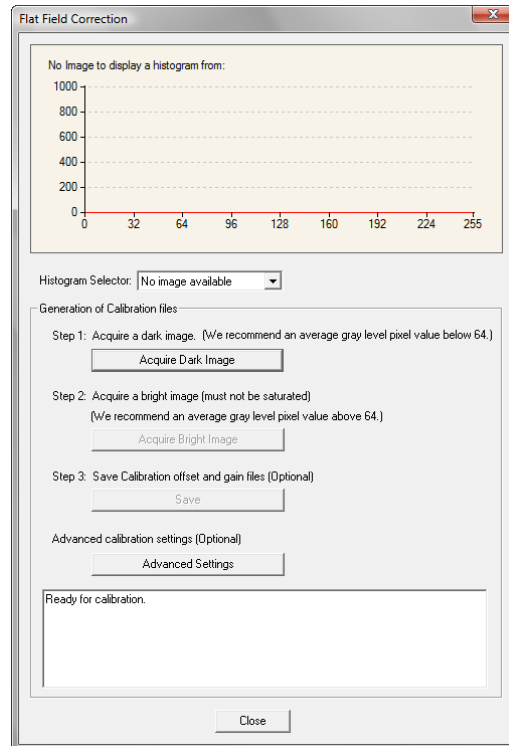


Figure 28: CamExpert Flat Field Correction Dialog

- Setup the camera to capture a uniform black image. Black paper with no illumination and the camera lens' iris closed to minimum can provide such a black image.
- Click on **Acquire Black Image**. The flat field demo will grab a video frame, analyze the pixel gray level spread, and present the statistics. The desired black reference image should have pixel values less than 20. If acceptable accept the image as the black reference.
- Setup the camera to acquire a uniform white image (but not saturated white). Even illumination on white paper can be used, with a minimum gray level of 128. It is preferable to prepare for the white level calibration before the calibration procedure.
- Click on **Acquire White Image**. The flat field demo will grab a video frame, analyze the pixel gray level spread, and present the statistics. The captured gray level for all pixels should be greater than 128. If acceptable accept the image as the white reference.
- Click on **Save**. The flat field correction data is saved as a TIF image with a file name of your choice (such as camera name and serial number).

## Using Flat Field Correction

From the CamExpert menu bar enable Flat Field correction (**Tools • Flat Field Correction • Enable**). Now when doing a live grab or snap, the incoming image is corrected by the current flat field calibration data for each pixel.

Use the menu function **Tools • Flat Field Correction • Load** to load in a flat field correction image from a previous saved calibration data. CamExpert allows saving and loading calibration data for all cameras used with the imaging system.

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## Using the Bayer Filter Tool

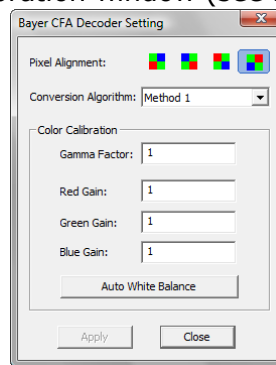
CamExpert supports the use of Bayer Filter cameras by providing a tool to select the Bayer filter mosaic pattern and to perform an auto white balance. Color calibration can then be manually fine-tuned with RGB gain and gamma adjustments.

The CamExpert Bayer filter tool supports using both software or hardware based decoding. With boards that have Bayer filter decoding in hardware, CamExpert directly controls the hardware for high performance real-time acquisitions from Bayer filter cameras. When standard acquisition boards are used, CamExpert performs software Bayer filter decoding using the host system processor.

### Bayer Filter White Balance Calibration Procedure

The following procedure uses the hardware Bayer filter support (Bayer Decoder firmware loaded) and any supported Bayer color camera. It is assumed that CamExpert was used to generate a camera file with correct camera timing parameters.

- On the CamExpert menu bar, click on **Tools • Bayer Filter**. The following menu should show **Hardware** selected by default when the frame grabber has Bayer support.
- Select **Setting** to access the color calibration window (see following figure).



- Click **Grab** to start live acquisition.
- Aim and focus the camera. The camera should see an area of white or place white paper in front of the object being imaged.
- Click on one of the four Bayer pixel alignment patterns to match the camera (best color before calibration). Typically, the CamExpert default is correct for a majority of cameras.
- Adjust the lens iris to reduce the exposure brightness so that the white image area is now darker. Make certain that no pixel in the white area is saturated.
- Using the mouse left button, click and drag a ROI enclosing a portion of the white area.
- Click on the **Auto White Balance** button. CamExpert will make RGB gain adjustments.
- Open the camera iris to have a correctly exposed image.
- Review the image for color balance.
- Manually make additional adjustments to the RGB gain values. Fine tune the color balance to achieve best results. Adjust the gamma factor to optionally improve the display.
- Stop the live acquisition and save the camera file (which now contains the Bayer RGB calibration information). Note that the gamma factor is not save because it is not a Samera parameter but only a display tool.

### Using the Bayer Filter

A Samera application, when loading the camera file parameters, will have the RGB gain adjustment values. The application can incorporate a calibration menu for RGB adjustments as required.

# Sapera Demo Applications

## Grab Demo Overview

The Grab Demo program demonstrates the basic acquisition functions included in the Sapera library. The program either allows you to acquire images, in continuous or in one-time mode, while adjusting the acquisition parameters. The program code may be extracted for use within your own application.

The Grab Demo is available as a compiled binary; source code is provided for both C++ and .NET projects using Visual Studio 2010/2012/2013/2015/2017.

All demos are available through the Start menu.

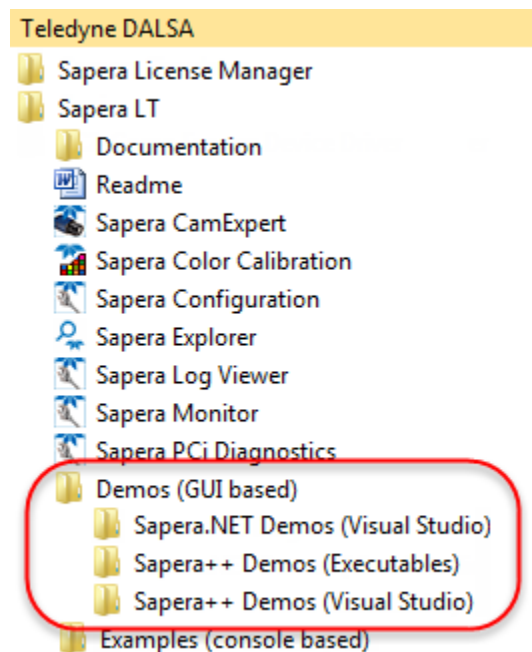


Table 5: Grab Demo Workspace Details

|                             |   |
|-----------------------------|---|
| <b>Program file</b>         | ... \... \Sapera \Demos \Binaries \GrabDemo.exe   |
| <b>Visual C++ Solution</b>  | ... \... \Sapera \Demos \Classes \Vc \SapDemos_2010.sln<br>... \... \Sapera \Demos \Classes \Vc \SapDemos_2012.sln<br>... \... \Sapera \Demos \Classes \Vc \SapDemos_2013.sln<br>... \... \Sapera \Demos \Classes \Vc \SapDemos_2015.sln<br>... \... \Sapera \Demos \Classes \Vc \SapDemos_2017.sln |
| <b>Visual .NET Solution</b> | ... \... \Sapera \Demos \NET \SapDemos_2010.sln<br>... \... \Sapera \Demos \NET \SapDemos_2012.sln<br>... \... \Sapera \Demos \NET \SapDemos_2013.sln<br>... \... \Sapera \Demos \NET \SapDemos_2015.sln<br>... \... \Sapera \Demos \NET \SapDemos_2017.sln   |
| <b>Remarks</b>              | This demo is based on Sapera LT classes. See the Sapera User's and Reference manuals for more information.  |

## Using the Grab Demo

### Server Selection

Run the grab demo from the start menu:

**Start•Programs•Sapera LT•Demos (GUI based)•Sapera++ Demos•GrabDemo.exe**

The demo program first displays the acquisition configuration menu. The first drop menu displayed permits selecting from any installed Sapera acquisition servers (installed Teledyne DALSA acquisition hardware using Sapera drivers). The second drop menu permits selecting from the available input devices present on the selected server.

### CCF File Selection

Use the acquisition configuration menu to select the required camera configuration file for the connected camera. Sapera camera files contain timing parameters and video conditioning parameters. The default folder for camera configuration files is the same used by the CamExpert utility to save user generated or modified camera files.

Use the Sapera CamExpert utility program to generate the camera configuration file based on timing and control parameters entered. The CamExpert live acquisition window allows immediate verification of those parameters. CamExpert reads both Sapera \*.cca and \*.cvi for backward compatibility with the original Sapera camera files.

### Grab Demo Main Window

The Grab Demo program provides basic acquisition control for the selected frame grabber. The loaded camera file (.ccf) defines the Frame buffer defaults.

Refer to the Sapera LT User's Manual (OC-SAPM-USER), in section "Demos and Examples – Acquiring with Grab Demo", for more information on the Grab Demo and others provided with Sapera LT.

# Xtium-CXP PX8 Reference

## Block Diagram

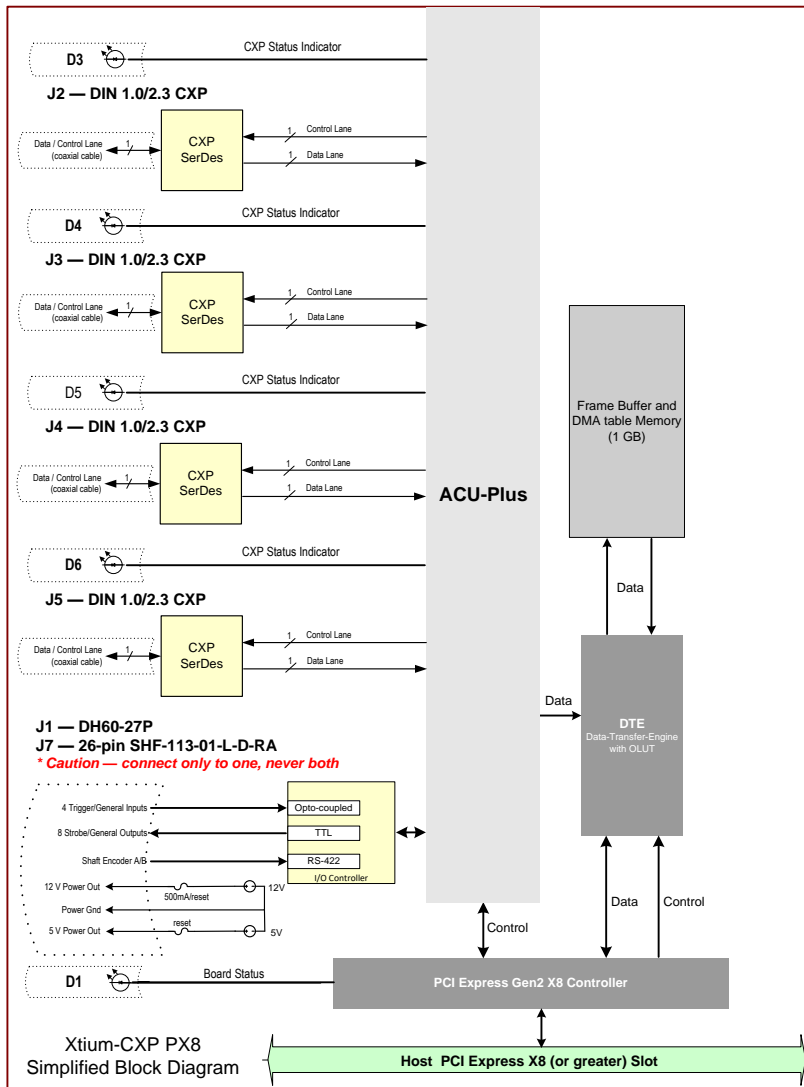


Figure 29: Xtium-CXP PX8 Block Diagram

# Xtium-CXP Flow Diagram

The following diagram represents the sequence in which the camera data acquired is processed through the Xtium-CXP.

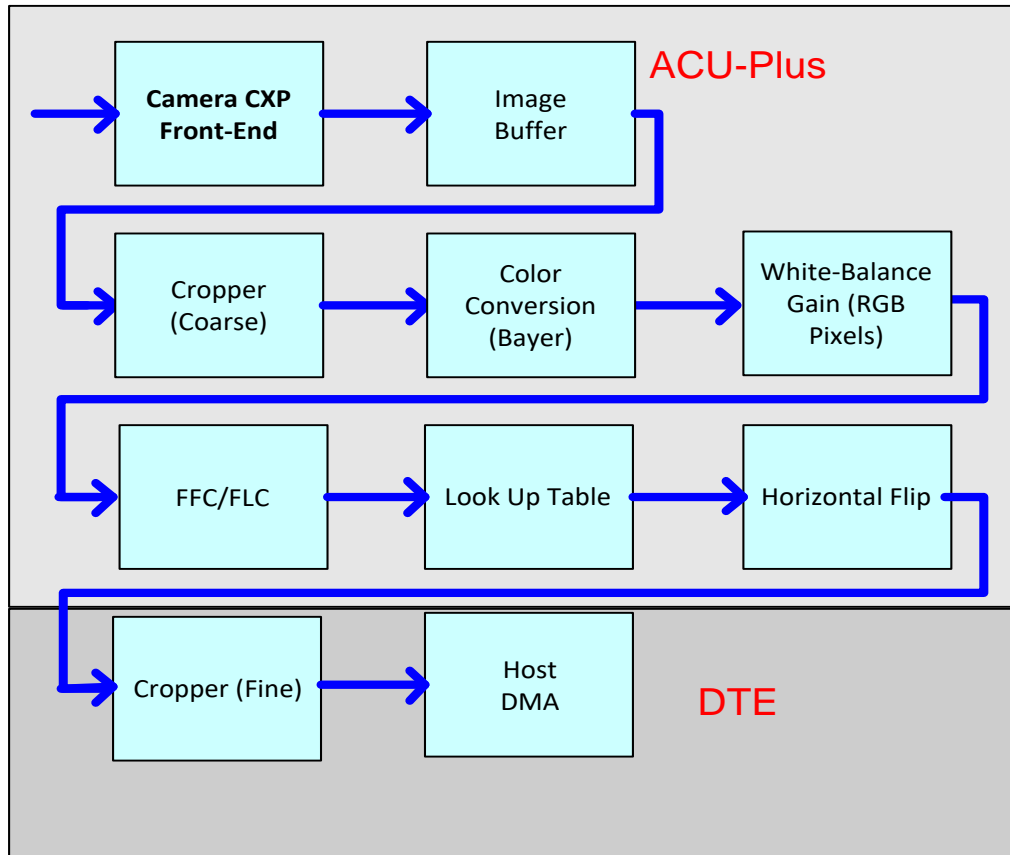


Figure 30: Xtium-CXP Flow Diagram

- **Camera CXP Front End:** Extracts the video data packets from the Camera CXP port(s).
- **Image Buffer:** Stores the video data using the model of video frames.
- **Cropper (Coarse):** Horizontal cropper used when reading out from the memory.
- **Color Conversion:** When enabled for particular cameras, converts Bayer video data into RGB data.
- **White Balance Gain:** Applies White Balance Gain to RGB data.
- **FFC/FLC:** Flat Field/Flat Line correction. Applies to Monochrome data only.
- **Lookup Tables:** Apply lookup table transformation to the image.
- **Horizontal Flip:** Performs the line data flip process.
- **Cropper (Fine):** Crops the resulting image when used, using an 8-byte resolution.
- **Host DMA:** Transfers the data from frame grabber into the host buffer memory. This module will also perform the vertical flip if enabled.

# Line Trigger Source Selection for Line scan Applications

Line scan imaging applications require some form of external event trigger to synchronize line scan camera exposures to the moving object. This synchronization signal is either an external trigger source (one exposure per trigger event) or a shaft encoder source composed of a single or dual phase (also known as a quadrature) signal.

The Xtium-CXP PX8 shaft encoder inputs provide additional functionality with pulse drop, pulse multiply, and pulse direction support.

The following table describes the line-trigger source types supported by the Xtium-CXP PX8. Refer to the Spera Acquisition Parameters Reference Manual (OC-SAPM-APR00) for descriptions of the Spera parameters.

## CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_SOURCE – Parameter Values Specific to the Xtium-CXP PX8

Table 6: CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_SOURCE – Parameter Values

| PRM Value | Input used as:<br>External Line Trigger                       | Input used as:<br>External Shaft Encoder                   |
|-----------|---|--|
|           | <i>if</i><br>CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE = <i>true</i> | <i>if</i><br>CORACQ_PRM_SHAFT_ENCODER_ENABLE = <i>true</i> |
| <b>0</b>  | From Shaft Encoder Phase A                                    | From Shaft Encoder Phase A & B                             |
| <b>1</b>  | From Shaft Encoder Phase A                                    | From Shaft Encoder Phase A                                 |
| <b>2</b>  | From Shaft Encoder Phase B                                    | From Shaft Encoder Phase B                                 |
| <b>3</b>  | n/a   | From Shaft Encoder Phase A & B                             |
| <b>4</b>  | From Board Sync #1  | n/a  |
| <b>5</b>  | From Board Sync #2  | n/a  |

### CVI/CCF File Parameters Used

- External Line Trigger Source = parameter value
- External Line Trigger Enable = true/false
- Shaft Encoder Enable = true/false

# Shaft Encoder Interface Timing

## Dual Balanced Shaft Encoder RS-422 Inputs:

- Input Phase A: Connector J1/J7: Pin 3 (Phase A +) & Pin 2 (Phase A -)
- Input Phase B: Connector J1/J7: Pin 6 (Phase B+) & Pin 5 (Phase B-)
- See J1: External I/O Signals Connector (Female DH60-27P) for complete connector signal details)

Web inspection systems with variable web speeds typically provide one or two synchronization signals from a web mounted encoder to coordinate trigger signals. These trigger signals are used by the acquisition linescan camera. The Xtium-CXP PX8 supports single or dual phase shaft encoder signals. Dual encoder signals are typically 90 degrees out of phase relative to each other and provide greater web motion resolution.

## Example using any Encoder Input with Pulse-drop Counter

When enabled, the triggered camera acquires one scan line for each shaft encoder pulse-edge. To optimize the web application, a second Sapera parameter defines the number of triggers to skip between valid acquisition triggers. The figure below depicts a system where a valid camera trigger is any pulse edge from either shaft encoder signal. After a trigger, the two following triggers are ignored (as defined by the Sapera pulse drop parameter).

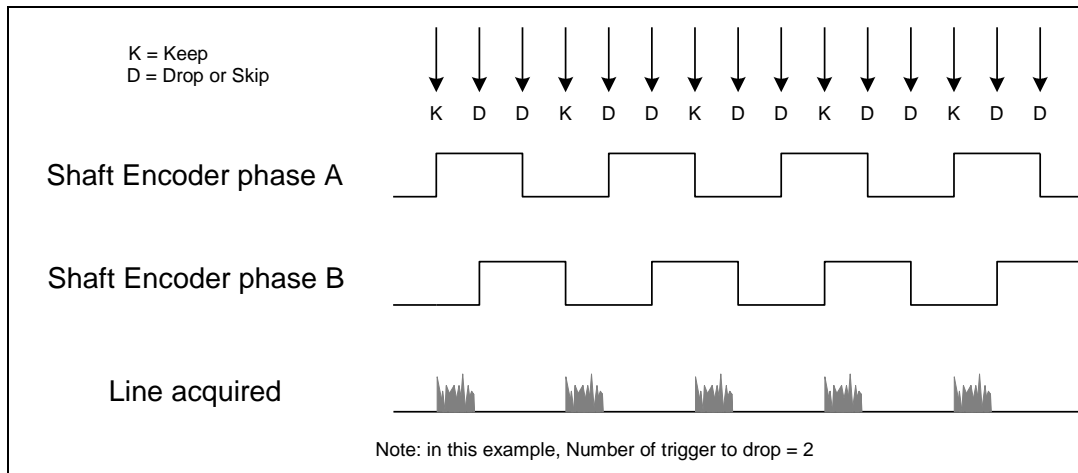


Figure 31: Encoder Input with Pulse-drop Counter



## Example using Sequential Encoder Input

Support of a dual phase encoder should consider the direction of motion of one phase signal to the other. Such a case might exist where system vibrations and/or conveyor backlash can cause the encoder to briefly travel backwards. The acquisition device must in those cases count the reverse steps and subtract the forward steps such that only pulses after the reverse count reaches zero are considered. By using the event "Shaft Encoder Reverse Counter Overflow", an application can monitor an overflow of this counter. The maximum count that can be reached by the counter is returned by the capability `CORACQ_CAP_SHAFT_ENCODER_REVERSE_COUNT_MAX`. Reading the parameter `CORACQ_PRM_SHAFT_ENCODER_REVERSE_COUNT` returns the current count value and writing any value to this parameter will reset the count to 0.

Also, if a maximum line rate camera trigger source is a high jitter shaft encoder, the parameter `CORACQ_PRM_LINE_TRIGGER_AUTO_DELAY` can be used to automatically delay line triggers to avoid over-triggering a camera, and thus not miss a line. Note that some cameras integrate this feature. See also the event "[Line Trigger Too Fast](#)" that can be enabled when using the 'auto delay' feature.

The example figure below shows shaft encoder signals with high jitter. If the acquisition is triggered when phase B follows phase A, with jitter present phase B may precede phase A. Use of the *Shaft Encoder Direction* parameter will prevent false trigger conditions.

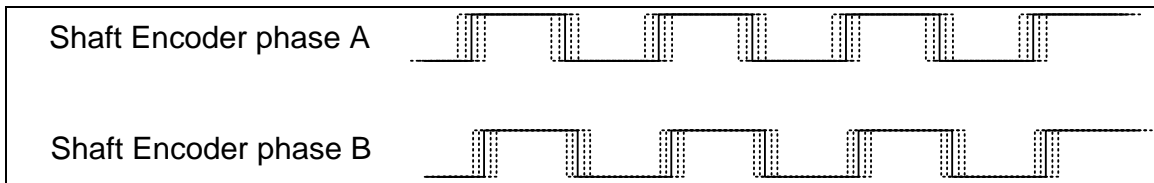


Figure 32: Using Shaft Encoder Direction Parameter



**Note:** Modify camera file parameters easily with the Sopera CamExpert program.

## CVI/CCF File Parameters Used

**Shaft Encoder Enable** = X, where:

- If X = 1, Shaft Encoder is enabled
- If X = 0, Shaft Encoder is disabled

**Shaft Encoder Pulse Drop** = X, where:

- X = number of trigger pulses ignored between valid triggers

**Shaft Encoder Pulse Multiply** = X, where:

- X = number of trigger pulses generated for each shaft encoder pulses

**Shaft Encoder Pulse Drop/Multiply Order** = X, where:

- If X = 1, the drop operation will be done first, followed by the multiplier operation
- If X = 0 or 2, the multiplier operation will be done first, followed by the drop operation

**Shaft Encoder Direction** = X, where:

- X = 0, Ignore direction
- X = 1, Forward steps are detected by pulse order A/B (forward motion)
- X = 2, Forward steps are detected by pulse order B/A (reverse motion)



**Note:** For information on camera configuration files, see the Sopera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

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## Virtual Frame Trigger for Line Scan Cameras

When using line scan cameras, a frame buffer is allocated in host system memory to store captured video lines. To control when a video line is stored as the first line in this “virtual” frame buffer, an external frame trigger signal is used.

For **fixed length** frames, the Spera vertical cropping parameter controls the number of lines sequentially grabbed and stored in the virtual frame buffer.

For **variable length** frames, the External Frame Trigger (when a level or dual input type is selected) controls the number of lines sequentially grabbed up to the maximum of lines in the virtual frame buffer.

For both fixed and variable length frames, choosing an active low/high or dual input permits grabbing multiple consecutive images as long as the chosen signal is active. This action is also called “rolling over” to the next buffer. When choosing a single rising or falling edge, a single frame will be acquired, there is never any roll over.

| External Frame Trigger Detection | Fixed Frame  | Variable Frame |
|----------------------------------|--------------|----------------|
| Active Low/High                  | Roll Over    | Roll Over      |
| Rising/Falling Edge              | No Roll Over | No Roll Over   |
| Dual Input Rising/Falling Edge   | Roll Over    | Roll Over      |

### Virtual Frame Trigger Timing Diagram

The virtual frame trigger signal (generated by some external event) connects to the Xtium-CXP PX8 trigger input.

- Virtual frame trigger can be differential (RS-422) or single ended (TTL, 12V, or 24V) industry standard, and be rising or falling edge active, active high or low, or double pulse rising or falling edge.
- In this example, virtual frame trigger control is configured for rising edge trigger.
- Virtual frame trigger connects to the Xtium-CXP PX8 via the External Trigger Input 1 & 2 inputs.
  - Trigger Input #1 on connector J1: pin 8
  - Trigger Input #2 on connector J1: pin 9
- Camera control signals are active at all times. These continually trigger the camera acquisition in order to avoid corrupted video lines at the beginning of a virtual frame.
- The camera control signals are either timing controls on Xtium-CXP PX8 shaft encoder inputs, or line triggers generated internally by the Xtium-CXP PX8.
- The Spera vertical cropping parameter specifies the number of lines captured.

### Synchronization Signals for a 10 Line Virtual Frame

The following timing diagram shows the relationship between External Frame Trigger input, External Shaft Encoder input (one phase used with the second terminated), and camera control output to the camera.

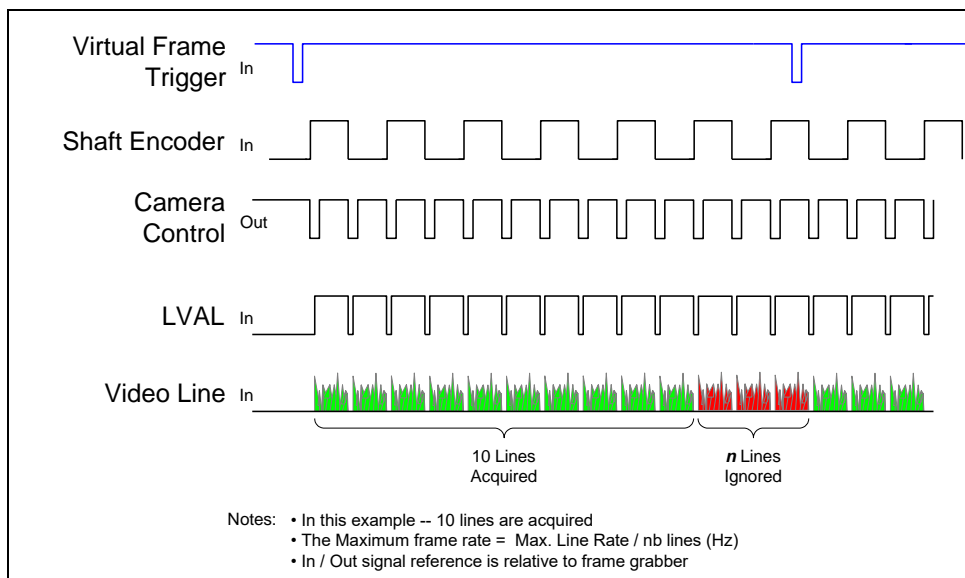


Figure 33: Synchronization Signals for a 10 Line Virtual Frame

### Synchronization Signals for Fixed Frame Length Acquisition

A trigger event is only generated when a grab is active; when not grabbing no trigger events are generated. When a frame is complete, the frame grabber checks for the specified active trigger level and, if present, grabs the next frame; otherwise, it waits for the next detected active trigger level.

In the following diagrams:

*Software Grab Start* indicates that the acquisition has been started using a software command (for example, SapTransfer::Grab).

*Software Grab Freeze* indicates that the acquisition has been stopped using a software command (for example, SapTransfer::Freeze).

"T" indicates a valid external trigger event (SapAcquisition::EventExternalTrigger).

"Ignored" is an ignored event (SapAcquisition::EventExternalTriggerIgnored).

such that

*Ignored* + *T* = total triggers received by frame grabber

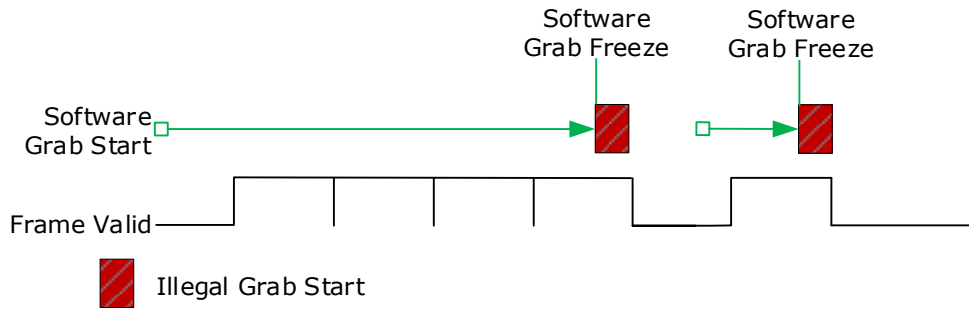


Figure 34: Line scan, Fixed Frame, No Trigger

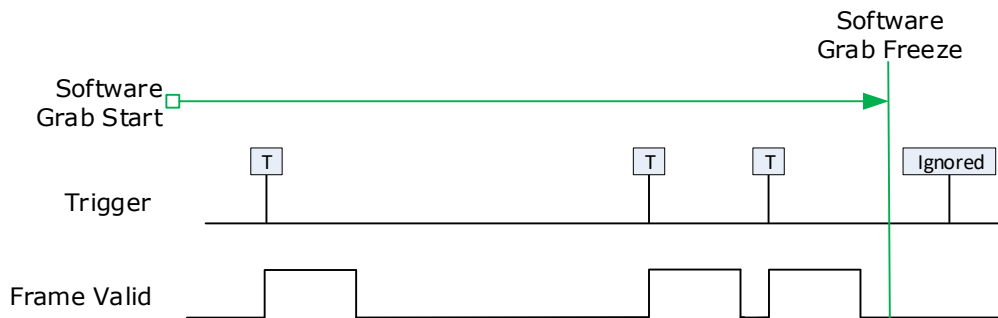


Figure 35: Line scan, Fixed Frame, Edge Trigger

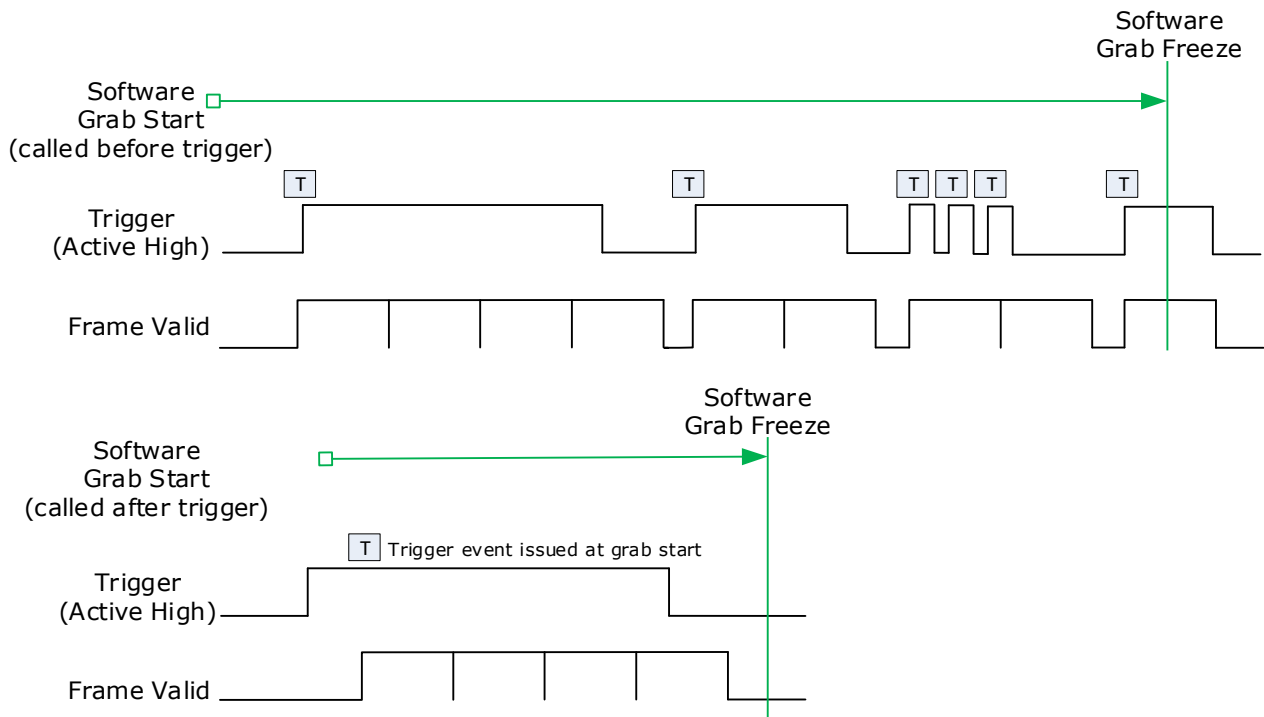


Figure 36: Line scan, Fixed Frame, Level Trigger (Roll-Over to Next Frame)

### Synchronization Signals for Variable Frame Length Acquisition

For variable length frames, trigger ignored events are not issued (SapAcquisition::EventExternalTriggerIgnored); a valid trigger event always initiates either a frame start or frame end.

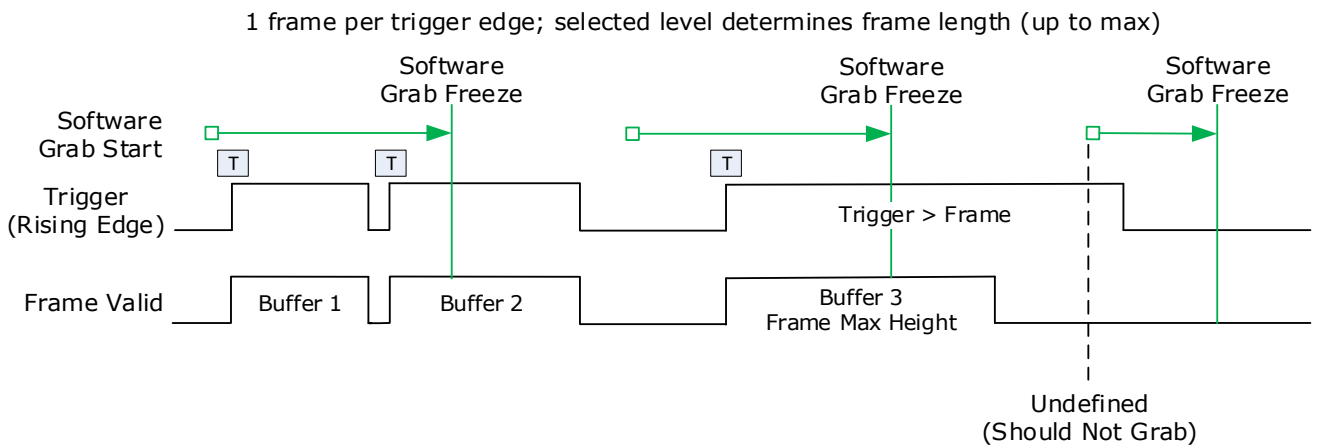


Figure 37: Line scan, Variable Frame, Edge Trigger (Active High determines Frame Length)

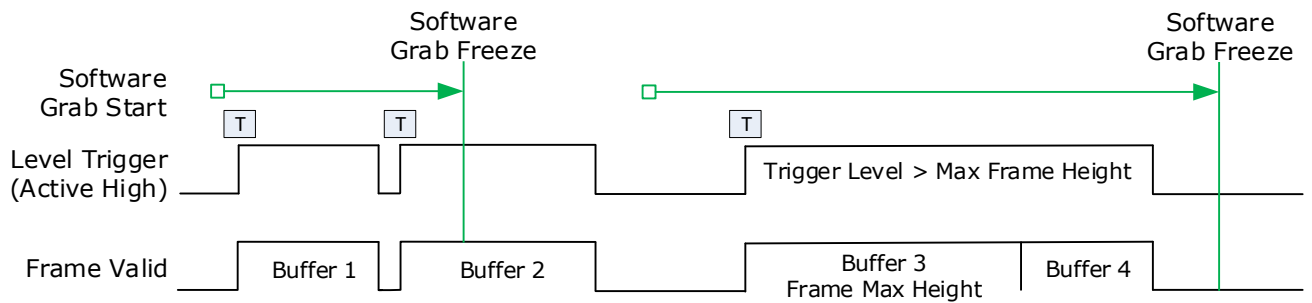


Figure 38: Line scan, Fixed Frame, Level Trigger ( Roll-Over)

### CVI File (VIC) Parameters Used

The VIC parameters listed below provide the control functionality for virtual frame reset. Sopera applications load pre-configured CVI files or change VIC parameters during runtime.



**Note:** Sopera camera file parameters are easily modified by using the CamExpert program.

**External Frame Trigger Enable** =  $X$ , where: (with Virtual Frame Trigger enabled)

- If  $X = 1$ , External Frame Trigger is enabled
- If  $X = 0$ , External Frame Trigger is disabled

**External Frame Trigger Detection** =  $Y$ , where: (with Virtual Frame Trigger edge select)

- If  $Y = 1$ , External Frame Trigger is active low
- If  $Y = 2$ , External Frame Trigger is active high
- If  $Y = 4$ , External Frame Trigger is active on rising edge
- If  $Y = 8$ , External Frame Trigger is active on falling edge
- If  $Y = 32$ , External Frame Trigger is dual-input rising edge
- If  $Y = 64$ , External Frame Trigger is dual-input falling edge



**Note:** For dual-input triggers, Trigger Input #1 signals the start of the frame trigger, Trigger Input #2 signals the end of the frame trigger.

**External Frame Trigger Level** =  $Z$ , where: (with Virtual Frame Trigger signal type)

- If  $Z = 1$ , External Frame Trigger is a TTL signal
- If  $Z = 2$ , External Frame Trigger is differential signal (RS-422)
- If  $Z = 8$ , External Frame Trigger is a 24V signal
- If  $Z = 64$ , External Frame Trigger is a 12V signal



**Note:** For information on camera configuration files, see the Sopera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

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## Sapera Acquisition Methods

Sapera acquisition methods define the control and timing of the camera and frame grabber board. Various methods are available, grouped as:

- Camera Trigger Methods (method 1 supported)
- Line Trigger Methods (method 1)
- Line Integration Methods (method 3 supported)
- Time Integration Methods (method 1 supported)
- Strobe Methods (method 1, 3 and 4 supported)

Refer to the Sapera LT Acquisition Parameters Reference manual (OC-SAPM-APR00) for detailed information concerning camera and acquisition control methods.

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# Trigger to Image Reliability

Trigger-to-image reliability incorporates all stages of image acquisition inside an integrated controller to increase reliability and simplify error recovery. The trigger-to-image reliability model brings together all the requirements for image acquisition to a central management unit. These include signals to control camera timing, on-board frame buffer memory to compensate for PCI bus latency, and comprehensive error notification. If the Xtium-CXP PX8 detects a problem, the application can take appropriate action to return to normal operation.

The Xtium-CXP PX8 is designed with a robust ACU (Acquisition and Control Unit). The ACU monitors in real-time, the acquisition state of the input plus the DTE (Data Transfer Engine) which transfers image data from on-board memory into PC memory. In general, these management processes are transparent to end-user applications. With the Xtium-CXP PX8, applications ensure trigger-to-image reliability by monitoring events and controlling transfer methods as described below:

## Supported Events and Transfer Methods

Listed below are the supported acquisition and transfer events. Event monitoring is a major component to the Trigger-to-Image Reliability framework.

### *Acquisition Events*

Acquisition events pertain to the acquisition module. They provide feedback on the image capture phase.

- **External Trigger** (Used/Ignored)  
Generated when the external trigger pin is asserted, which indicates the start of the acquisition process. There are two types of external trigger events: 'Used' or 'Ignored'. Following an external trigger, if the event generates a captured image, an External Trigger Used event will be generated (CORACQ\_VAL\_EVENT\_TYPE\_EXTERNAL\_TRIGGER). If there is no captured image, an External Trigger Ignored event will be generated (CORACQ\_VAL\_EVENT\_TYPE\_EXTERNAL\_TRIGGER\_IGNORED). An external trigger event is ignored if the event rate is higher than the possible frame rate of the camera.
- **Start of Frame**  
Event generated during acquisition, with the detection of the start of a video frame by the board acquisition hardware. The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_START\_OF\_FRAME.
- **End of Frame**  
Event generated during acquisition, with the detection of the end of a video frame by the board acquisition hardware. The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_END\_OF\_FRAME.
- **Data Overflow**  
The Data Overflow event indicates that there is not enough bandwidth for the acquired data transfer without loss. Data Overflow would occur with limitations of the acquisition module and should never occur.  
The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_DATA\_OVERFLOW.
- **Frame Valid**  
Event generated on detection of the start of a video frame by the board acquisition hardware. Acquisition does not need to be active; therefore, this event can verify a valid signal is connected. The Sopera event value is: CORACQ\_VAL\_EVENT\_TYPE\_VERTICAL\_SYNC.
- **Link** Lock/Unlock)  
Event generated on the transition from locking or not locking, of the required lanes. The Sopera event values are:  
CORACQ\_VAL\_EVENT\_TYPE\_LINK\_LOCK  
CORACQ\_VAL\_EVENT\_TYPE\_LINK\_UNLOCK.



- **Frame Lost**  
The Frame Lost event indicates that an acquired image failed to transfer to on-board memory. An example is if there are no free on-board buffers available for the new image. This may be the case if the image transfer from onboard buffers to host PC memory is not sustainable due to bus bandwidth issues or no host buffers are available to receive an image.  
The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_FRAME\_LOST.
- **External Line Trigger Too Slow**  
Event which indicates that the detected shaft encoder input tick rate is too slow for the device to take into account the specified shaft encoder multiplier value. The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_EXT\_LINE\_TRIGGER\_TOO\_SLOW.
- **Line Trigger Too Fast**  
Event which indicates a previous line-trigger did not generate a complete video line from the camera. Note that due to jitter associated with using shaft encoders, the acquisition device can delay a line trigger if a previous line has not yet completed. This event is generated if a second line trigger comes in while the previous one is still pending. This event is generated once per virtual frame. The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_LINE\_TRIGGER\_TOO\_FAST.
- **Shaft Encoder Reverse Count Overflow**  
Event which indicates that the shaft encoder has travelled in the opposite direction expected and that the number of pulses encountered during that travel has exceeded the acquisition device counter. The acquisition device will thus not be able to skip the appropriate number of pulses when the expected direction is detected. The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_SHAFT\_ENCODER\_REVERSE\_COUNT\_OVERFLOW
- **Link Error**  
Event which indicates that an error has occurred on one or more of the lanes. Information about the source of the link error and the number of occurrences of this error can be retrieved using the SapAcqCallbackInfo class.
  - **GetGenericParam0:** returns the source of the error:
    - 1: CRC Error
    - 2: 8B/10B Error
    - 3: Packet Buffer Overflow
    - 4: Packet Size Error
  - **GetGenericParam1:** returns a bitfield indicating which lane(s) generated the error
    - Bit 0 = Lane 1, Bit 1= Lane 2, ...
  - **GetCustomSize:** returns 4 \* UINT32
  - **GetCustomData:** returns the number of errors per lane. There are 4 entries, each entry being a UINT32.
  - **Note:** 8B/10B error is the only error that is per lane. CRC error, Packet BufferOverflow and Packet Size Error is per camera and will always be linked to the master lane of the camera.

## Transfer Events

Transfer events are the ones related to the transfer module. Transfer events provide feedback on image transfer from onboard memory frame buffers to PC memory frame buffers.

- **Start of Frame**  
Start of Frame event generated when the first image pixel is transferred from on-board memory into PC memory.  
The Sapera event value is CORXFER\_VAL\_EVENT\_TYPE\_START\_OF\_FRAME.
- **End of Frame**  
End of Frame event generated when the last image pixel is transferred from on-board memory into PC memory.  
The Sapera event value is CORXFER\_VAL\_EVENT\_TYPE\_END\_OF\_FRAME.
- **End of Line**  
The End of Line event is generated after a video line is transferred to a PC buffer.  
The Sapera event value is CORXFER\_VAL\_EVENT\_TYPE\_END\_OF\_LINE.
- **End of N Lines**  
The End of N Lines event is generated after a set number of video lines are transferred to a PC buffer. The Sapera event value is CORXFER\_VAL\_EVENT\_TYPE\_END\_OF\_NLINES.
- **End of Transfer**  
End of Transfer event generated at the completion of the last image transfer from on-board memory into PC memory. Issue a stop command to the transfer module to complete a transfer (if transfers are already in progress). If a frame transfer of a fixed number of images is requested, the transfer module will stop transfer automatically. The Sapera event value is CORXFER\_VAL\_EVENT\_TYPE\_END\_OF\_TRANSFER.

## Trigger Signal Validity

The ACU ignores external trigger signal noise with its programmable debounce control. Program the debounce parameter for the minimum pulse duration considered as a valid external trigger pulse. For more information see Note 1: General Inputs / External Trigger Inputs Specifications.

## Supported Transfer Cycling Methods

The Xtium-CXP PX8 supports the following transfer modes, which are either synchronous or asynchronous.

Images are accumulated in on-board memory in a FIFO type manner. On-board memory can get filled up if the rate at which the images are acquired is greater than the rate at which the DMA engine can write them to host buffer memory. On-board memory can also get filled-up if there are no more empty buffers available to transfer the on-board images.

When no memory is available for a new image to be stored in on-board memory, the image is discarded and a CORACQ\_VAL\_EVENT\_TYPE\_FRAME\_LOST or trash buffer callback is generated. If a CORACQ\_VAL\_EVENT\_TYPE\_FRAME\_LOST occurs when host buffers are available, it can indicate a problem with the PX4 bus bandwidth.

If image buffers are constructed using a trash buffer (SapBufferWithTrash using a transfer cycle mode with trash), when no host buffers are available and no memory is available for a new image to be stored in on-board memory, the SapXferCallbackInfo::IsTrash (C++) function or SaxXferNotifyEventsArgs.Trash (.NET) property returns true. If a trash callback function has been registered during construction of the SapTransfer object, it will be executed when a trash event occurs.

When stopping the image acquisition, the event CORXFER\_VAL\_EVENT\_TYPE\_END\_OF\_TRANSFER will occur once all images currently in the on-board memory are transferred to host buffer memory. Note that if the application does not provide enough empty buffers, the Xtium event will not occur and an acquisition abort will be required.

- **CORXFER\_VAL\_CYCLE\_MODE\_SYNCHRONOUS\_WITH\_TRASH**  
Before cycling to the next buffer in the list, the transfer device will check the next buffer's state. If its state is full, the transfer will keep the image in on-board memory until the next buffer's state changes to empty. If the on-board memory gets filled, trash callbacks will be generated.
- **CORXFER\_VAL\_CYCLE\_MODE\_SYNCHRONOUS\_NEXT\_EMPTY\_WITH\_TRASH**  
When starting an acquisition, the buffer list is put in an empty buffer queue list in the exact order they were added to the transfer. Whenever a user sets a buffer to empty, it is added to the empty buffer queue list, so that after cycling once through the original buffer list, the buffers acquired into will follow the order in which they are put empty by the user. So in this mode, the on-board images will be transferred to host buffer memory as long as there are buffers in the empty buffer queue list. If no buffers are available on the host and the on-board memory gets filled, trash callbacks will be generated.
- **CORXFER\_VAL\_CYCLE\_MODE\_ASYNCHRONOUS**  
The transfer device cycles through all buffers in the list without concern about the buffer state.

The following table describes the possible buffer states and resulting behavior:

| Trash Buffer<br>(cycling mode with trash) | Xtium On-Board<br>Memory State         | Host Sopera Buffer<br>State            | Resulting Event                       |
|---|--|--|---------------------------------------|
| NO  | Empty buffer available<br>(at least 1) | Empty buffer available<br>(at least 1) | Normal acquisition events             |
| NO  | Empty buffer available<br>(at least 1) | Full                                   | Acquire into Xtium on-board<br>memory |
| NO  | Full                                   | Empty buffer available<br>(at least 1) | Frame Lost Event                      |
| NO  | Full                                   | Full                                   | Frame Lost Event                      |
| YES                                       | Empty buffer available<br>(at least 1) | Empty buffer available<br>(at least 1) | Normal acquisition events             |
| YES                                       | Empty buffer available<br>(at least 1) | Full                                   | Acquire into Xtium on-board<br>memory |
| YES                                       | Full                                   | Empty buffer available<br>(at least 1) | Frame Lost Event                      |
| YES                                       | Full                                   | Full                                   | Trash Callback                        |

- By default, the buffer state (empty or full) is automatically managed by Sopera LT; it can be managed manually by the user if necessary.

## Output LUT Availability

The following table defines the supported output LUT (look up tables) for the Xtium-CXP PX8. Note that unsupported modes are not listed.

Table 7: Output LUT Availability

| Number of Digital Bits | Output Pixel Format                           | LUT Format   | Notes*                       |
|------------------------|---|--|------------------------------|
| 8                      | MONO 8  | 8-in, 8-out  | 8 bits in 8 LSBs of 16-bit   |
| 8                      | MONO 16                                       | 8-in, 16-out   |                              |
| 10                     | MONO 8  | 10-in, 8-out   |                              |
| 10                     | MONO 16                                       | 10-in, 16-out  | 10 bits in 10 LSBs of 16-bit |
| 12                     | MONO 8  | 12-in, 8-out   | 8 MSB                        |
| 12                     | MONO 16                                       | 12-in, 16-out  | 12 bits in 12 LSBs of 16-bit |
| 8 x 3 (RGB)            | RGB888<br>RGB8888<br>RGBP8                    | 8-in, 8-out  |                              |
| 10 x 3 (RGB)           | RGB888<br>RGB8888<br>RGB101010<br>RGB16161616 | 10-in, 8-out<br>10-in, 8-out<br>10-in, 10-out<br>10-in, 16-out | 10 bits in 10 LSBs of 16-bit |
| 12 x 3 (RGB)           | RGB888<br>RGB8888<br>RGB101010<br>RGB16161616 | 12-in, 8-out<br>12-in, 8-out<br>12-in, 10-out<br>12-in, 16-out | 12 bits in 12 LSBs of 16-bit |

\*When no LUTs are available or LUTs are disabled, the data is packed in the LSBs of the target destination.

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# Flat Field Correction: Theory of Operation

The following provides additional details on the Flat Field Correction and Flat Line Correction (FFC/FLC) implementation.

## Flat Field Correction Lists

The Xtium-CXP PX8 supports defining more than one Flat Field Correction (FFC) / Flat Line Correction (FLC) data sets. Using the Xfer parameter `CORXFER_PRM_FLATFIELD_CYCLE_MODE`, the user can decide to cycle automatically through the list of FFC/FLC sets by setting the parameter to `CORXFER_VAL_FLATFIELD_CYCLE_MODE_AUTOMATIC`, or select a specific FFC/FLC set from the list by setting the parameter to `CORXFER_VAL_FLATFIELD_CYCLE_MODE_OFF` and selecting the FFC/FLC index to use with the parameter `CORACQ_PRM_FLAT_FIELD_SELECT`.

While the cycling mode is set to off, users can upload new coefficients to an inactive FFC set even when grabbing. When cycling automatically, the FFC/FLC sets are selected in a round-robin fashion, changing at the beginning of every new frame.

The architecture of the Xtium-CXP PX8 is such that the FFC/FLC data sets are independent of the host buffers. In automatic mode, the FFC/FLC sets are chosen in a round-robin fashion as images are acquired. So if using the Xfer cycling mode Synchronous with Trash, it is recommended that the number of host buffers be a multiple of the number of FFC/FLC in the list in order to maintain the FFC/FLC relationship with the Host buffers.

- When the FFC/FLC cycle mode automatic is active, reset the acquisition module to start on the 1<sup>st</sup> FFC/FLC data set of the selected list as follows:
  - Disconnect/Reconnect the transfer (assuming 1<sup>st</sup> buffer is empty).
  - Selecting a set using the `CORACQ_PRM_FLAT_FIELD_SET_SELECT` parameter will choose the 1<sup>st</sup> FFC/FLC in the list of the selected set.
- When the FFC/FLC cycle mode automatic is active, start the acquisition module to start on a specific FFC/FLC of the selected list as follows:
  - While acquisition is stopped, by selecting an Xfer pair [ACQ, Buffer]. The index of the FFC/FLC will be selected based on the modulo of the number of FFC/FLC in the list with respect to the [ACQ, Buffer] index pair.

## Flat Field Correction Sets

The concept of sets allows a user to define multiple lists of FFC/FLC correction data. The FFC/FLC API allows users to allocate and pre-program those FFC/FLC sets. When acquiring images, the board driver will cycle through the FFC/FLC list of the selected set. During that operation, users can upload new FFC/FLC data to non-active sets without any ill effects.

When changing the active set while grabbing, the new active set will be switched when the current cycling of the current list is completed.

### ***Xtium-CXP PX8 specific limitations***

- Software driver permits the creation of up to 16 FFC/FLC sets.
- Software driver permits the use of up to 16 sets.
- When the FFC cycling mode is off, the concept of sets is not used. Whichever a FFC index is chosen using CORACQ\_PRM\_FLAT\_FIELD\_SELECT, it will be used independently of the set it belongs to.
- Upload of any FFC data is permitted at any time, even while grabbing. If an upload is done to an FFC index of the currently select set while grabbing, then the resulting acquired image will be undefined.
- When changing FFC cycling mode, the acquisition must be stopped.

### ***Programming the sets***

The following scheme is used to program FFC/FLC data within a set:

```
// select an active set
CorAcqSetPrm( hAcq, CORAQ_PRM_FLAT_FIELD_SET_SELECT, 0);

// Create 4 new FFC that will be part of the currently active set '0'
For( i = 0; i < 4; i++)
{
CorAcqNewFlatfield( hAcq, pFlatfieldNumber); // Will create FFC #1, #2, #3, #4
}

// select an active set
CorAcq SetPrm( hAcq, CORAQ_PRM_FLAT_FIELD_SET_SELECT, 1);

// Create 4 new FFC that will be part of the currently active set '1'
For( i = 0; i < 4; i++)
{
CorAcqNewFlatfield( hAcq, pFlatfieldNumber); // Will create FFC #5, #6, #7, #8
}
}
```

# Xtium-CXP PX8 Supported Parameters

The tables below describe the Spera capabilities supported by the Xtium-CXP PX8. Unless specified, each capability applies to all configuration modes and all acquisition modes.

The information here is subject to change. The application needs to verify capabilities. New board driver releases may change product specifications.

Spera describes the Xtium-CXP PX8 family as:

- Board Server: Xtium-CXP\_PX8\_1
- Acquisition Module: *dependent on firmware used*

## Camera Related Capabilities

Table 8: Camera Related Capabilities

| Capability                | Values                               |
|---------------------------|--------------------------------------|
| CORACQ_CAP_CONNECTOR_TYPE | CORACQ_VAL_CONNECTOR_TYPE_CXP (0x20) |

## Camera Related Parameters

Table 9: Camera Related Parameters

| Parameter                        | Values   |
|----------------------------------|--|
| CORACQ_PRM_CHANNEL               | CORACQ_VAL_CHANNEL_SINGLE (0x1)  |
| CORACQ_PRM_FRAME                 | CORACQ_VAL_FRAME_PROGRESSIVE (0x2)   |
| CORACQ_PRM_INTERFACE             | CORACQ_VAL_INTERFACE_DIGITAL (0x2)   |
| CORACQ_PRM_SCAN                  | CORACQ_VAL_SCAN_AREA (0x1)<br>CORACQ_VAL_SCAN_LINE (0x2)   |
| CORACQ_PRM_SIGNAL                | CORACQ_VAL_SIGNAL_DIFFERENTIAL (0x2)   |
| CORACQ_PRM_VIDEO                 | <i>Mono</i> CORACQ_VAL_VIDEO_MONO (0x1)<br>CORACQ_VAL_VIDEO_BAYER (0x10)<br><br><i>RGB</i> CORACQ_VAL_VIDEO_RGB (0x8)<br><br><i>Bayer</i> CORACQ_VAL_VIDEO_BAYER (0x10)  |
| CORACQ_PRM_PIXEL_DEPTH           | <i>Mono</i> 8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8<br>8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO16<br>10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8<br>10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO16<br>12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8<br>12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO16<br>14 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO16<br>16 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO16<br><br><i>RGB</i> 8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8<br><i>Bayer</i> 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8<br>10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10<br>10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI16<br>12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8<br>12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10<br>12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI16 |
| CORACQ_PRM_VIDEO_STD             | CORACQ_VAL_VIDEO_STD_NON_STD (0x1)   |
| CORACQ_PRM_FIELD_ORDER           | CORACQ_VAL_FIELD_ORDER_NEXT_FIELD (0x4)  |
| CORACQ_PRM_HACTIVE               | <i>Mono</i> min = 32 pixel<br><i>Bayer</i> max = 65536 pixel<br>step = 1 pixel<br><br><i>RGB</i> min = 32 pixel<br>max = 16384 pixel<br>step = 1 pixel   |
| CORACQ_PRM_VACTIVE               | min = 1 line<br>max = 16777215 line<br>step = 1 line   |
| CORACQ_PRM_TIME_INTEGRATE_METHOD | CORACQ_VAL_TIME_INTEGRATE_METHOD_1 (0x1)   |

|  |  |  |
|--|--|--|
| CORACQ_PRM_CAM_TRIGGER_METHOD              |  | CORACQ_VAL_CAM_TRIGGER_METHOD_1 (0x1)  |
| CORACQ_PRM_CAM_TRIGGER_POLARITY            |  | CORACQ_VAL_ACTIVE_LOW (0x1)<br>CORACQ_VAL_ACTIVE_HIGH (0x2)  |
| CORACQ_PRM_CAM_TRIGGER_DURATION            |  | min = 5 µsec<br>max = 85899345 µs<br>step = 1 µsec   |
| CORACQ_PRM_CAM_NAME                        | Mono<br>RGB<br>Bayer   | Default Camera CXP Area Scan Mono<br>Default Camera CXP Area Scan Color<br>Default Camera CXP Bayer Area Scan Color  |
| CORACQ_PRM_LINE_INTEGRATE_METHOD           |  | CORACQ_VAL_LINE_INTEGRATE_METHOD_3 (0x4)   |
| CORACQ_PRM_LINE_TRIGGER_METHOD             |  | CORACQ_VAL_LINE_TRIGGER_METHOD_1 (0x1)   |
| CORACQ_PRM_LINE_TRIGGER_POLARITY           |  | CORACQ_VAL_ACTIVE_LOW (0x1)<br>CORACQ_VAL_ACTIVE_HIGH (0x2)  |
| CORACQ_PRM_LINE_TRIGGER_DELAY              |  | min = 0 nsec<br>max = 4294967295 nsec<br>step = 1 nsec   |
| CORACQ_PRM_LINE_TRIGGER_DURATION           |  | min = 5000 nsec<br>max = 4294967295 nsec<br>step = 1 nsec  |
| CORACQ_PRM_CHANNELS_ORDER                  |  | CORACQ_VAL_CHANNELS_ORDER_NORMAL (0x1)   |
| CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MIN       |  | 1 Hz   |
| CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MAX       |  | 10000000 Hz  |
| CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MIN |  | 1 µs   |
| CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MAX |  | 85899345 µs  |
| CORACQ_PRM_CAM_IO_CONTROL (*)              |  |  |
| CORACQ_PRM_COLOR_ALIGNMENT                 | Bayer  | CORACQ_VAL_COLOR_ALIGNMENT_GB_RG (0x1)<br>CORACQ_VAL_COLOR_ALIGNMENT_BG_GR (0x2)<br>CORACQ_VAL_COLOR_ALIGNMENT_RG_GB (0x4)<br>CORACQ_VAL_COLOR_ALIGNMENT_GR_BG (0x8)                   |
| CORACQ_PRM_COLOR_ALIGNMENT                 |  | Not available  |
| CORACQ_PRM_CAM_CONTROL_DURING_READOUT      |  | CORACQ_VAL_CAM_CONTROL_DURING_READOUT_INVALID (0x0)<br>CORACQ_VAL_CAM_CONTROL_DURING_READOUT_VALID (0x01)<br>CORACQ_VAL_CAM_CONTROL_DURING_READOUT_IGNORE (0x2)                        |
| CORACQ_PRM_DATA_LANES                      | 1 CXP camera firmware<br>2 CXP camera firmware<br>3 CXP camera firmware<br>4 CXP camera firmware | min = 1 lane, max = 4 lanes, step = 1 lane<br>min = 1 lane, max = 2 lanes, step = 1 lane<br>min = 1 lane, max = 1/2 lanes, step = 1 lane<br>min = 1 lane, max = 1 lanes, step = 1 lane |
| CORACQ_PRM_BIT_TRANSFER_RATE               |  | 1.250 Gbps<br>2.500 Gbps<br>3.125 Gbps<br>5.000 Gbps<br>6.250 Gbps   |



## VIC Related Parameters

Table 10: VIC Related Parameters

| Parameter                          | Values                                |  |
|------------------------------------|---------------------------------------|--|
| CORACQ_PRM_CAMSEL                  | Mono<br>RGB<br>Bayer                  | CAMSEL_MONO = from 0 to 0<br>CAMSEL_RGB = from 0 to 0  |
| CORACQ_PRM_CROP_LEFT               | Mono<br>Bayer<br><br>RGB              | min = 0 pixel<br>max = 65528 pixel<br>step = 8 pixel<br><br>min = 0 pixel<br>max = 16376 pixel<br>step = 8 pixel   |
| CORACQ_PRM_CROP_TOP                |                                       | min = 0 line<br>max = 16777215 line<br>step = 1 line   |
| CORACQ_PRM_CROP_WIDTH              | Mono<br>Bayer<br><br>RGB              | min =32 pixel<br>max = 65536 pixel<br>step =8 pixel<br><br>min =32 pixel<br>max = 16384 pixel<br>step =8 pixel<br><br>* Maximum allowed is 64 kBytes, so maximum in pixels is dependent on the output pixel depth. For RGB-12, data is unpacked to 16161616, so maximum will be 8192 pixels. |
| CORACQ_PRM_CROP_HEIGHT             |                                       | min = 1 line<br>max = 16777215 line<br>step = 1 line   |
| CORACQ_PRM_DECIMATE_METHOD         |                                       | CORACQ_VAL_DECIMATE_DISABLE (0x1)  |
| CORACQ_PRM_LUT_ENABLE              |                                       | TRUE<br>FALSE  |
| CORACQ_PRM_LUT_NUMBER              |                                       | Default = 0  |
| CORACQ_PRM_STROBE_ENABLE           |                                       | TRUE<br>FALSE  |
| CORACQ_PRM_STROBE_METHOD           |                                       | CORACQ_VAL_STROBE_METHOD_1 (0x1)<br>CORACQ_VAL_STROBE_METHOD_3 (0x4)<br>CORACQ_VAL_STROBE_METHOD_4 (0x8)   |
| CORACQ_PRM_STROBE_POLARITY         |                                       | CORACQ_VAL_ACTIVE_LOW (0x1)<br>CORACQ_VAL_ACTIVE_HIGH (0x2)  |
| CORACQ_PRM_STROBE_DURATION         |                                       | min = 1 $\mu$ s<br>max = 85899345 $\mu$ s<br>step = 1 $\mu$ s  |
| CORACQ_PRM_STROBE_DELAY            |                                       | min = 0 $\mu$ s<br>max = 85899345 $\mu$ s<br>step = 1 $\mu$ s  |
| CORACQ_PRM_TIME_INTEGRATE_ENABLE   |                                       | TRUE<br>FALSE  |
| CORACQ_PRM_TIME_INTEGRATE_DURATION |                                       | min = 5 $\mu$ s<br>max = 85899345 $\mu$ s<br>step = 1 $\mu$ s  |
| CORACQ_PRM_CAM_TRIGGER_ENABLE      |                                       | TRUE<br>FALSE  |
| CORACQ_PRM_OUTPUT_FORMAT           | Mono<br>Bayer<br><br><br>RGB<br>Bayer | CORACQ_VAL_OUTPUT_FORMAT_MONO8<br>CORACQ_VAL_OUTPUT_FORMAT_MONO16<br><br><br>CORACQ_VAL_OUTPUT_FORMAT_RGB8888<br>CORACQ_VAL_OUTPUT_FORMAT_RGB888<br>CORACQ_VAL_OUTPUT_FORMAT_RGB101010<br>CORACQ_VAL_OUTPUT_FORMAT_RGB16161616<br>CORACQ_VAL_OUTPUT_FORMAT_RGBP8 (8-bit only)                |
| CORACQ_PRM_EXT_TRIGGER_ENABLE      |                                       | CORACQ_VAL_EXT_TRIGGER_OFF (0x1)<br>CORACQ_VAL_EXT_TRIGGER_ON (0x8)  |
| CORACQ_PRM_VIC_NAME                | Mono<br><br>RGB<br>Bayer              | Default Camera CXP Area Scan Mono<br><br>Default Camera CXP Area Scan Color<br>Default Camera CXP Bayer Area Scan Color  |

|  |   |   |
|--|---|---|
| CORACQ_PRM_LUT_MAX                     |   | 1   |
| CORACQ_PRM_EXT_TRIGGER_DETECTION       |   | CORACQ_VAL_ACTIVE_LOW (0x1)<br>CORACQ_VAL_ACTIVE_HIGH (0x2)<br>CORACQ_VAL_RISING_EDGE (0x4)<br>CORACQ_VAL_FALLING_EDGE (0x8)  |
| CORACQ_PRM_LUT_FORMAT                  | <i>Mono</i><br><i>RGB</i><br><i>Bayer</i> | Default = CORDATA_FORMAT_MONO8<br>Default = CORDATA_FORMAT_COLORNI8   |
| CORACQ_PRM_LINE_INTEGRATE_ENABLE       |   | TRUE<br>FALSE   |
| CORACQ_PRM_LINE_INTEGRATE_DURATION     |   | min = 5000 nsec<br>max = 4294967295 nsec<br>step = 1 nsec   |
| CORACQ_PRM_LINE_TRIGGER_ENABLE         |   | TRUE<br>FALSE   |
| CORACQ_PRM_EXT_FRAME_TRIGGER_ENABLE    |   | TRUE<br>FALSE   |
| CORACQ_PRM_EXT_FRAME_TRIGGER_DETECTION |   | CORACQ_VAL_ACTIVE_LOW (0x1)<br>CORACQ_VAL_ACTIVE_HIGH (0x2)<br>CORACQ_VAL_RISING_EDGE (0x4)<br>CORACQ_VAL_FALLING_EDGE (0x8)<br>CORACQ_VAL_DOUBLE_PULSE_RISING_EDGE (0x20)<br>CORACQ_VAL_DOUBLE_PULSE_FALLING_EDGE (0x40) |
| CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE     |   | TRUE<br>FALSE   |
| CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION  |   | CORACQ_VAL_RISING_EDGE (0x4)<br>CORACQ_VAL_FALLING_EDGE (0x8)   |
| CORACQ_PRM_SNAP_COUNT                  |   | Not Available   |
| CORACQ_PRM_INT_LINE_TRIGGER_ENABLE     |   | TRUE<br>FALSE   |
| CORACQ_PRM_INT_LINE_TRIGGER_FREQ       |   | Default = 5000 Hz   |
| CORACQ_PRM_BIT_ORDERING                |   | CORACQ_VAL_BIT_ORDERING_STD (0x1)   |
| CORACQ_PRM_EXT_TRIGGER_LEVEL           |   | CORACQ_VAL_LEVEL_TTL (0x1)<br>CORACQ_VAL_LEVEL_422 (0x2)<br>CORACQ_VAL_LEVEL_12VOLTS (0x040)<br>CORACQ_VAL_LEVEL_24VOLTS (0x8)  |
| CORACQ_PRM_STROBE_LEVEL                |   | CORACQ_VAL_LEVEL_TTL (0x1)  |
| CORACQ_PRM_EXT_FRAME_TRIGGER_LEVEL     |   | CORACQ_VAL_LEVEL_TTL (0x1)<br>CORACQ_VAL_LEVEL_422 (0x2)<br>CORACQ_VAL_LEVEL_12VOLTS (0x040)<br>CORACQ_VAL_LEVEL_24VOLTS (0x8)  |
| CORACQ_PRM_EXT_LINE_TRIGGER_LEVEL      |   | CORACQ_VAL_LEVEL_422 (0x2)  |
| CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MIN   |   | 8 Hz  |
| CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MAX   |   | 500000 Hz   |
| CORACQ_PRM_MASTER_MODE                 |   | Not available   |
| CORACQ_PRM_SHAFT_ENCODER_DROP          |   | min = 0 tick<br>max = 254 tick<br>step = 1 tick   |
| CORACQ_PRM_SHAFT_ENCODER_ENABLE        |   | TRUE<br>FALSE   |
| CORACQ_PRM_EXT_TRIGGER_FRAME_COUNT     |   | min = 1 frame<br>max = 262142 frame<br>step = 1 frame<br>Note: Infinite not supported   |
| CORACQ_PRM_INT_FRAME_TRIGGER_ENABLE    |   | TRUE<br>FALSE   |
| CORACQ_PRM_INT_FRAME_TRIGGER_FREQ      |   | min = 1 milli-Hz<br>max = 10000000 milli-Hz<br>step = 1 milli-Hz  |
| CORACQ_PRM_STROBE_DELAY_2              |   | Not Available   |
| CORACQ_PRM_FRAME_LENGTH                |   | CORACQ_VAL_FRAME_LENGTH_FIX (0x1)<br>CORACQ_VAL_FRAME_LENGTH_VARIABLE (0x2)   |
| CORACQ_PRM_FLIP                        |   | CORACQ_VAL_FLIP_OFF (0x00)<br>CORACQ_VAL_FLIP_HORZ (0x01)   |

|  |  |   |
|--|--|---|
| CORACQ_PRM_EXT_TRIGGER_DURATION          |  | min = 0 $\mu$ s<br>max = 255 $\mu$ s<br>step = 1 $\mu$ s  |
| CORACQ_PRM_TIME_INTEGRATE_DELAY          |  | min = 0 $\mu$ s<br>max = 85899345 $\mu$ s<br>step = 1 $\mu$ s   |
| CORACQ_PRM_CAM_TRIGGER_DELAY             |  | min = 0 $\mu$ s<br>max = 85899345 $\mu$ s<br>step = 1 $\mu$ s   |
| CORACQ_PRM_SHAFT_ENCODER_LEVEL           |  | CORACQ_VAL_LEVEL_422 (0x2)  |
| CORACQ_PRM_LUT_NENTRIES                  | 8-bit/pixel component<br>10-bit/pixel component<br>12-bit/pixel component<br>14/16-bit/pixel component | 256 entries<br>1024 entries<br>4096 entries<br>0 entries  |
| CORACQ_PRM_EXT_FRAME_TRIGGER_SOURCE (*)  |  | min = 0<br>max = 7<br>step = 1  |
| CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE (*)   |  | min = 0<br>max = 5<br>step = 1  |
| CORACQ_PRM_EXT_TRIGGER_SOURCE (*)        |  | min = 0<br>max = 7<br>step = 1  |
| CORACQ_PRM_SHAFT_ENCODER_MULTIPLY        |  | min = 1<br>max = 32<br>step = (2 <sup>N</sup> )   |
| CORACQ_PRM_EXT_TRIGGER_DELAY             |  | min = 0<br>max = 16777215<br>step = 1   |
| CORACQ_PRM_EXT_TRIGGER_DELAY_TIME_BASE   |  | CORACQ_VAL_TIME_BASE_LINE_VALID (0x4)<br>CORACQ_VAL_TIME_BASE_LINE_TRIGGER (0x8)<br>CORACQ_VAL_TIME_BASE_SHAFT_ENCODER (0x40)<br>CORACQ_VAL_TIME_BASE_NS (0x80)   |
| CORACQ_PRM_COLOR_DECODER_ENABLE          | Mono<br>RGB<br>Bayer   | Not Available<br>TRUE<br>FALSE  |
| CORACQ_PRM_COLOR_DECODER_METHOD          | Bayer  | CORACQ_VAL_COLOR_DECODER_METHOD_1 (0x1)   |
| CORACQ_PRM_WB_GAIN                       | RGB<br>Bayer   | min = 100000<br>max = 900000<br>step = 1  |
| CORACQ_PRM_WB_GAIN_RED                   | RGB<br>Bayer   | min = 100000<br>max = 900000<br>step = 1  |
| CORACQ_PRM_WB_GAIN_GREEN                 | RGB<br>Bayer   | min = 100000<br>max = 900000<br>step = 1  |
| CORACQ_PRM_WB_GAIN_BLUE                  | RGB<br>Bayer   | min = 100000<br>max = 900000<br>step = 1  |
| CORACQ_PRM_EXT_TRIGGER_IGNORE_DELAY      |  | min = 0<br>max = 85899345<br>step = 1   |
| CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE (*) |  | min = 0<br>max = 6<br>step = 1  |
| CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE (*) |  | min = 0<br>max = 6<br>step = 1  |
| CORACQ_PRM_EXT_TRIGGER_SOURCE_STR        |  | [0] = Automatic<br>[1] = External Trigger #1<br>[2] = External Trigger #2<br>[3] = Board Sync #1<br>[4] = Board Sync #2<br>[5] = Software Trigger<br>[6] = External Trigger #3<br>[7] = External Trigger #4 |

|   |  |
|---|--|
| CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE_STR        | [0] = Automatic<br>[1] = Shaft Encoder Phase A<br>[2] = Shaft Encoder Phase B<br>[3] = Shaft Encoder Phase A & B<br>[4] = Board Sync #1<br>[5] = Board Sync #2   |
| CORACQ_PRM_VERTICAL_TIMEOUT_DELAY             | Not Available  |
| CORACQ_PRM_POEXP_ENABLE                       | TRUE<br>FALSE  |
| CORACQ_PRM_SHAFT_ENCODER_DIRECTION            | CORACQ_VAL_SHAFT_ENCODER_DIRECTION_IGNORE (0x00)<br>CORACQ_VAL_SHAFT_ENCODER_DIRECTION_FORWARD (0x01)<br>CORACQ_VAL_SHAFT_ENCODER_DIRECTION_REVERSE (0x02)   |
| CORACQ_PRM_LINE_TRIGGER_AUTO_DELAY            | CORACQ_VAL_LINE_TRIGGER_AUTO_DELAY_DISABLE (0x0)<br>CORACQ_VAL_LINE_TRIGGER_AUTO_DELAY_FREQ_MAX (0x2)  |
| CORACQ_PRM_TIME_STAMP_BASE                    | CORACQ_VAL_TIME_BASE_US (0x1)<br>CORACQ_VAL_TIME_BASE_LINE_VALID (0x4)<br>CORACQ_VAL_TIME_BASE_LINE_TRIGGER (0x8)<br>CORACQ_VAL_TIME_BASE_SHAFT_ENCODER (0x40)<br>CORACQ_VAL_TIME_BASE_100NS (0x200)                   |
| CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE_STR      | [0] = Disabled<br>[1] = External Frame Trigger<br>[2] = Reserved<br>[3] = External Trigger Ignore Region<br>[4] = Shaft Encoder Before Mult/Drop<br>[5] = Shaft Encoder After Mult/Drop<br>[6] = Internal Line Trigger |
| CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE_STR      | [0] = Disabled<br>[1] = External Frame Trigger<br>[2] = Reserved<br>[3] = External Trigger Ignore Region<br>[4] = Shaft Encoder Before Mult/Drop<br>[5] = Shaft Encoder After Mult/Drop<br>[6] = Internal Line Trigger |
| CORACQ_PRM_SHAFT_ENCODER_ORDER                | CORACQ_VAL_SHAFT_ENCODER_ORDER_AUTO (0x0)<br>CORACQ_VAL_SHAFT_ENCODER_ORDER_DROP_MULTIPLY (0x1)<br>CORACQ_VAL_SHAFT_ENCODER_ORDER_MULTIPLY_DROP (0x2)<br><br>* For auto mode, the order is multiply/drop.              |
| CORACQ_PRM_CAM_FRAMES_PER_TRIGGER             | Not Available  |
| CORACQ_PRM_LINE_INTEGRATE_TIME_BASE           | CORACQ_VAL_TIME_BASE_NS (0x80)   |
| CORACQ_PRM_EXT_TRIGGER_IGNORE_REGION_DURATION | min = 0 $\mu$ s<br>max = 6553 $\mu$ s<br>step = 1 $\mu$ s  |
| CORACQ_PRM_STROBE_DESTINATION (*)             | min = 0<br>max = 4<br>step = 1   |
| CORACQ_PRM_STROBE_DESTINATION_STR             | [0] = Automatic<br>[1] = Strobe #1<br>[2] = Strobe #2<br>[3] = Strobe #3<br>[4] = Strobe #4  |
| CORACQ_PRM_SHAFT_ENCODER_AVERAGING_ENABLE     | TRUE<br>FALSE  |
| CORACQ_PRM_SHAFT_ENCODER_AVERAGING_PULSES     | max 'N' = 8 (ie 2**N Pulses)   |
| CORACQ_PRM_SHAFT_ENCODER_AVERAGING_PERIOD_MIN | 50 nsec  |
| CORACQ_PRM_SHAFT_ENCODER_AVERAGING_PERIOD_MAX | 2000000 nsec   |
| CORACQ_PRM_HDR_ENABLE                         | Not Available  |

# ACQ Related Parameters

Table 11: Acquisition Related Parameters

| Parameter                    |             | Values   |
|------------------------------|-------------|--|
| CORACQ_PRM_LABEL             | Mono        | CXP Mono   |
|                              | RGB         | CXP Color RGB  |
| CORACQ_PRM_EVENT_TYPE        |             | CORACQ_VAL_EVENT_TYPE_START_OF_FRAME<br>CORACQ_VAL_EVENT_TYPE_END_OF_FRAME<br>CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER<br>CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC<br>CORACQ_VAL_EVENT_TYPE_FRAME_LOST<br>CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW<br>CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED<br>CORACQ_VAL_EVENT_TYPE_EXT_LINE_TRIGGER_TOO_SLOW<br>CORACQ_VAL_EVENT_TYPE_LINK_ERROR<br>CORACQ_VAL_EVENT_TYPE_SHAFT_ENCODER_REVERSE_COUNT_OVERFLOW<br>CORACQ_VAL_EVENT_TYPE_LINE_TRIGGER_TOO_FAST   |
| CORACQ_PRM_EVENT_TYPE_EX     |             | CORACQ_VAL_EVENT_TYPE_START_OF_FRAME<br>CORACQ_VAL_EVENT_TYPE_END_OF_FRAME<br>CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER<br>CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC<br>CORACQ_VAL_EVENT_TYPE_FRAME_LOST<br>CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW<br>CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED<br>CORACQ_VAL_EVENT_TYPE_EXT_LINE_TRIGGER_TOO_SLOW<br>CORACQ_VAL_EVENT_TYPE_LINK_ERROR<br>CORACQ_VAL_EVENT_TYPE_SHAFT_ENCODER_REVERSE_COUNT_OVERFLOW<br>CORACQ_VAL_EVENT_TYPE_LINE_TRIGGER_TOO_FAST<br>CORACQ_VAL_EVENT_TYPE_LINK_LOCK<br>CORACQ_VAL_EVENT_TYPE_LINK_UNLOCK |
| CORACQ_PRM_SIGNAL_STATUS     |             | CORACQ_VAL_SIGNAL_HSYNC_PRESENT<br>CORACQ_VAL_SIGNAL_VSYNC_PRESENT<br>CORACQ_VAL_SIGNAL_POWER_PRESENT<br>CORACQ_VAL_SIGNAL_POCP_ACTIVE<br>CORACQ_VAL_SIGNAL_POCP_ACTIVE_2<br>CORACQ_VAL_SIGNAL_POCP_ACTIVE_3<br>CORACQ_VAL_SIGNAL_POCP_ACTIVE_4<br>CORACQ_VAL_SIGNAL_LINK_LOCK<br>CORACQ_VAL_SIGNAL_LANE1_LOCK<br>CORACQ_VAL_SIGNAL_LANE2_LOCK<br>CORACQ_VAL_SIGNAL_LANE3_LOCK<br>CORACQ_VAL_SIGNAL_LANE4_LOCK<br>CORACQ_VAL_SIGNAL_DATA_LANES   |
| CORACQ_PRM_FLAT_FIELD_ENABLE | Mono        | TRUE / FALSE   |
|                              | RGB         | Not available  |
|                              | Bayer       |  |
| CORACQ_CAP_FLAT_FIELD_OFFSET | 8-bit Mono  | min = 0<br>max = 255<br>step = 1   |
|                              | 10-bit Mono | min = 0<br>max = 1023<br>step = 1  |
|                              | 12-bit Mono | min = 0<br>max = 4095<br>step = 1  |
|                              | 14-bit Mono | min = 0<br>max = 16383<br>step = 1   |
|                              | 16-bit Mono | Not Available  |

|  |             |   |
|--|-------------|---|
| CORACQ_CAP_FLAT_FIELD_GAIN                     | 8-bit Mono  | min = 0<br>max = 255<br>step = 1  |
|  | 10-bit Mono | min = 0<br>max = 1023<br>step = 1   |
|  | 12-bit Mono | min = 0<br>max = 4095<br>step = 1   |
|  | 14-bit Mono | min = 0<br>max = 16383<br>step = 1  |
|  | 16-bit Mono | Not Available   |
| CORACQ_CAP_FLAT_FIELD_GAIN_DIVISOR             | 8-bit Mono  | 0x80  |
|  | 10-bit Mono | 0x200   |
|  | 12-bit Mono | 0x800   |
|  | 14-bit Mono | 0x2000  |
|  | 16-bit Mono | Not Available   |
| CORACQ_PRM_FLAT_FIELD_PIXEL_REPLACEMENT_METHOD |             | CORACQ_VAL_FLAT_FIELD_PIXEL_REPLACEMENT_METHOD_2<br>(Pixel replacement is done by averaging the 2 neighborhood pixels. When one of the neighbors is not available (border image pixels, the pixel is simply replaced with the available neighbor) |
| CORACQ_PRM_FLAT_FIELD_SET_SELECT               |             | min = 0<br>max = 16<br>step = 1   |
| CORACQ_PRM_TIME_STAMP                          |             | Available   |
| CORACQ_PRM_IMAGE_FILTER_ENABLE                 |             | Not Available   |
| CORACQ_PRM_SHAFT_ENCODER_REVERSE_COUNT         |             | Max = 65536 ticks   |
| CORACQ_PRM_META_DATA                           |             | CORACQ_VAL_META_DATA_PER_LINE_RIGHT (0x2)   |
| CORACQ_PRM_SHAFT_ENCODER_STATUS                |             | CORACQ_VAL_SHAFT_ENCODER_STATUS_DIRECTION_FORWARD /<br>CORACQ_VAL_SHAFT_ENCODER_STATUS_DIRECTION_REVERSE (0x1)<br>CORACQ_VAL_SHAFT_ENCODER_STATUS_TOO_SLOW (0x2)<br>CORACQ_VAL_SHAFT_ENCODER_STATUS_REVERSE_COUNT_OVERFLOW<br>(0x4)               |
| CORACQ_PRM_SHAFT_ENCODER_COUNT                 |             | Available   |

## Transfer Related Capabilities

| Capability                          | Values                                    |
|-------------------------------------|---|
| CORXFER_CAP_NB_INT_BUFFERS          | CORXFER_VAL_NB_INT_BUFFERS_AUTO (0x2)     |
| CORXFER_CAP_MAX_XFER_SIZE           | 4294967040 Bytes                          |
| CORXFER_CAP_MAX_FRAME_COUNT         | 16777215 Frames                           |
| CORXFER_CAP_COUNTER_STAMP_AVAILABLE | FALSE                                     |
| CORXFER_CAP_TRANSFER_SYNC           | CORXFER_VAL_TRANSFER_SYNC_SUPPORTED (0x1) |

Table 12: Transfer Related Capabilities

## Transfer Related Parameters

Table 13: Transfer Related Parameters

| Parameter   | Values   |
|---|--|
| CORXFER_PRM_EVENT_TYPE<br>CORXFER_PRM_EVENT_TYPE_EX | CORXFER_VAL_EVENT_TYPE_START_OF_FRAME<br>CORXFER_VAL_EVENT_TYPE_END_OF_FRAME<br>CORXFER_VAL_EVENT_TYPE_END_OF_LINE<br>CORXFER_VAL_EVENT_TYPE_END_OF_NLINES<br>CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER   |
| CORXFER_PRM_START_MODE                              | CORXFER_VAL_START_MODE_ASYNCHRONOUS (0x0)<br>CORXFER_VAL_START_MODE_SYNCHRONOUS (0x1)<br>CORXFER_VAL_START_MODE_HALF_ASYNCHRONOUS (0x2)<br>CORXFER_VAL_START_MODE_SEQUENTIAL (0x3)                     |
| CORXFER_PRM_CYCLE_MODE                              | CORXFER_VAL_CYCLE_MODE_ASYNCHRONOUS (0x0)<br>CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_WITH_TRASH (0x2)<br>CORXFER_VAL_CYCLE_MODE_OFF (0x3)<br>CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_NEXT_EMPTY_WITH_TRASH (0x5) |
| CORXFER_PRM_FLIP                                    | CORXFER_VAL_FLIP_OFF (0x0)<br>CORXFER_VAL_FLIP_VERT (0x2)  |
| CORXFER_PRM_INT_BUFFERS                             | * Depends on acquired image size.<br>By default driver will optimize the number of on-board buffers.   |
| CORXFER_PRM_EVENT_COUNT_SOURCE                      | CORXFER_VAL_EVENT_COUNT_SOURCE_DST (0x1)<br>CORXFER_VAL_EVENT_COUNT_SOURCE_SRC (0x2)   |
| CORXFER_PRM_BUFFER_TIMESTAMP_MODULE                 | CORXFER_VAL_BUFFER_TIMESTAMP_MODULE_ACQ (0x1)<br>CORXFER_VAL_BUFFER_TIMESTAMP_MODULE_XFER (0x13)   |
| CORXFER_PRM_BUFFER_TIMESTAMP_EVENT (ACQ Related)    | CORACQ_VAL_EVENT_TYPE_START_OF_FRAME (0x80000)<br>CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER (0x1000000)   |
| CORXFER_PRM_BUFFER_TIMESTAMP_EVENT (XFER Related)   | CORXFER_VAL_EVENT_TYPE_END_OF_FRAME (0x800000)   |
| CORXFER_PRM_LINE_MERGING                            | CORXFER_VAL_LINE_MERGING_AUTO (0x0)<br>CORXFER_VAL_LINE_MERGING_OFF (0x2)  |

## General Outputs #1: Related Capabilities (for GIO Module #0)

Outputs available on connector J1 and J7.

Table 14: GIO-0 Related Capabilities

| Capability              | Values   |
|-------------------------|--|
| CORGIO_CAP_IO_COUNT     | 8 I/Os   |
| CORGIO_CAP_DIR_OUTPUT   | 0xff   |
| CORGIO_CAP_DIR_TRISTATE | 0xff   |
| CORGIO_CAP_EVENT_TYPE   | Not Available  |
| CORGIO_CAP_READ_ONLY    | 0x01 (* depends on strobe outputs reserved for acquisition device) |

## General Outputs #1: Related Parameters (for GIO Module #0)

Table 15: GIO-0 Related Parameters

| Parameter              | Values                              |
|------------------------|-------------------------------------|
| CORGIO_PRM_LABEL       | General Outputs #1                  |
| CORGIO_PRM_DEVICE_ID   | 0                                   |
| CORGIO_PRM_OUTPUT_TYPE | CORGIO_VAL_OUTPUT_TYPE_LVTTL (0x20) |
| CORGIO_PRM_CONNECTOR   | CORGIO_VAL_CONNECTOR_1 (0x1)        |

## General Inputs #1: Related Capabilities (for GIO Module #1)

Inputs available on connector J1 and J7.

Table 16: GIO-1 Related Capabilities

| Capability              | Values  |
|-------------------------|---|
| CORGIO_CAP_IO_COUNT     | 4 I/Os  |
| CORGIO_CAP_DIR_OUTPUT   | 0x0   |
| CORGIO_CAP_DIR_TRISTATE | 0x0   |
| CORGIO_CAP_EVENT_TYPE   | CORGIO_VAL_EVENT_TYPE_RISING_EDGE (0x1)<br>CORGIO_VAL_EVENT_TYPE_FALLING_EDGE (0x2) |
| CORGIO_CAP_READ_ONLY    | 0x03 (* depends on external trigger inputs reserved for acquisition device)         |

## General Inputs #1: Related Parameters (for GIO Module #1)

Table 17: GIO-1 Related Parameters

| Parameter              | Values  |
|------------------------|---|
| CORGIO_PRM_LABEL       | General Inputs #1   |
| CORGIO_PRM_DEVICE_ID   | 1   |
| CORGIO_PRM_INPUT_LEVEL | CORGIO_VAL_INPUT_LEVEL_TTL (0x1)<br>CORGIO_VAL_INPUT_LEVEL_422 (0x2)<br>CORGIO_VAL_INPUT_LEVEL_24VOLTS (0x8)<br>CORGIO_VAL_INPUT_LEVEL_12VOLTS (0x40) |
| CORGIO_PRM_CONNECTOR   | CORGIO_VAL_CONNECTOR_1 (0x1)  |

## Bidirectional General I/Os: Related Capabilities (for GIO Module #2)

These I/Os are available on connector J9

Table 18: GIO-1 Related Parameters

| Capability              | Values  |
|-------------------------|---|
| CORGIO_CAP_IO_COUNT     | 8 I/Os  |
| CORGIO_CAP_DIR_OUTPUT   | 0xff  |
| CORGIO_CAP_DIR_TRISTATE | 0xff  |
| CORGIO_CAP_EVENT_TYPE   | Not Available   |
| CORGIO_CAP_READ_ONLY    | 0x03 (* depends on board syncs reserved for acquisition device) |



## Bidirectional General I/Os: Related Parameters (for GIO Module #2)

Table 19: GIO-2 Related Parameters

| Parameter              | Values                              |
|------------------------|-------------------------------------|
| CORGIO_PRM_LABEL       | Bidirectional General I/Os #1       |
| CORGIO_PRM_DEVICE_ID   | 2                                   |
| CORGIO_PRM_OUTPUT_TYPE | CORGIO_VAL_OUTPUT_TYPE_LVTTL (0x20) |
| CORGIO_PRM_INPUT_LEVEL | CORGIO_VAL_INPUT_LEVEL_LVTTL (0x20) |
| CORGIO_PRM_CONNECTOR   | CORGIO_VAL_CONNECTOR_2 (0x2)        |

# Sapera Servers and Resources

A Sapera Server is an abstract representation of a physical device like a frame-grabber or camera. When using the SapAcquisition or SapAcqDevice constructors, the location parameter specifies the server to use to create the object. Use the Sapera Configuration utility to find the names and indices of all Sapera servers in your system.

In Sapera LT all frame grabbers are configured using the SapAcquisition class. All CXP cameras are GenCP compliant and are configured in Sapera LT using the SapAcqDevice class.



**Note:** Currently, CXP cameras do not have their own server, therefore it is available under the Xtium\_CXP server. For example, in CamExpert the Xtium server displays both the frame grabber and camera resources.

## The following table describes the Xtium-CXP PX8 board

Table 20: Xtium-CXP PX8 - Servers and Resources

| Servers                        |                    | Resources   |              |   |
|--------------------------------|--------------------|---|--------------|---|
| Name                           | Type               | Name  | Index        | Description                                 |
| Xtium-CXP_PX8_1<br>(1 Camera)  | Acquisition Module | CXP Mono #1   | 0            | CXP Mono Camera                             |
|                                |                    | CXP Color RGB #1  | 1            | CXP RGB Camera                              |
|                                |                    | CXP Bayer #1  | 2            | CXP Bayer Camera                            |
|                                | Acquisition Device | <Device Name><br>[SN: <Serial Number>]<br>*Name of camera | 0            | CXP Camera connected to respective Camera # |
| Xtium-CXP_PX8_1<br>(2 Cameras) | Acquisition Module | CXP Mono #1   | 0            | CXP Mono Camera                             |
|                                |                    | CXP Mono #2   | 1            |   |
|                                |                    | CXP Color RGB #1  | 2            | CXP RGB Camera                              |
|                                |                    | CXP Color RGB #2  | 3            |   |
|                                |                    | CXP Bayer #1  | 4            | CXP Bayer Camera                            |
|                                |                    |   | CXP Bayer #2 | 5   |
|                                | Acquisition Device | <Device Name><br>[SN: <Serial Number>]<br>*Name of camera | 0<br>1       | CXP Camera connected to respective Camera # |
| Xtium-CXP_PX8_1<br>(3 Cameras) | Acquisition Module | CXP Mono #1   | 0            | CXP Mono Camera                             |
|                                |                    | CXP Mono #2   | 1            |   |
|                                |                    | CXP Mono #3   | 2            |   |
|                                |                    | CXP Color RGB #1  | 3            | CXP RGB Camera                              |
|                                |                    | CXP Color RGB #2  | 4            |   |
|                                |                    | CXP Color RGB #3  | 5            |   |
|                                |                    | CXP Bayer #1  | 6            | CXP Bayer Camera                            |
|                                |                    | CXP Bayer #2  | 7            |   |
|                                |                    |   | CXP Bayer #3 | 8   |
|                                | Acquisition Device | <Device Name><br>[SN: <Serial Number>]<br>*Name of camera | 0<br>1<br>2  | CXP Camera connected to respective Camera # |

|                                |                    |                               |    |   |
|--------------------------------|--------------------|-------------------------------|----|---|
| Xtium-CXP_PX8_1<br>(4 Cameras) | Acquisition Module | CXP Mono #1                   | 0  | CXP Mono Camera                             |
|                                |                    | CXP Mono #2                   | 1  |   |
|                                |                    | CXP Mono #3                   | 2  |   |
|                                |                    | CXP Mono #4                   | 3  |   |
|                                |                    | CXP Color RGB #1              | 4  | CXP RGB Camera                              |
|                                |                    | CXP Color RGB #2              | 5  |   |
|                                |                    | CXP Color RGB #3              | 6  |   |
|                                |                    | CXP Color RGB #4              | 7  |   |
|                                |                    | CXP Bayer #1                  | 8  | CXP Bayer Camera                            |
|                                |                    | CXP Bayer #2                  | 9  |   |
|                                |                    | CXP Bayer #3                  | 10 |   |
|                                |                    | CXP Bayer #4                  | 11 |   |
|                                | Acquisition Device | <Device Name>                 | 0  | CXP Camera connected to respective Camera # |
|                                |                    | [SN: <Serial Number>]         | 1  |   |
|                                |                    | *Name of camera               | 2  |   |
|                                |                    |                               | 3  |   |
| All                            | GIO Module         | General Outputs #1            | 0  | 8 General Outputs                           |
|                                |                    | General Inputs #1             | 1  | 4 General Inputs                            |
|                                |                    | Bidirectional General I/Os #1 | 2  | 8 Bidirectional General I/Os                |

# Technical Specifications

## Xtium-CXP PX8 Board Specifications

### Digital Video Input & Controls

Table 21: Board Specifications

|   |  |
|---|--|
| Input Type  | CoaXPress Specifications Rev 1.0, 1.1 and 1.1.1 compatible   |
| Common Pixel Formats  | 8, 10, 12, 14 and 16-bit mono, 8, 10 and 12-bit RGB and Bayer  |
| Scanning  | Area scan and Line scan  |
| Resolution<br><i>note: these are Xtium-CXP PX8 maximums, not CoaXPress specifications</i> | Horizontal Minimum:<br>32 pixels per lane<br>Horizontal Maximum:<br>64kBs/line (Mono or Color)<br>Vertical Minimum:<br>1 line<br>Vertical Maximum:<br>up to 65536 lines—for area scan sensors<br>infinite line count—for linescan sensors  |
| Bit Transfer Rate   | 1.250 Gbps, 2.500 Gbps, 3.125 Gbps, 5.000 Gbps and 6.250 Gbps  |
| Image Buffer  | Available with 1 GB  |
| Bandwidth to Host System  | Approximately 3.4 GB/s (maximum obtained is dependent on firmware loaded and PC characteristics)   |
| Controls  | Compliant with Teledyne DALSA Trigger-to-Image Reliability framework<br>Comprehensive event notifications<br>Timing control logic for camera triggers and strobe signals<br>4 opto-coupled general inputs where 2 are shared acquisition trigger inputs (RS-422/TTL/12V/24V)<br>Trigger inputs are programmable as active high or low (edge or level trigger, at maximum input frequency of 100 KHz)<br>External trigger latency less than 100 nsec<br>8 LVTTTL general Outputs where 1 is shared as Strobe Output<br>Quadrature (phase A & B) shaft encoder inputs for external web synchronization: RS-422 input maximum frequency is 5 MHz<br>Supports multi-camera synchronization of 2 to 4 boards<br>I/O available on a DH60-27P connector (J1) and on 26-pin SHF-113-01-L-D-RA (J7) |
| Processing<br><i>Dependent on user loaded firmware configuration</i>                      | Output Lookup Table<br>Flat Field/Flat Line Correction<br>Bayer Mosaic Filter  |

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# Host System Requirements

## Xtium-CXP PX8 Dimensions

Approximately 6 in. (14 cm) wide by 4 in. (10 cm) high

## General System Requirements for the Xtium-CXP PX8

- PCI Express Gen2 x8 slot compatible; (will work in Gen1 x8 slot with reduced bandwidth to host)
- On some computers the Xtium-CXP PX8 may function installed in a x16 slot. The computer documentation or direct testing by the user is required.
- Xtium-CXP PX8 operates correctly when installed in a multi-processor system (including Hyper-Threading multi-core processors).

## Operating System Support

Windows 7, Windows 8 and Windows 10, each in either 32-bit or 64-bit

## Environment

Table 22: Environment Specifications

|                      |   |
|----------------------|---|
| Ambient Temperature: | 10° to 50°C (operation)<br>-40° to 75°C (storage)           |
| Relative Humidity:   | 5% to 90% non-condensing (operating)<br>0% to 95% (storage) |
| MTBF @40°C           | 74.0 years  |



Note: Ensure adequate airflow for proper functioning of the board across the entire temperature range of 10 – 50°C. We recommend airflow measuring 80 LFM (linear feet per minute) across the surface of the board.

## Power Requirements while grabbing

Table 23: Power Specifications

|       |       |
|-------|-------|
| +12V: | 1.38A |
|-------|-------|

# EMI Certifications



## EC & FCC DECLARATION OF CONFORMITY

We :  
 Teledyne DALSA inc.  
 880 Rue McCaffrey  
 St-Laurent, Québec  
 Canada H4T 2C7

Declare under sole legal responsibility that the following products conform to the protection requirements of council directive 2004/108/EC (2014/30/EU after April 2016) on the approximation of the laws of member states relating to electromagnetic compatibility and are CE-marked accordingly:

Xtium-CXP PX8

The products to which this declaration relates are in conformity with the following relevant harmonized standards, the reference numbers of which have been published in the Official Journal of the European Communities:

|                              |  |
|------------------------------|--|
| EN55032 (2012)               | Electromagnetic compatibility of multimedia equipment — Emission requirements  |
| EN55011 (2009) with A1(2010) | Industrial, scientific and medical equipment — Radio-frequency disturbance characteristics — Limits and methods of measurement |
| EN 61326-1 (2013)            | Electrical equipment for measurement, control and laboratory use — EMC requirements — Part 1: General requirements             |
| EN 55024 (2010)              | Information technology equipment — Immunity characteristics — Limits and methods of measurement                                |

Further declare under our sole legal responsibility that the product listed also conforms to the following international standards:

|          |  |
|----------|--|
| CFR 47   | part 15 (2008), subpart B, for a class A product. Limits for digital devices   |
| ICES-003 | Information Technology Equipment (ITE) — Limits and Methods of Measurement   |
| CISPR 11 | Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement |
| CISPR 32 | Electromagnetic compatibility of multimedia equipment - Emission requirements  |

Note: this product is intended to be a component of a larger system.

Waterloo, Canada

2016-10-25

Location

Date

Hank Helmond.  
 Director, Quality Assurance

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Figure 39: EMI Certifications

# Connector and Switch Locations

## Xtium-CXP PX8 Board Layout Drawing

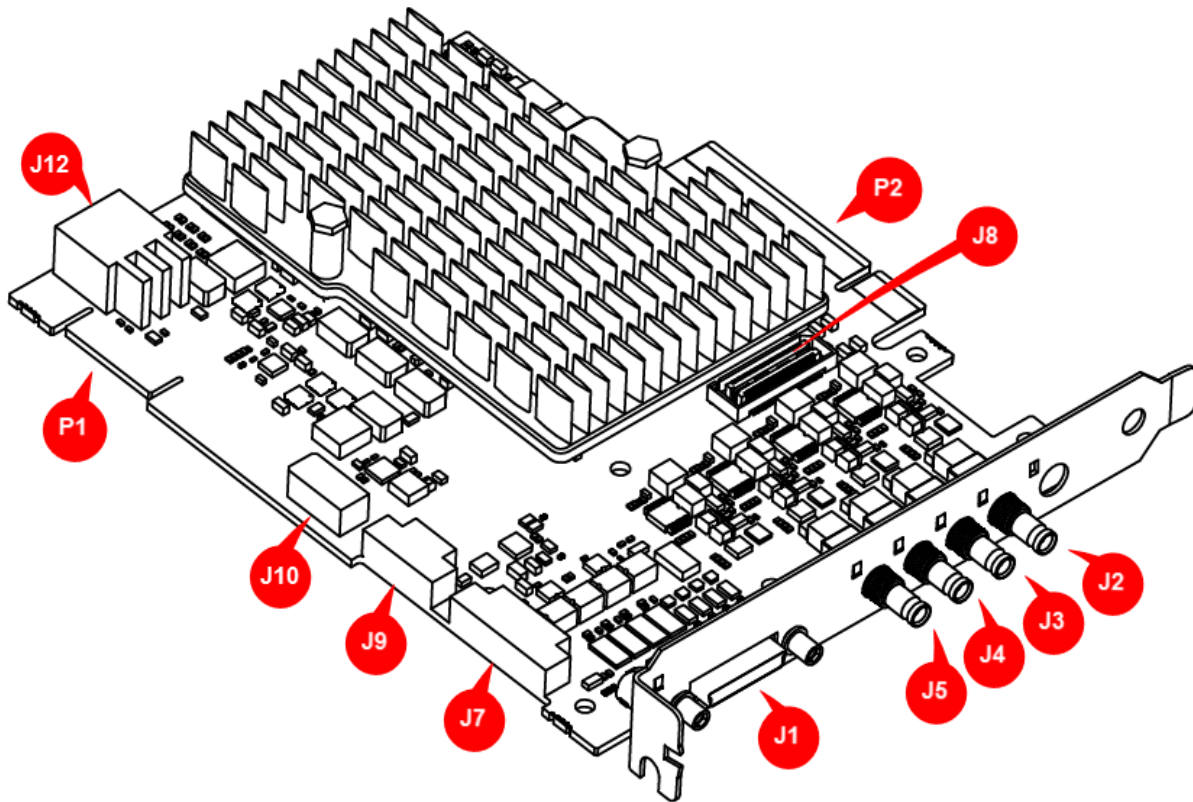


Figure 40: Board Layout

### Connector / LED Description List

The following table lists components on the Xtium-CXP PX8 board. Detailed information concerning the connectors/LEDs follows this summary table.

Table 24: Board Connector List

| Location                       | Description   | Location            | Description  |
|--------------------------------|---|---------------------|--|
| <a href="#">J1</a>             | External I/O Signals connector (DH60-27P)                 | <a href="#">J9</a>  | Multi Board Sync   |
| <a href="#">D1</a>             | Boot-up/PCIe Status LED (refer to text)                   | <a href="#">J12</a> | PC power to J1   |
| <a href="#">J2, J3, J4, J5</a> | Camera CXP Input Connectors                               | P1                  | PCIe x8 computer bus connector (Gen2 compliant slot preferred) |
| <a href="#">D3, D4, D5, D6</a> | Camera CXP status LEDs                                    | P2                  | Reserved   |
| <a href="#">J7</a>             | Internal I/O Signals connector (26-pin SHF-113-01-L-D-RA) | J8/J10              | Reserved   |

# Connector and Switch Specifications

## Xtium-CXP PX8 End Bracket Detail

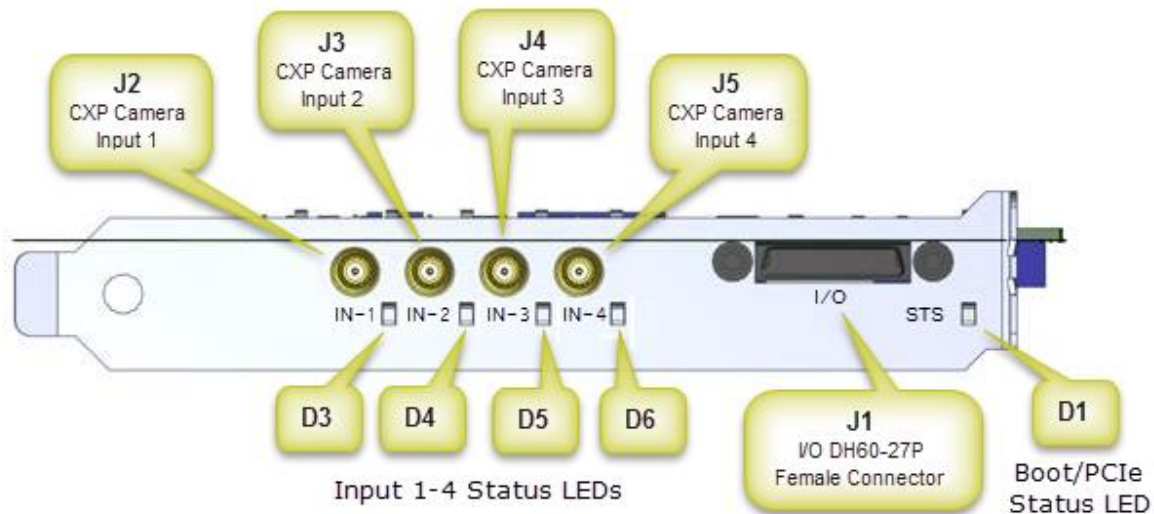


Figure 41: End Bracket Details

The hardware installation process is completed with the connection of a supported camera to the Xtium-CXP PX8 board using a DIN 1.0/2.3 CXP cable. (see the CoaXPress Cables section).

- The Xtium-CXP PX8 board supports up to 4 CoaXPress camera output.
- 1 Camera connection:
  - Connect the camera to the J2, J3, J4 and J5 connectors. Order to which the cables are connected to the camera does not matter.
- 2 Camera connection:
  - Connect Camera #1 to J2/J3 and Camera #2 to J4/J5. Order to which the cables are connected to the camera does not matter.
- 3 Camera connection:
  - Connect Camera #1 to J2, Camera #2 to J3 and Camera #3 to J4/J5 Order to which the cables are connected to the camera #3 does not matter.
- 4 Camera connection:
  - Connect Camera #1 to J2, Camera #2 to J3, Camera #3 to J4 and Camera #4 to J5.



## Status LEDs Functional Descriptions

Three LED indicators, mounted on the board bracket, provide information on board and connection status as per the tables below.

**D1: Boot-up/PCIe Status LED** — Provides general board status information

**D3, D4, D5, D6: CoaXPress status LED** — Indicates status for J2, J3, J4 and J5 respectively.

### *D1: Boot-up/PCIe Status LED*

Table 25: D1 Boot-up/PCIe Status LED

| Color  | State    | Description  |
|--------|----------|--|
| Red    | Solid    | FPGA firmware not loaded                                     |
| Green  | Solid    | Normal FPGA firmware loaded, Gen2 speed, link width x8       |
| Green  | Flashing | Normal FPGA firmware loaded, Gen1 speed, link width x8       |
| Yellow | Solid    | Normal FPGA firmware loaded, Gen2 speed, link width not x8   |
| Yellow | Flashing | Normal FPGA firmware loaded, Gen1 speed, link width not x8   |
| Blue   | Solid    | Safe FPGA firmware loaded, Gen2 speed                        |
| Blue   | Flashing | Safe FPGA firmware loaded, Gen1 speed                        |
| Red    | Flashing | PCIe Training Issue – Board will not be detected by computer |

### *D3, D4, D5, D6: CoaXPress Status LED*

The Xtium-CXP PX8 implements the mandatory LED states defined by the CoaXPress Specification v1.1.

This LED status table reflects activity on input connectors J2, J3, J4 and J5.

Table 26: Camera CXP Status LED

| LED State                    | Description   |
|------------------------------|---|
| Off                          | No power, driver not started or Backup FPGA running?  |
| Slow Pulse Red               | Driver running, but nothing connected. Only if PoCXP is disabled.                               |
| Fast Flashing Green / Orange | Connection detection in progress, PoCXP enabled.  |
| Fast Flashing Orange         | Connection detection in progress, PoCXP disabled.   |
| Solid Red                    | PoCXP over-current.   |
| Solid Green                  | Connected, but no data being transferred.   |
| Fast Flashing Green          | Connected, data being transferred.  |
| Fast Flashing Red            | System error:<br>If PoCXP is enabled, 12V not detected. Make sure PC power is connected to J12. |

## J1: External I/O Signals Connector (Female DH60-27P)

## J7: Internal I/O Signals Connector (26-pin SHF-113-01-L-D-RA)



**Warning:** J1 and J7 have the same pinout assignment. Signals are routed to both connectors directly from their internal circuitry. Therefore never connect both J1 and J7 to external devices at the same time.

Table 27: DH60-27P/ SHF-113-01-L-D-RA Connector Signals

| Description   | Pin # | Pin # | Description                                  |
|---|-------|-------|--|
| Ground  | 1     | 15    | External Trigger Input 3/General Input 3 (+) |
| RS-422 Shaft Encoder Phase A (-)  | 2     | 16    | External Trigger Input 4/General Input 4 (+) |
| RS-422 Shaft Encoder Phase A (+)<br>(see note 3)                        | 3     | 17    | External Trigger Input 4/General Input 4 (-) |
| Ground  | 4     | 18    | External Trigger Input 3/General Input 3 (-) |
| RS-422 Shaft Encoder Phase B (-)  | 5     | 19    | Power Output 5 Volts, 100mA max              |
| RS-422 Shaft Encoder Phase B (+)  | 6     | 20    | External Trigger Input 2/General Input 2 (-) |
| External Trigger Input 1/General Input 1 (-)                            | 7     | 21    | Strobe 3 / General Output 3                  |
| External Trigger Input 1/General Input 1 (+)                            | 8     | 22    | Strobe 4 / General Output 4                  |
| External Trigger Input 2/General Input 2 (+)                            | 9     | 23    | General Output 5                             |
| Ground  | 10    | 24    | General Output 6                             |
| Strobe 1 / General Output 1<br>(See note 2)                             | 11    | 25    | General Output 7                             |
| Strobe 2 / General Output 2   | 12    | 26    | General Output 8                             |
| Ground  | 13    | 27    | NC   |
| Power Output 12 Volts, 350mA max<br>(from Aux Power Connector, see J12) | 14    |       |  |

### **Note 1: General Inputs / External Trigger Inputs Specifications**

Each of the four General Inputs are opto-coupled and able to connect to differential or single ended source signals. General Inputs can also act as External Trigger Inputs. See "Board Information" user settings. These inputs generate individual interrupts and are read by the Sapera application. The following figure is typical for each General Input.

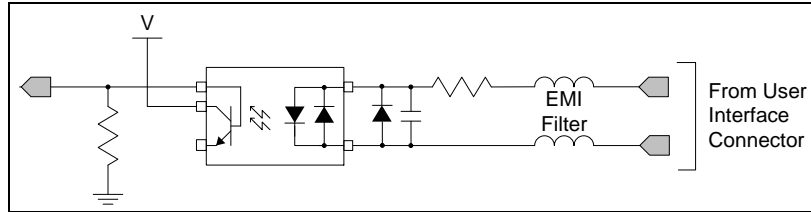


Figure 42: General Inputs Electrical Diagram

#### **Input Details:**

- Maximum input voltage is 26V.
- Maximum input signal frequency is 100 KHz.
- Each input has a 649-ohm series resistor on the opto-coupler input.
- The 0.01uF capacitor provide high frequency noise filtering.
- Minimum current is dependent on input voltage applied:  $I_{optoin(min)} = (V_{optoin} - 0.5)/649\Omega$
- The switch point is software programmable to support differential RS-422 or single ended TTL, 12V or 24V input signals.

#### **For External Trigger usage:**

- Input signal is "debounced" to ensure that no voltage glitch is detected as a valid transition. This debounce circuit time constant can be programmed from 1 $\mu$ s to 255 $\mu$ s. Any pulse smaller than the programmed value is blocked and therefore not seen by the board. If no debounce value is specified (value of 0 $\mu$ s), the minimum value of 1 $\mu$ s will be used.
- Refer to Sapera parameters:  
CORACQ\_PRM\_EXT\_TRIGGER\_SOURCE  
CORACQ\_PRM\_EXT\_TRIGGER\_ENABLE  
CORACQ\_PRM\_EXT\_TRIGGER\_LEVEL  
CORACQ\_PRM\_EXT\_FRAME\_TRIGGER\_LEVEL  
CORACQ\_PRM\_EXT\_TRIGGER\_DETECTION  
CORACQ\_PRM\_EXT\_TRIGGER\_DURATION
- See also \*.cvi file entries:  
External Trigger Level, External Frame Trigger Level, External Trigger Enable, External Trigger Detection.
- External Trigger Input 2 used for two pulse external trigger with variable frame length line scan acquisition.

## Trigger Signal Total Delay

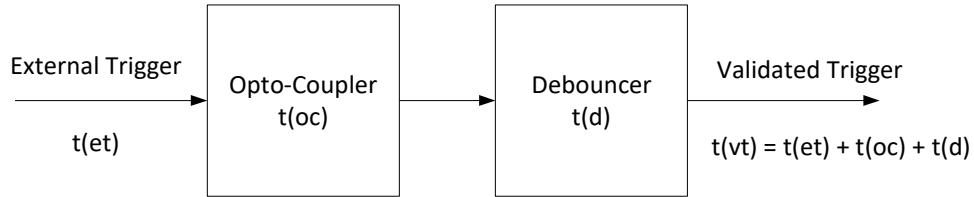


Figure 43: External Trigger Input Validation & Delay

Table 28: External Trigger Timing Specifications

|     |  |
|-----|--|
| Let | $t(et)$ = time of external trigger in $\mu s$<br>$t(oc)$ = time opto-coupler takes to change state (time varies dependent on input voltage)<br>$t(d)$ = user set debounce duration from 1 to 255 $\mu s$<br>$t(vt)$ = time of validated trigger in $\mu s$ |
|-----|--|



**Note:** Teledyne DALSA recommends using the fastest transition to minimize the time it takes for the opto-coupler to change state.

If the duration of the external trigger is  $> t(oc) + t(d)$ , then a valid acquisition trigger is detected.

It is possible to emulate an external trigger using the software trigger which is generated by a function call from an application.

Table 29: Input Switching Points and Propagation Delay

| Trigger Level | Switch Point | Propagation Delay<br>$t(oc)$<br>(rising edge signal $\uparrow$ ) | Propagation Delay<br>$t(oc)$<br>(falling edge signal $\downarrow$ ) |
|---------------|--------------|--|---|
| <b>RS-422</b> | 1.6V         | 1.75 $\mu s$   | 5.5 $\mu s$   |
| <b>TTL</b>    | 1.6V         | 1.75 $\mu s$   | 5.5 $\mu s$   |
| <b>12V</b>    | 6V           | 2.6 $\mu s$  | 2.6 $\mu s$   |
| <b>24V</b>    | 12V          | 1.9 $\mu s$  | 3.1 $\mu s$   |

## Block Diagram: Connecting External Drivers to General Inputs on J1

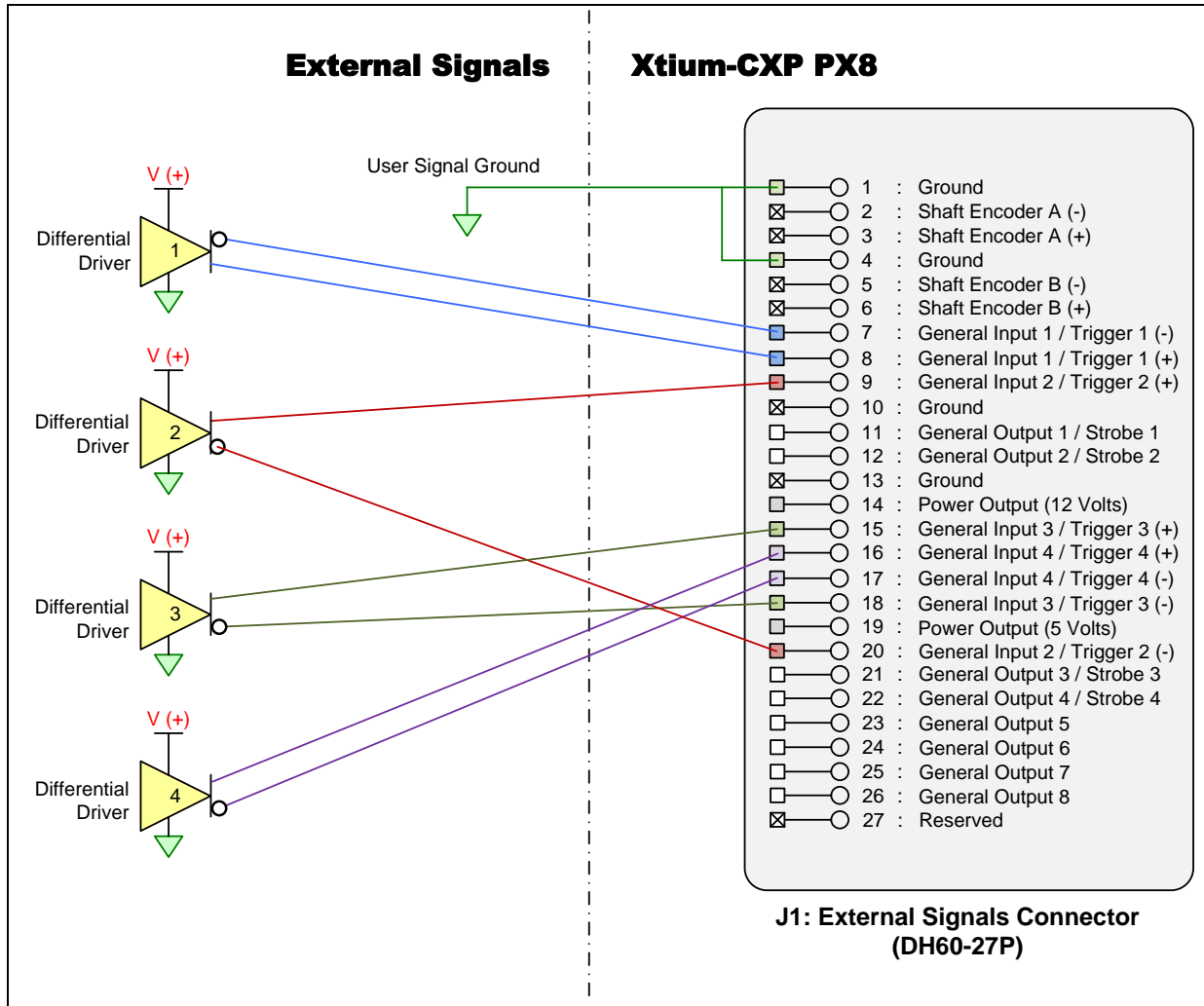


Figure 44: External Signals Connection Diagram

### External Driver Electrical Requirements

The Xtium-CXP allows user selected (software programmable) input switching points to support differential (RS-422) input signals and single ended (TTL, 12V or 24V) input signals. The following table defines the external signal voltage requirements from the driver circuits connected to the Xtium external inputs.

Table 30: External Driver Electrical Requirements

| Input Level | Description                      | MIN    | MAX     |
|-------------|----------------------------------|--------|---------|
| RS-422      | Output Voltage High ( $V_{OH}$ ) | 2.4 V  | 13.0 V  |
|             | Output Voltage Low ( $V_{OL}$ )  | -2.4 V | -13.0 V |
| TTL         | Output Voltage High ( $V_{OH}$ ) | 2.4 V  | 5.5 V   |
|             | Output Voltage Low ( $V_{OL}$ )  | 0 V    | 0.8 V   |
| 12V         | Output Voltage High ( $V_{OH}$ ) | 9 V    | 13.2 V  |
|             | Output Voltage Low ( $V_{OL}$ )  | 0 V    | 3 V     |
| 24V         | Output Voltage High ( $V_{OH}$ ) | 18 V   | 26.4 V  |
|             | Output Voltage Low ( $V_{OL}$ )  | 0 V    | 6 V     |

## Note 2: General Outputs /Strobe Output Specifications

Each of the four General Outputs are TTL (3.3V) compatible. General Outputs 1, 2,3 and 4 can also function as the Strobe Output controlled by Sapera strobe control functions. See "Board Information" user settings. The following figure is typical for each General Output.

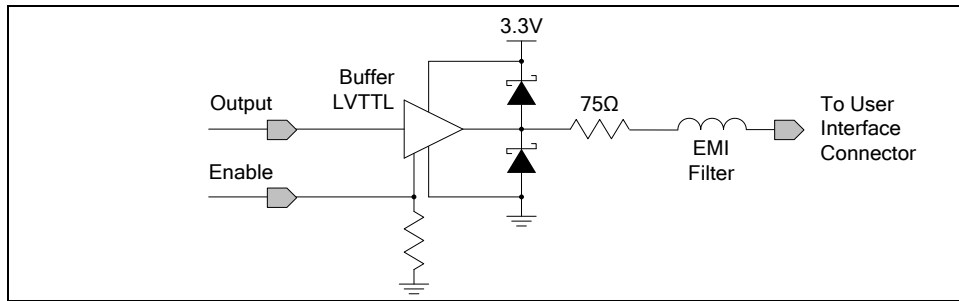


Figure 45: General Outputs Electrical Diagram

### Output Details:

- Each output has a 75-ohm series resistor
- The 2 diodes protect the LVTTL buffer against overvoltage
- Each output is a tri-state driver, enabled by software
- Minimum guaranteed output current is +/- 24mA @ 3.3V
- Maximum output current is 50mA
- Maximum short circuit output current is 44mA
- Minimum voltage for output level high is 2.4V, while maximum voltage for output low is 0.55V
- Maximum output switching frequency is limited by driver and register access on the PCIe bus.

### For Strobe Usage:

- Refer to Sapera Strobe Methods parameters:  
CORACQ\_PRM\_STROBE\_ENABLE  
CORACQ\_PRM\_STROBE\_POLARITY  
CORACQ\_PRM\_STROBE\_LEVEL  
CORACQ\_PRM\_STROBE\_METHOD  
CORACQ\_PRM\_STROBE\_DELAY  
CORACQ\_PRM\_STROBE\_DURATION  
CORACQ\_PRM\_STROBE\_DESTINATION
- See also \*.cvi file entries:  
Strobe Enable, Strobe Polarity, Strobe Level, Strobe Method, Strobe Delay, Strobe Duration.

## Block Diagram: Connecting External Receivers to the General Outputs

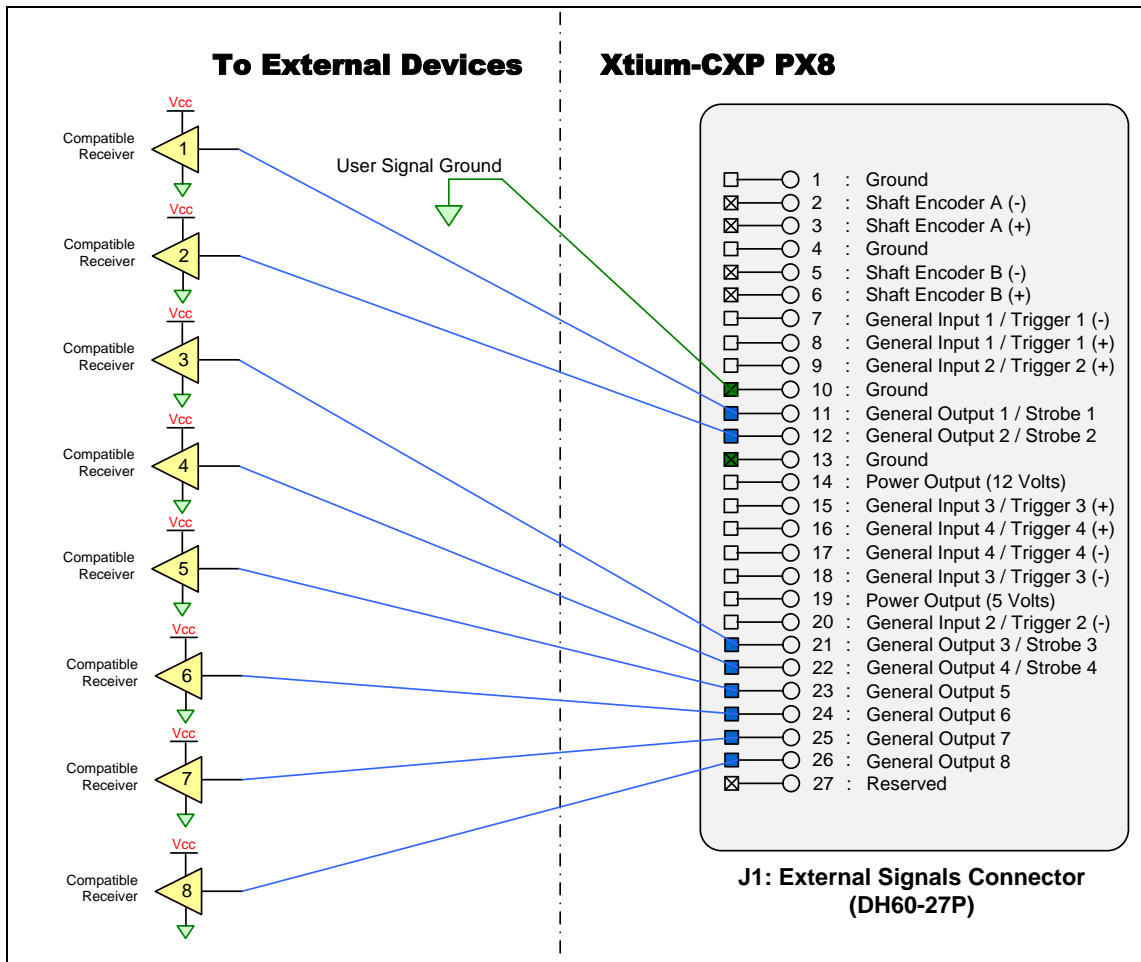


Figure 46: Output Signals Connection Diagram

### External Receiver Electrical Requirements

- Xtium General Outputs are standard TTL logic levels.
- External receiver circuits must be compatible to TTL signals.

Table 31: External Receiver Electrical Requirements

| Xtium PX8 Output Level | Description                   | MIN   | MAX   |
|------------------------|-------------------------------|-------|-------|
| TTL                    | Output Voltage High ( $V_H$ ) | 2.0 V | -     |
|                        | Output Voltage Low ( $V_L$ )  | -     | 0.8 V |

### Note 3: RS-422 Shaft Encoder Input Specifications

Dual Quadrature Shaft Encoder Inputs (phase A and phase B) connect to differential signals (RS-422) or single ended signals. The figure below shows the simplified representation of these inputs.

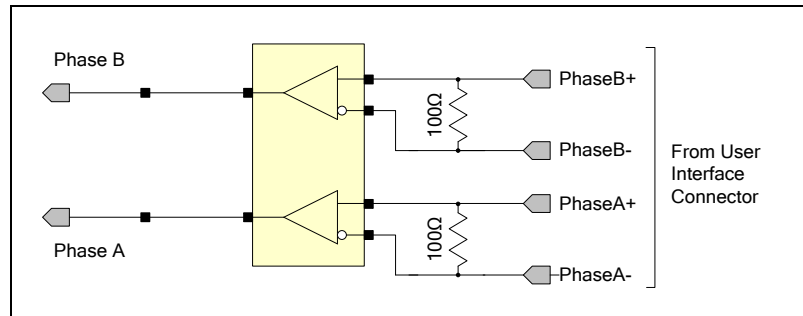


Figure 47: RS-422 Shaft Encoder Input Electrical Diagram

- RS-422 differential line receiver used is am26lv32.
- Input signals must meet the following
  - Maximum differential input voltage is +/- 7V.
  - Minimum differential voltage level is +/- 200mV.
- Both inputs have a 100-ohm differential resistor.
- Maximum input signal frequency is 10 MHz.
- The Xtium-CXP provides ESD filtering on-board.
- See Line Trigger Source Selection for Line scan Applications for more information.
- Refer to Sapera parameters:  
CORACQ\_PRM\_SHAFT\_ENCODER\_ENABLE CORACQ\_PRM\_SHAFT\_ENCODER\_DROP  
or refer to CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_ENABLE  
CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_DETECTION  
CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_LEVEL (fixed at RS-422)  
CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_SOURCE
- See also \*.cvi file entries:  
Shaft Encoder Enable, Shaft Encoder Pulse Drop,  
or see External Line Trigger Enable, External Line Trigger Detection, External Line Trigger Level,  
External Line Trigger Source.
- For TTL single ended signals, connect a bias voltage to the RS-422 (-) input to ensure correct detection of the logic state of the signal connected to the RS-422 (+) input. See the following section for connection methods.



**Example: Connecting to the RS-422 Shaft Encoder Block Diagram**

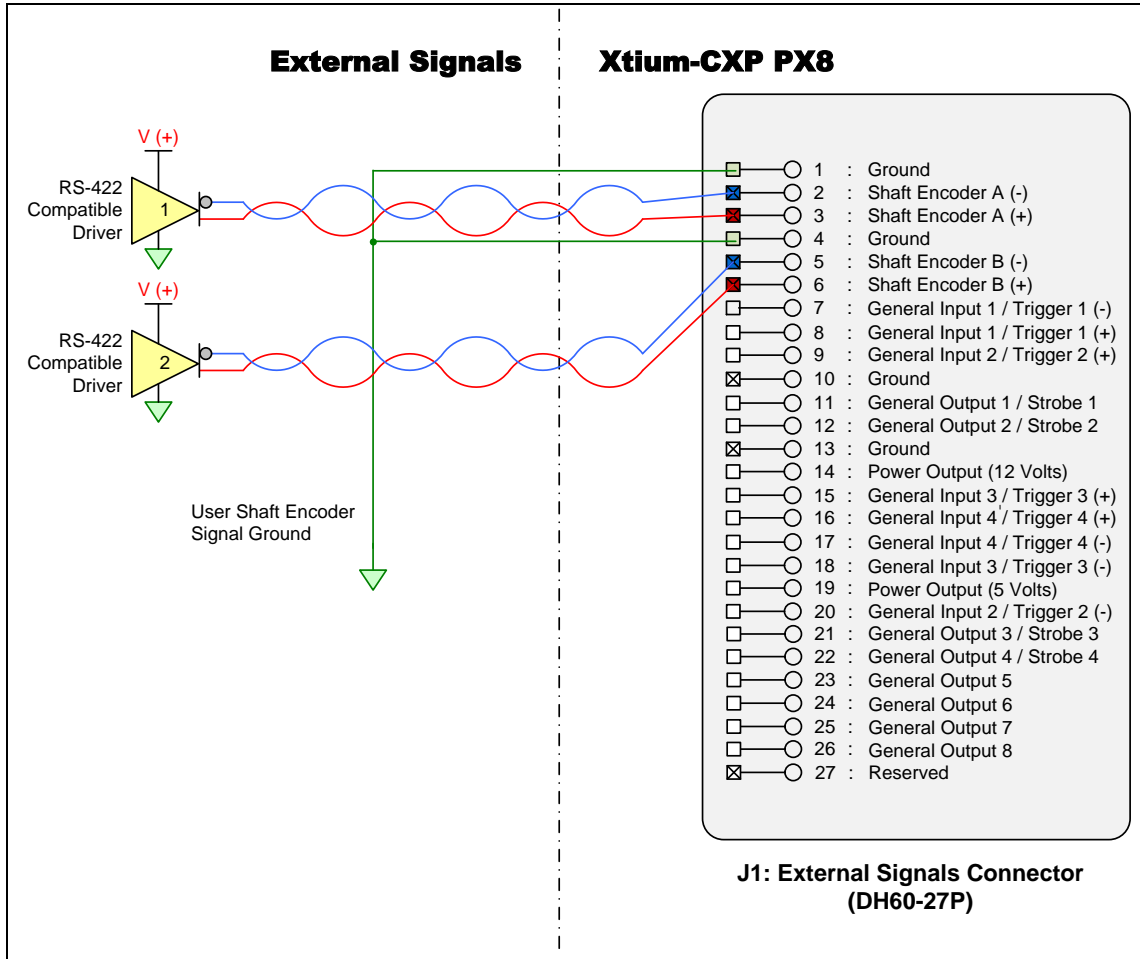


Figure 48: External RS-422 Signals Connection Diagram

**Note 3.2: Interfacing to a TTL (also called Push-Pull) Output**

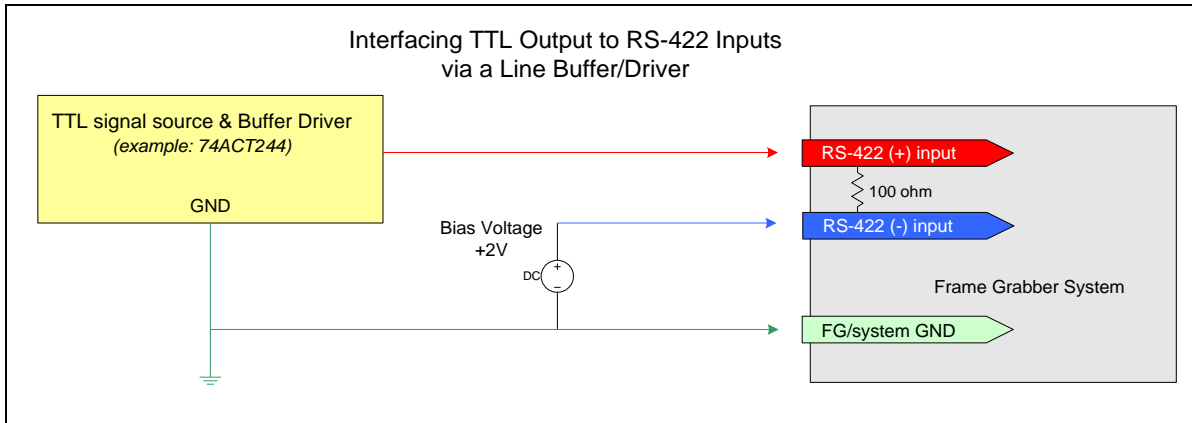


Figure 49: Interfacing TTL to RS-422 Shaft Encoder Inputs

- The graphic shows a single-ended driver signal interfaced to the RS-422 input.
- RS-422 (-) input is biased to a DC voltage of +2 volts.
- This guarantees that the TTL signal connected to the RS-422 (+) input will be detected as a logic high or low relative to the (-) input.
- The TTL shaft encoder ground, the bias voltage ground, and the Xtium-CL PX4 computer system ground must be connected together.
- DC voltage for the RS-422 (-) input can be generated by a resistor voltage divider.
- Use a single battery cell if this is more suitable to your system.

**Note 3.3: Interfacing to a Line Driver (also called Open Emitter) Output**

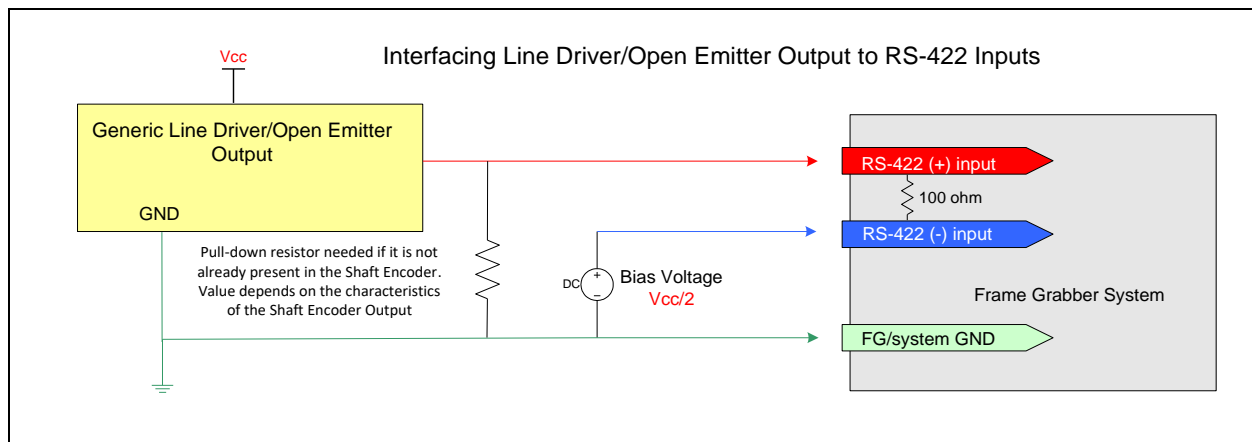


Figure 50: Interfacing to a Line Driver Output

### Note 3.4: Interfacing to an Open Collector Output

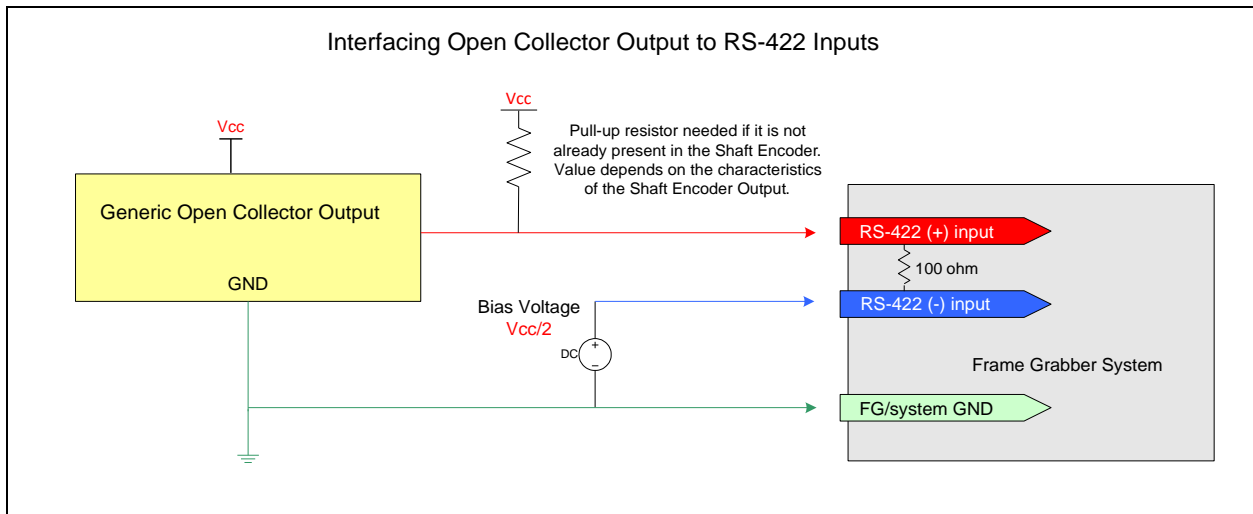


Figure 51: Interfacing to an Open Collector Output

## J2, J3, J4, J5: CoaXPress Connector



**Note:** The CoaXPress camera connector is defined in the JIIA document "CoaXPress Standard" version 1.1, ©2013 JIIA. Typically, there is no need to be concerned with the physical pinout of the connector or cables.

## J9: Multi-Board Sync / Bi-directional General I/Os

There are 8 bi-directional General I/Os that can be interconnected between multiple boards. These bi-directional I/Os can be read/written by Sopera application. Bi-directional General I/Os no.1 and no.2 also can also act as the multi-board sync I/Os.

The multi-board sync feature permits interconnecting multiple Xtium boards to synchronize acquisitions to one or two triggers or events. The trigger source origin can be either an external signal or a software control signal. The board sending the trigger(s) is the "Sync Master" board, while the one or more boards receiving the control signal(s) are "Sync Slaves".

Setup of the boards is done either by setting parameters via a Sopera application or by using CamExpert to configure two camera files (.cxf). For testing purposes, two instances of CamExpert (one for each board) can be run on the system where the frame grabbers are installed.

### Hardware Preparation

- Interconnect two, three, or four Xtium boards via their J9 connector using the OR-YXCC-BSYNC20 cable (for 2 boards) or the OR-YXCC-BSYNC40 cable (see Board Sync Cable Assembly OR-YXCC-BSYNC40 for 3 or 4 boards).



**Warning:** Multi-Board Sync / Bi-directional General I/Os are only for use with Teledyne DALSA frame grabbers within the same PC, otherwise electrical damage to boards can occur.

### Configuration via Sapera Application Programming

- **Sync Master Board** Software Setup: Choose one Xtium as "Sync Master". The Sapera parameter CORACQ\_PRM\_BOARD\_SYNC\_OUTPUT1\_SOURCE and/or CORACQ\_PRM\_BOARD\_SYNC\_OUTPUT2\_SOURCE select the signal(s) to send to the "Sync Slave" boards.
- Other sync master board parameters are set as for any external trigger application, such as External Trigger enable, detection, and level. See Sapera documentation for more details.
- **Sync Slave Board** Software Setup: The Sapera parameter CORACQ\_PRM\_EXT\_TRIGGER\_SOURCE and/or CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_SOURCE are set to Board Sync #1 or #2.

### Configuration via Sapera CamExpert

- Start the first instance of CamExpert and select one installed **Xtium board** to be the **sync master**. As shown in the following image, this board is configured to use an external trigger on input #1.

The screenshot shows a 'Parameters' dialog box with a tree view on the left and a table of parameters on the right. The tree view is expanded to 'External Trigger'. The table lists the following parameters and values:

| Category             | Parameter                                 | Value               |
|----------------------|---|---------------------|
| Basic Timing         | External Trigger                          | Enable              |
| Advanced Control     | External Trigger Detection                | Rising Edge         |
| External Trigger     | External Trigger Level                    | TTL                 |
| Image Buffer and ROI | External Trigger Source                   | External Trigger #1 |
|                      | External Trigger Minimum Duration (in us) | 0                   |
|                      | Frame Count per External Trigger          | 1                   |
|                      | External Trigger Delay                    | 0                   |
|                      | External Trigger Delay Time Base          | nanoseconds         |
|                      | External Trigger Ignore Delay             | 0                   |

- The **Sync Master Xtium board** is also configured to output the external trigger on board sync #1, as shown in the following image.

The screenshot shows a 'Parameters' dialog box with a tree view on the left and a table of parameters on the right. The tree view is expanded to 'Attached Camera - Xtiu...'. The table lists the following parameters and values:

| Category | Parameter                                | Value                  |
|----------|--|------------------------|
| Board    | Internal Frame Trigger                   | Disabled               |
|          | Internal Frame Trigger Frequency (in Hz) | 30                     |
|          | Camera Control method selected           | None                   |
|          | Time Integration Method Setting          | None                   |
|          | Camera Trigger Method Setting            | None                   |
|          | Camera Frames Per Trigger                | 1                      |
|          | Camera Control During Readout            | Invalid                |
|          | Strobe Method Setting                    | None                   |
|          | Time Stamp Base                          | Microseconds           |
|          | Board Sync Output 1 Source               | External Frame Trigger |
|          | Board Sync Output 2 Source               | Disabled               |

- The **Sync Slave Xtium board** is configured to receive its trigger on the board sync signal. As an example the following image shows the Xtium board configured for an external sync on board sync #2.

| Parameters  |   | Parameter     | Value |
|---|---|---------------|-------|
| <ul style="list-style-type: none"> <li>Board               <ul style="list-style-type: none"> <li>Basic Timing</li> <li>Advanced Control</li> <li>External Trigger</li> <li>Image Buffer and ROI</li> </ul> </li> <li>Attached Camera - Xtium...</li> </ul> | External Trigger                          | Enable        |       |
|   | External Trigger Detection                | Rising Edge   |       |
|   | External Trigger Level                    | TTL           |       |
|   | External Trigger Source                   | Board Sync #2 |       |
|   | External Trigger Minimum Duration (in us) | 0             |       |
|   | Frame Count per External Trigger          | 1             |       |
|   | External Trigger Delay                    | 0             |       |
|   | External Trigger Delay Time Base          | Nanoseconds   |       |
|   | External Trigger Ignore Delay             | 0             |       |

- **Test Setup:** Start the acquisition on all slave boards. The acquisition process is now waiting for the control signal from the master board. Trigger master board acquisition and the acquisition start signal is sent to each slave board.

## J12: Power Connector

### DC Power Details



**Warning:** Never remove or install any hardware component with the computer power on. Never connect a power cable to J12 when the computer is powered on.

- Connect a computer 6-pin PCI Express power connector to J12 to supply DC power to the CoaXPress connectors for PoCXP operation and/or to supply power to connector J1/J7. Older computers may need a power cable adapter (see Power Cable Assembly OR-YXCC-PWRY00).
- The 12 Volt can supply up to 6W to J1 or J7. Note that J1 and J7 have a 500 mA re-settable fuse on the board. If the fuse trips open, turn off the host computer power. When the computer is powered again, the fuse is automatically reset.
- The 12 Volt also supplies the 24V (through a step-up circuitry) with up to 13W of power to each CXP input as per CoaXPress specifications.

# Cables & Accessories

The following cables and accessories are available for purchase via third party vendors or Teledyne DALSA. Contact sales for information.

## CoaXPress Cables

The Xtium CXP frame grabber uses DIN 1.0/2.3 coaxial connectors (camera connectors may vary depending on the camera model). For additional information on cables and their specifications, visit the following web sites:

Table 32: CoaXPress Cable Suppliers

|                    |   |
|--------------------|---|
| Components Express | <a href="http://www.componentsexpress.com/">http://www.componentsexpress.com/</a> |
| Samtec             | <a href="https://www.samtec.com/">https://www.samtec.com/</a>                     |

## DH40-27S Cable to Blunt End (OR-YXCC-27BE2M1, Rev B1)

Cable assembly consists of a 2000 mm (~6 ft.) blunt end cable to mate to Xtium external connector **J1**. Note: The applicable wiring color code table is included with the printed Product Notice shipped with the cable package — no other wiring table should be used.

Important: Cable part number OR-YXCC-27BE2M0 rev.3 is obsolete and should not be used with any Xtium series boards.

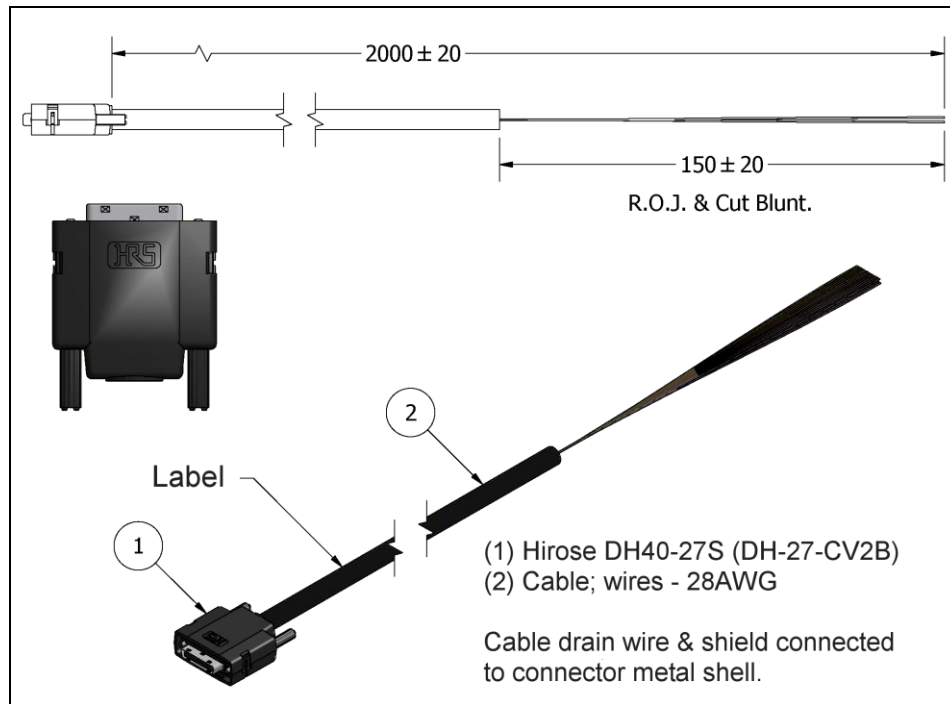


Figure 52: DH60-27P Cable No. OR-YXCC-27BE2M1 Detail



Figure 53: Photo of cable OR-YXCC-27BE2M1

## DH40-27S Connector Kit for Custom Wiring

Teledyne DALSA makes available a kit comprised of the DH40-27S connector plus a screw lock housing package, for clients interested in assembling their own custom I/O cable. Order part number "OR-YXCC-H270000", (package as shown below).

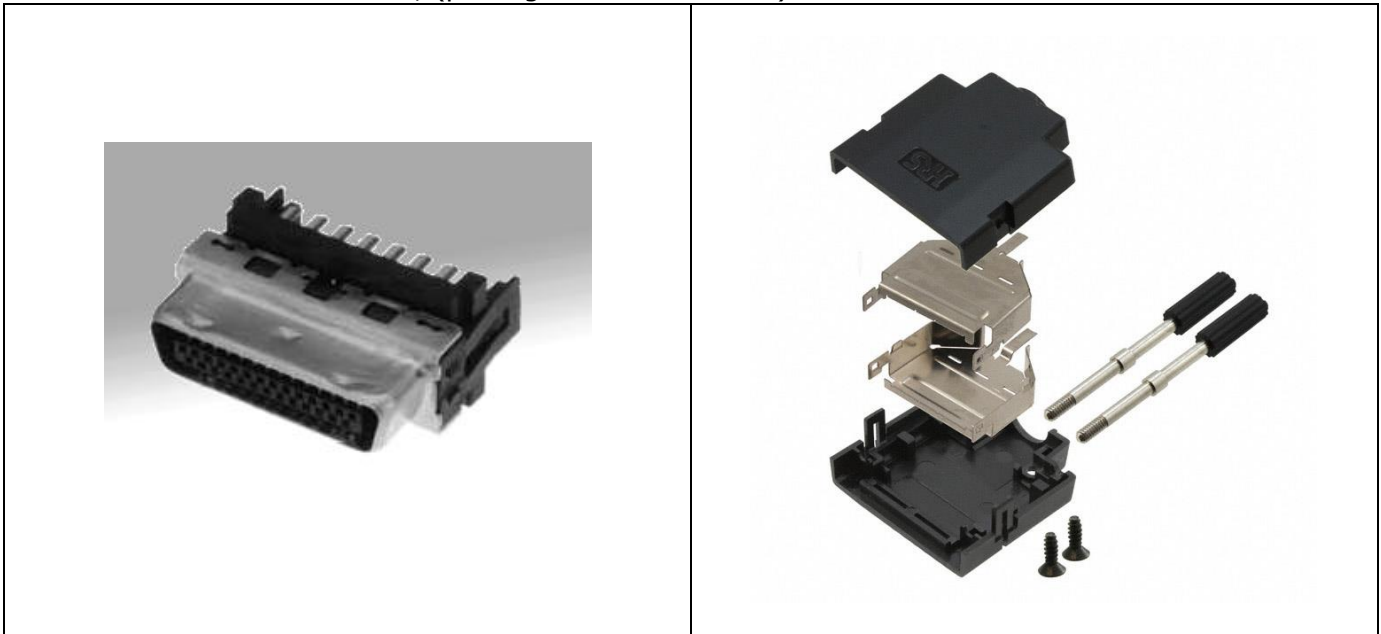


Figure 54: OR-YXCC-H270000 Custom Wiring Kit

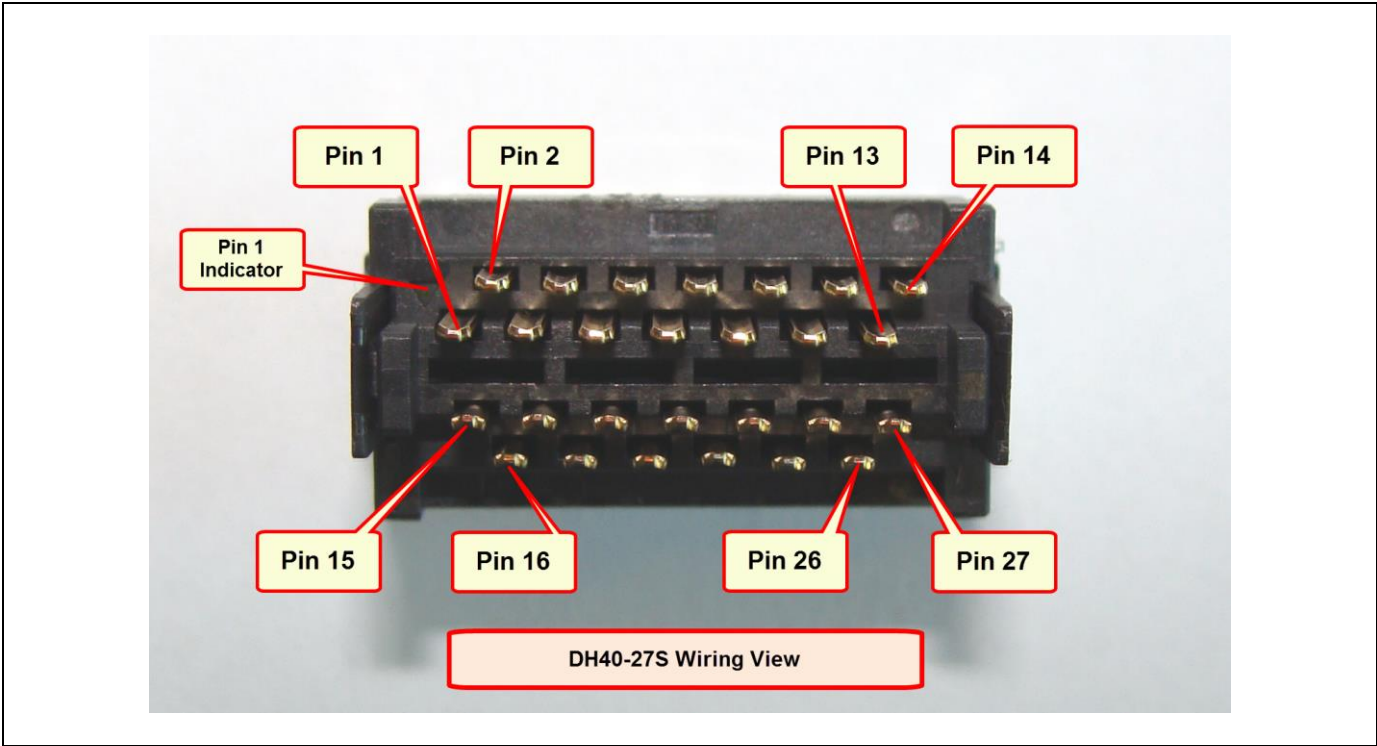


Figure 55: OR-YXCC-H270000 Pin Configuration



## Cable assemblies for I/O connector J7

Flat ribbon cables for connecting to J7 can be purchased from Teledyne DALSA or from third part suppliers, as described below.

### ***Teledyne DALSA I/O Cable (part #OR-YXCC-TIOF120)***

Contact Teledyne DALSA Sales to order the 12 inch (~30cm) I/O cable with connectors on both ends, as shown in the following picture.

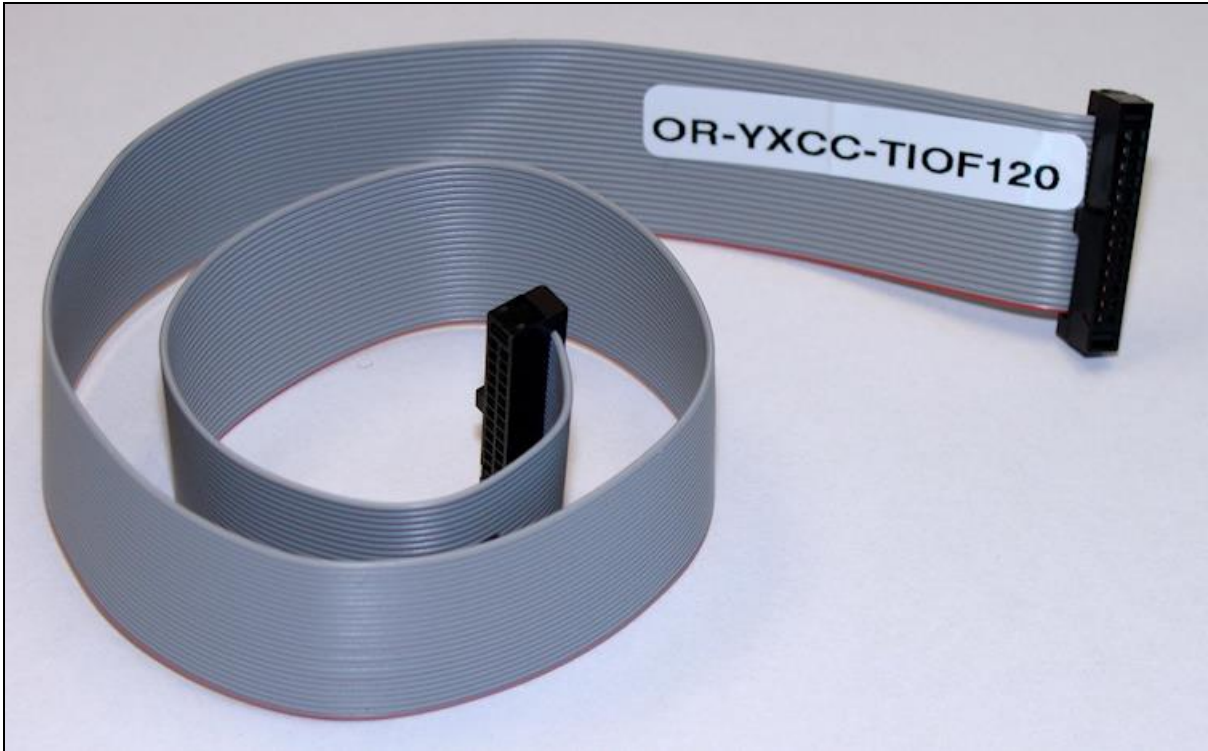


Figure 56: I/O Cable #OR-YXCC-TIOF120

### ***Third Party I/O Cables for J7***

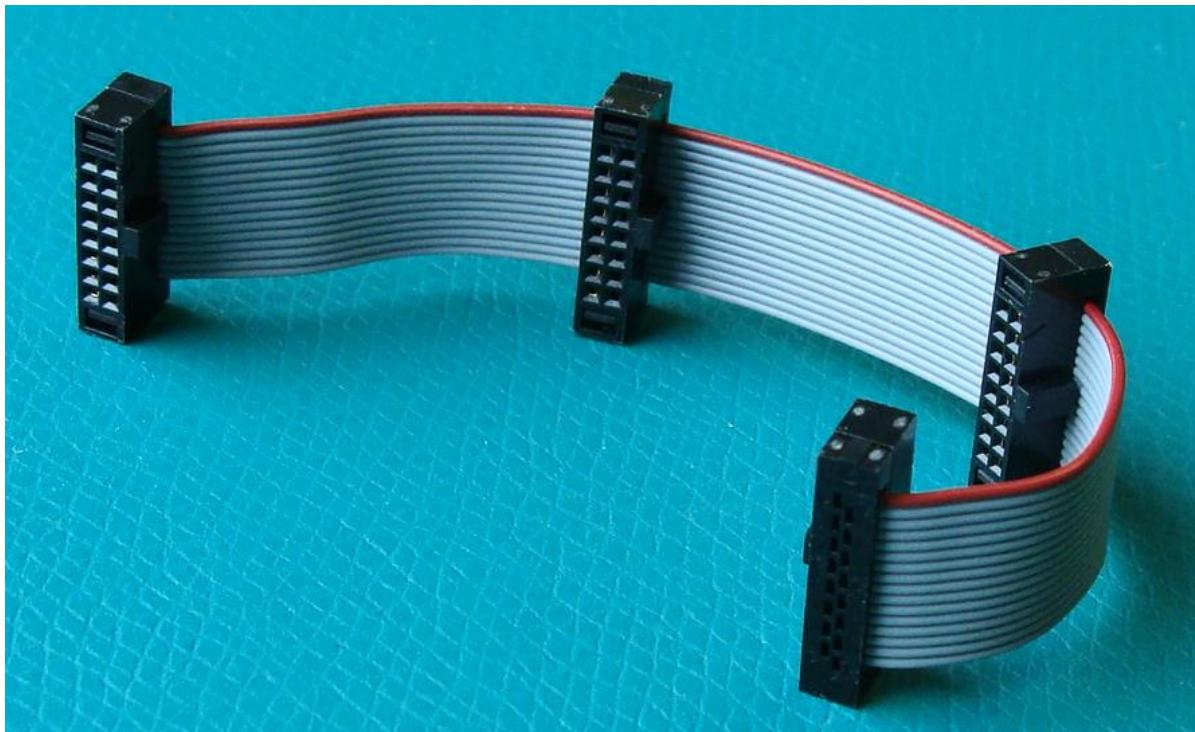
Suggested third party cables are available from SAMTEC. Below are two examples:

- Connector to connector (FFSD-13-D-xx.xx-01-N)
- Connector to blunt end (FFSD-13-S-xx.xx-01-N)
- Note: xx.xx denotes length, where 06.00 is a 6 inch (~15 cm) length cable
- URL: [http://cloud.samtec.com/catalog\\_english/FFSD.PDF](http://cloud.samtec.com/catalog_english/FFSD.PDF)

## Board Sync Cable Assembly OR-YXCC-BSYNC40

This cable connects 3 to 4 Xtium boards for the board sync function as described in section J9: Multi-Board Sync / Bi-directional General I/Os. For a shorter 2 board cable, order cable assembly OR-YXCC-BSYNC20.

For a third part source of cables, see [http://cloud.samtec.com/catalog\\_english/FFSD.PDF](http://cloud.samtec.com/catalog_english/FFSD.PDF).

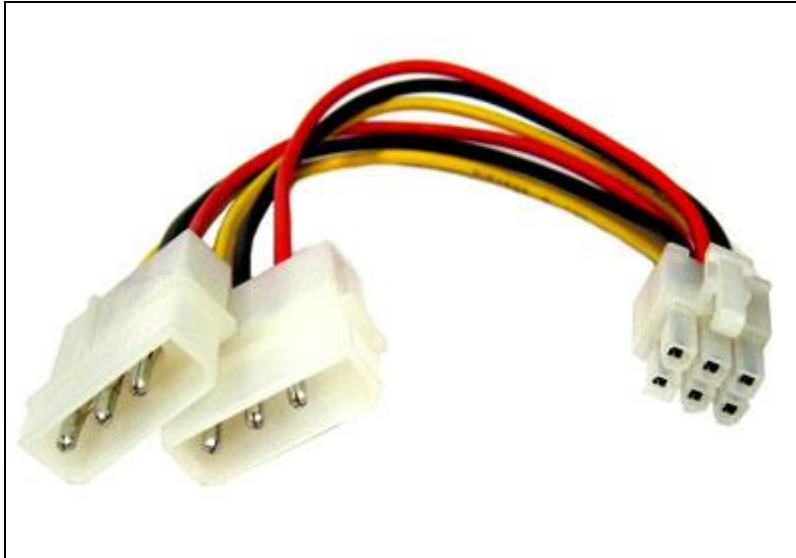


*Figure 57: Photo of cable OR-YXCC-BSYNC40*

## Power Cable Assembly OR-YXCC-PWRY00

When the Xtium-CXP PX8 supplies power to cameras via PoCXP and/or when power is supplied to external devices via the J1/J7 I/O connector, PC power must be connected to the Xtium external power source connector (J12).

Recent computer power supplies provide multiple 6-pin power source connectors for PCI Express video cards, where one is connected to J12 on the Xtium-CXP. But if the computer is an older model, this power supply adapter converts 2 standard 4-pin large power connectors to a 6-pin power connector.



*Figure 58: Photo of cable assembly OR-YXCC-PWRY00*

This is an industry standard adapter cable which can be purchased from Teledyne DALSA.

# CoaXPress Interface

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## CoaXPress Overview



**Note:** The following text is extracted from the CoaXPress website; refer to their site [www.coaxpress.com](http://www.coaxpress.com) for additional information.

CoaXPress (CXP) is an asymmetric high-speed point to point serial communication standard for the transmission of video and still images, scalable over single or multiple coaxial cables. It has a high speed downlink of up to 6.25Gbps per cable for video, images and data, plus a lower speed, 20Mbps uplink for communications and control. Power is also available over the cable ("Power-over-Coax") and cable lengths of greater than 100m may be achieved.

- High-speed data rates: up to 6.25 Gbps over a single coax cable and scalable for multiple cables. (for example, 4 cables give 25 Gbps, 8 cables give 50 Gbps, and so forth).
- Long Cable Lengths: In excess of 100m at 3.125 Gbps and 40m at 6.25 Gbps.
- Real time behavior with fixed, low latency transmission.
- Precise triggering capability.
- Flexible and reliable through use of standard coax – for example, RG59 and RG6.
- Ease of integration: image data, communication, control and power over a single coax cable.
- Cost-effective cabling solutions
- Hot pluggable.
- Royalty-free solution.

# Contact Information

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## Sales Information

**Visit our web site:**

<http://www.teledynedalsa.com/en/products/imaging/>

**Email:**

<mailto:info@teledynedalsa.com>

### Canadian Sales

Teledyne DALSA — Head office  
605 McMurray Road  
Waterloo, Ontario, Canada, N2V 2E9  
Tel: 519 886 6000  
Fax: 519 886 8023

Teledyne DALSA — Montreal office  
880 Rue McCaffrey  
St. Laurent, Quebec, Canada, H4T 2C7  
Tel: (514) 333-1301  
Fax: (514) 333-1388

### USA Sales

Teledyne DALSA — Billerica office  
700 Technology Park Drive  
Billerica, Ma. 01821  
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Support requests for imaging applications

Camera support information

Product literature and driver updates

<http://www.teledynedalsa.com/mv/support>