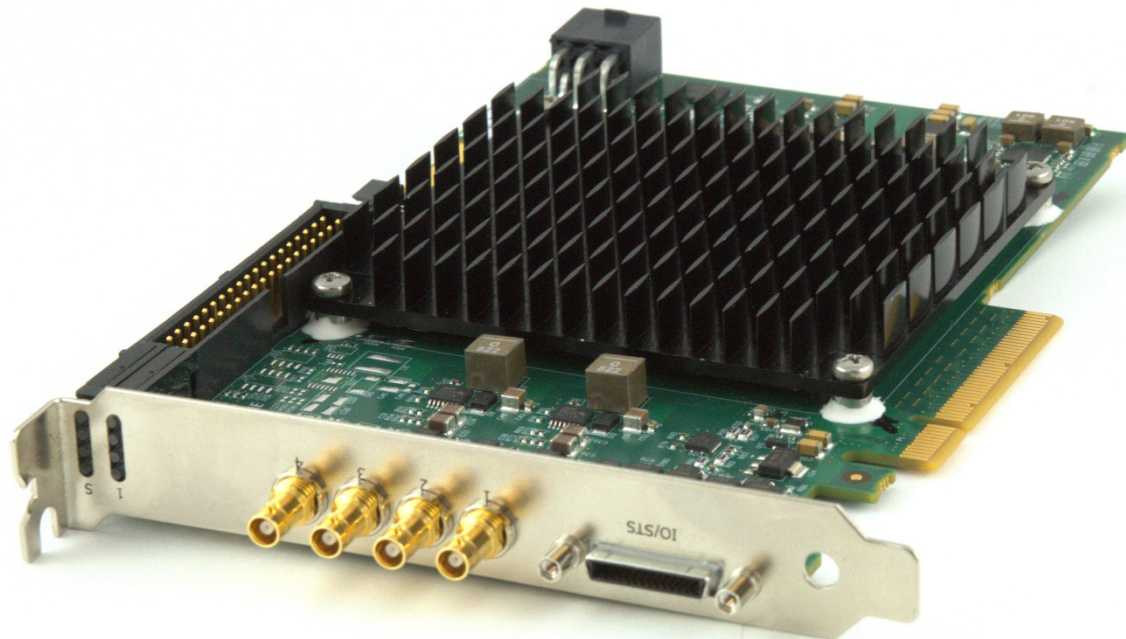


# Xtium2-CXP PX8™

User's Manual  
Edition 1.01

sensors | cameras | **frame grabbers** | processors | software | vision solutions



P/N: OC-A8XM-PX8U0  
[www.teledynedalsa.com](http://www.teledynedalsa.com)

 **TELEDYNE DALSA**  
Everywhereyoulook™

# Notice

© 2023 Teledyne DALSA, Inc. All rights reserved.

This document may not be reproduced nor transmitted in any form or by any means, either electronic or mechanical, without the express written permission of TELEDYNE DALSA. Every effort is made to ensure the information in this manual is accurate and reliable. Use of the products described herein is understood to be at the user's risk. TELEDYNE DALSA assumes no liability whatsoever for the use of the products detailed in this document and reserves the right to make changes in specifications at any time and without notice.

Microsoft® is a registered trademark;  
Windows®, Windows® 10 are trademarks of Microsoft Corporation.

All other trademarks or intellectual property mentioned herein belongs to their respective owners.

Edition 1.01 released on March 15, 2023  
Document Number: OC-A8XM-PX8U0

## **About Teledyne DALSA**

Teledyne DALSA is an international high performance semiconductor and Electronics Company that designs, develops, manufactures, and markets digital imaging products and solutions, in addition to providing wafer foundry services.

Teledyne DALSA Digital Imaging offers the widest range of machine vision components in the world. From industry-leading image sensors through powerful and sophisticated cameras, frame grabbers, vision processors and software to easy-to-use vision appliances and custom vision modules.

# Contents

<b>OVERVIEW</b>	<b>1</b>
PRODUCT PART NUMBERS	1
XTIUM2-CXP PX8 FRAME GRABBER FEATURES	2
<i>User Programmable Configurations</i>	2
<i>ACUPlus: Acquisition Control Unit</i>	3
<i>DTE: Intelligent Data Transfer Engine</i>	3
<i>PCI Express x8 Gen3 Interface</i>	3
<i>Advanced Controls Overview</i>	3
DEVELOPMENT SOFTWARE OVERVIEW	4
<i>Sapera LT Library</i>	4
<i>Sapera Processing Library</i>	4
<i>About CoaXPress</i>	4
<b>QUICK START SETUP &amp; INSTALLATION</b>	<b>5</b>
<b>INSTALLING XTIUM2-CXP PX8</b>	<b>9</b>
WARNING! (GROUNDING INSTRUCTIONS)	9
INSTALLATION OVERVIEW	9
<i>Hardware Installation</i>	9
Multi-board Sync & I/O Setup	9
<i>Sapera LT Library &amp; Xtium2-CXP PX8 Driver Installation</i>	10
Installation Procedure	10
<i>Xtium2-CXP PX8 Firmware Update</i>	10
Firmware Update: Automatic Mode	11
Firmware Update: Manual Mode	11
Executing the Firmware Update program from the Start Menu	12
UPGRADING SAPERA OR BOARD DRIVER	13
<i>Board Driver Upgrade Only</i>	13
<i>Upgrading both Sapera and Board Driver</i>	13
<i>Preserving Board Parameters during Driver Upgrade</i>	14
PRESERVING BOARD PARAMETERS DURING BOARD REPLACEMENT OR SYSTEM CLONING	15
DISPLAYING XTIUM2-CXP PX8 BOARD INFORMATION	16
<i>Device Manager – Board Viewer</i>	16
<i>Information Field Description</i>	17
<i>Changing Device Settings</i>	20
<i>Device Information Report</i>	21
CONFIGURING SAPERA	22
<i>Increasing Contiguous Memory for Sapera Resources</i>	22
Host Computer Frame Buffer Memory Limitations	23
Contiguous Memory for Sapera Messaging	23
<b>CAMEXPERT QUICK START</b>	<b>24</b>
INTERFACING CXP CAMERAS WITH CAMEXPERT	24
<i>CamExpert Example with a Monochrome Camera</i>	24
CAMEXPERT DEMONSTRATION AND TEST TOOLS	26
<i>Camera Types &amp; Files</i>	26
<i>Overview of Sapera Acquisition Parameter Files (.ccf or .cca/.cvi)</i>	26
<i>Saving a Camera File</i>	27
<i>Camera Interfacing Check List</i>	27
USING CAMEXPERT WITH XTIUM2-CXP PX8	28
BASIC TIMING CATEGORY	29

<i>Parameter Descriptions</i> .....	29
ADVANCED CONTROL CATEGORY .....	31
<i>Parameter Descriptions</i> .....	32
EXTERNAL TRIGGER CATEGORY .....	34
<i>Parameter Descriptions</i> .....	35
IMAGE BUFFER AND ROI CATEGORY .....	37
<i>Parameter Descriptions</i> .....	38
USING THE FLAT FIELD CORRECTION TOOL .....	39
<i>Xtium2-CXP PX8 Flat Field Support</i> .....	39
Loading the Required Camera File .....	39
<i>Set up Dark and Bright Acquisitions with the Histogram Tool</i> .....	39
Verify a Dark Acquisition .....	39
Verify a Bright Acquisition .....	40
<i>Flat Field Correction Calibration Procedure</i> .....	41
Flat Field Correction Dialog .....	42
<i>Using Flat Field Correction</i> .....	42
USING THE BAYER FILTER TOOL .....	43
<i>Bayer Filter White Balance Calibration Procedure</i> .....	43
Using the Bayer Filter .....	43
<b>SAPERA DEMO APPLICATIONS</b> .....	<b>44</b>
GRAB DEMO OVERVIEW .....	45
<i>Using the Grab Demo</i> .....	45
<b>XTIUM2-CXP PX8 REFERENCE</b> .....	<b>46</b>
BLOCK DIAGRAM .....	46
XTIUM2-CXP FLOW DIAGRAM .....	47
LINE TRIGGER SOURCE SELECTION FOR LINE SCAN APPLICATIONS .....	48
SHAFT ENCODER INTERFACE TIMING .....	49
VIRTUAL FRAME TRIGGER FOR LINE SCAN CAMERAS .....	51
<i>Synchronization Signals for a 10 Line Virtual Frame</i> .....	51
<i>Synchronization Signals for Fixed Frame Length Acquisition</i> .....	52
<i>Synchronization Signals for Variable Frame Length Acquisition</i> .....	53
SAPERA ACQUISITION METHODS .....	55
TRIGGER TO IMAGE RELIABILITY .....	56
<i>Supported Events and Transfer Methods</i> .....	56
Acquisition Module Events .....	56
Acquisition Device Events .....	57
Transfer Events .....	58
Trigger Signal Validity .....	59
Supported Transfer Cycling Methods .....	59
OUTPUT LUT AVAILABILITY .....	61
METADATA: THEORY OF OPERATION .....	62
<i>Metadata Data Structure</i> .....	62
Clearing Metadata Counters .....	62
Metadata Example .....	62
FLAT FIELD CORRECTION: THEORY OF OPERATION .....	63
<i>Flat Field Correction Lists</i> .....	63
<i>Flat Field Correction Sets</i> .....	63
Xtium2-CXP PX8 specific limitations .....	63
Programming the sets .....	64
XTIUM2-CXP PX8 SUPPORTED PARAMETERS .....	65
<i>Camera Related Capabilities</i> .....	65
<i>Camera Related Parameters</i> .....	65
<i>VIC Related Parameters</i> .....	67
<i>ACQ Related Parameters</i> .....	71

<i>Transfer Related Capabilities</i> .....	73
<i>Transfer Related Parameters</i> .....	73
<i>General Outputs #1: Related Capabilities (for GIO Module #0)</i> .....	74
<i>General Outputs #1: Related Parameters (for GIO Module #0)</i> .....	74
<i>General Inputs #1: Related Capabilities (for GIO Module #1)</i> .....	74
<i>General Inputs #1: Related Parameters (for GIO Module #1)</i> .....	74
<i>Bidirectional General I/Os: Related Capabilities (for GIO Module #2)</i> .....	75
<i>Bidirectional General I/Os: Related Parameters (for GIO Module #2)</i> .....	75
SAPERA SERVERS AND RESOURCES .....	76

## **TECHNICAL SPECIFICATIONS** **78**

XTIUM2-CXP PX8 BOARD SPECIFICATIONS .....	78
HOST SYSTEM REQUIREMENTS .....	79
EMC DECLARATIONS OF CONFORMITY .....	80
<i>FCC Statement of Conformance</i> .....	80
FCC Class A Product .....	80
<i>CE Declaration of Conformity</i> .....	80
CONNECTOR AND SWITCH LOCATIONS .....	81
<i>Xtium2-CXP PX8 Board Layout Drawing</i> .....	81
<i>Connector / LED Description List</i> .....	81
CONNECTOR AND SWITCH SPECIFICATIONS .....	82
<i>Xtium2-CXP PX8 End Bracket Detail</i> .....	82
<i>Status LEDs Functional Descriptions</i> .....	83
S: Boot-up/PCIe Status LED .....	83
L1, L2, L3, L4: CoaXPress Status LED .....	83
<i>J7: External I/O Signals Connector (Female DH60-27P)</i> .....	84
<i>J8: Internal I/O Signals Connector (40-pin TST-120-01-G-D)</i> .....	85
Note 1: General Inputs / External Trigger Inputs Specifications.....	86
Block Diagram: Connecting External Drivers to General Inputs .....	88
External Driver Electrical Requirements.....	89
Note 2: General Outputs /Strobe Output Specifications.....	90
Block Diagram: Connecting External Receivers to the General Outputs .....	91
External Receiver Electrical Requirements .....	92
Note 3: RS-422/TTL Shaft Encoder Input Specifications .....	93
Note 3.1: Interfacing to an RS-422 Driver Output .....	95
Note 3.2: Interfacing to a Line Driver (also called Open Emitter) Output .....	97
Note 3.3: Interfacing to an Open Collector Output.....	97
Note 3.4: Interfacing directly to a TTL (also called Push-Pull) Output .....	98
Note 3.5: Interfacing to a TTL using a Bias Voltage .....	98
<i>C1, C2, C3, C4: CoaXPress Connector</i> .....	99
<i>J9: Multi-Board Sync / Bi-directional General I/Os</i> .....	99
Hardware Preparation .....	99
Configuration via Sapera Application Programming.....	99
Configuration via Sapera CamExpert.....	100
<i>J10: Power Connector</i> .....	101
DC Power Details .....	101
CABLES & ACCESSORIES .....	102
<i>CoaXPress Cables</i> .....	102
<i>DH40-27S Cable to Blunt End (OR-YXCC-27BE2M1, Rev B1)</i> .....	102
<i>DH40-27S Connector Kit for Custom Wiring</i> .....	104
<i>Cable assemblies for I/O connector J8</i> .....	105
External Signals Connector Bracket Assembly .....	105
External Signals Connector Bracket Drawing.....	105
External Signals Connector Bracket Pinout.....	105
<i>Board Sync Cable Assembly OR-YXCC-BSYNC40</i> .....	107
<i>Power Cable Assembly OR-YXCC-PWRY00</i> .....	108

<b>COAXPRESS INTERFACE</b>	<b>109</b>
COAXPRESS OVERVIEW	109
<b>APPENDIX A: SILENT INSTALLATION</b>	<b>110</b>
SILENT MODE INSTALLATION	110
<i>Creating a Response File</i>	110
<i>Running a Silent Mode Installation</i>	111
SILENT MODE UNINSTALL	111
<i>Creating a Response File</i>	111
<i>Running a Silent Mode Uninstall</i>	111
SILENT MODE INSTALLATION RETURN CODE	112
INSTALLATION SETUP WITH CORAPPLAUNCHER.EXE	112
CUSTOM DRIVER INSTALLATION USING INSTALL.INI	113
<i>Creating the install.ini File</i>	113
<i>Run the Installation using install.ini</i>	113
<b>APPENDIX B: TROUBLESHOOTING PROBLEMS</b>	<b>114</b>
OVERVIEW	114
PROBLEM TYPE SUMMARY	114
<i>First Step: Check the Status LED</i>	114
<i>Possible Installation Problems</i>	114
<i>Possible Functional Problems</i>	115
TROUBLESHOOTING PROCEDURES	116
<i>Diagnostic Tool Overview</i>	116
Diagnostic Tool Main Window	116
Diagnostic Tool Self-Test Window	118
Camera Input Eye Diagram Monitor	118
Diagnostic Tool Live Monitoring Window	119
<i>Checking for PCI Bus Conflicts</i>	119
<i>Windows Device Manager</i>	121
<i>BSOD (blue screen) Following a Board Reset</i>	121
<i>Sapera and Hardware Windows Drivers</i>	122
<i>Recovering from a Firmware Update Error</i>	122
<i>Driver Information via the Device Manager Program</i>	122
Information Window	123
<i>Sapera Log Viewer</i>	124
<i>On-board Image Memory Requirements for Acquisitions</i>	124
<i>Symptoms: CamExpert Detects no Boards</i>	125
Troubleshooting Procedure	125
<i>Symptoms: Xtium2-CXP PX8 Does Not Grab</i>	125
<i>Symptoms: Card grabs black</i>	125
<i>Symptoms: Card acquisition bandwidth is less than expected</i>	126
<i>Symptoms: PoCXP does not power the camera</i>	126
Over-current protection circuit is tripped	127
<b>REVISION HISTORY</b>	<b>129</b>
<b>CONTACT INFORMATION</b>	<b>130</b>
SALES INFORMATION	130
TECHNICAL SUPPORT	130

# Tables

Table 1: Xtium2-CXP PX8 Board Product Numbers.....	1
Table 2: Xtium2-CXP PX8 Software Product Numbers .....	1
Table 3: Xtium2-CXP PX8 Cables & Accessories.....	1
Table 4: Demos Workspace Details.....	44
Table 5: CORACO_PRM_EXT_LINE_TRIGGER_SOURCE – Parameter Values .....	48
Table 6: Buffer states. ....	60
Table 7: Output LUT Availability .....	61
Table 8: Camera Related Capabilities.....	65
Table 9: Camera Related Parameters.....	65
Table 10: VIC Related Parameters .....	67
Table 11: Acquisition Related Parameters.....	71
Table 12: Transfer Related Capabilities .....	73
Table 13: Transfer Related Parameters .....	73
Table 14: GIO-0 Related Capabilities .....	74
Table 15: GIO-0 Related Parameters .....	74
Table 16: GIO-1 Related Capabilities .....	74
Table 17: GIO-1 Related Parameters .....	74
Table 18: GIO-1 Related Parameters .....	75
Table 19: GIO-2 Related Parameters .....	75
Table 20: Xtium2-CXP PX8 - Servers and Resources .....	76
Table 21: Board Specifications .....	78
Table 22: Environment Specifications .....	79
Table 23: Power Specifications.....	79
Table 24: Board Connector List .....	81
Table 25: S Boot-up/PCIe Status LED .....	83
Table 26: Camera CXP Status LED.....	83
Table 27: DH60-27P Connector Signals.....	84
Table 28: 40-pin TST-120-01-G-D Connector Signals.....	85
Table 29: External Trigger Timing Specifications .....	87
Table 30: Input Switching Points and Propagation Delay .....	87
Table 31: External Driver Electrical Requirements .....	89
Table 32: External Receiver Electrical Requirements .....	92
Table 33: CoaXPress Cable Suppliers .....	102
Table 34: DB37 Cable Connector Details .....	106
Table 35: Xtium2-CXP PX8 Device Drivers .....	122

# Figures

Figure 1: Automatic Firmware Update .....	11
Figure 2: Manual Firmware Update .....	12
Figure 3: Start Menu Firmware Update Shortcut .....	12
Figure 4: Device Manager Parameter Setting Differences .....	14
Figure 5: Firmware Update Status .....	15
Figure 6: Same Firmware For All Devices Checkbox .....	15
Figure 7: Board Information via Device Manager .....	16
Figure 8: Device Manager File Menu save Device Info Command .....	21
Figure 9: CamExpert Program .....	24
Figure 10: CamExpert Device Tree .....	25
Figure 11: CamExpert Histogram of Dark Image .....	40
Figure 12: CamExpert Histogram of Bright Image .....	41
Figure 13: CamExpert Flat Field Correction Menu Command .....	41
Figure 14: CamExpert Flat Field Correction Dialog .....	42
Figure 15: The Sapera Explorer application .....	44
Figure 16: Xtium2-CXP PX8 Block Diagram .....	46
Figure 17: Xtium2-CXP Flow Diagram .....	47
Figure 18: Encoder Input with Pulse-drop Counter .....	49
Figure 19: Using Shaft Encoder Direction Parameter .....	50
Figure 20: Synchronization Signals for a 10 Line Virtual Frame .....	52
Figure 21: Line scan, Fixed Frame, No Trigger .....	52
Figure 22: Line scan, Fixed Frame, Edge Trigger .....	53
Figure 23: Line scan, Fixed Frame, Level Trigger (Roll-Over to Next Frame) .....	53
Figure 24: Line scan, Variable Frame, Edge Trigger (Active High determines Frame Length) .....	53
Figure 25: Line scan, Fixed Frame, Level Trigger (Roll-Over) .....	54
Figure 26: Board Layout .....	81
Figure 27: End Bracket Details .....	82
Figure 28: General Inputs Electrical Diagram .....	86
Figure 29: External Trigger Input Validation & Delay .....	87
Figure 30: External Signals to J7 Connection Diagram .....	88
Figure 31: External Signals to J8 Connection Diagram .....	89
Figure 32: General Outputs Electrical Diagram .....	90
Figure 33: Output Signals to J7 Connection Diagram .....	91
Figure 34: Output Signals to J8 Connection Diagram .....	92
Figure 35: RS-422 Shaft Encoder Input Electrical Diagram .....	93
Figure 36: External RS-422 Signals to J7 Connection Diagram .....	95
Figure 37: External RS-422 Signals to J8 Connection Diagram .....	96
Figure 38: Interfacing to a Line Driver Output .....	97
Figure 39: Interfacing to an Open Collector Output .....	97
Figure 40: Interfacing TTL to TTL Shaft Encoder Inputs .....	98
Figure 41: Interfacing TTL to RS-422 Shaft Encoder Inputs using a Bias Voltage .....	98
Figure 42: DH60-27P Cable No. OR-YXCC-27BE2M1 Detail .....	102
Figure 43: Photo of cable OR-YXCC-27BE2M1 .....	103
Figure 44: OR-YXCC-H270000 Custom Wiring Kit .....	104
Figure 45: DB37 Output Cable .....	105
Figure 46: Photo of cable OR-YXCC-BSYNC40 .....	107
Figure 47: Photo of cable assembly OR-YXCC-PWRY00 .....	108
Figure 48: Create an install.ini File .....	113
Figure 49: Diagnostic Tool "Resource in use" .....	116
Figure 50: Diagnostic Tool Main Window .....	117
Figure 51: Diagnostic Tool Main Window .....	118



Figure 52: Eye Diagram .....	118
Figure 53: Diagnostic Tool Live Monitoring Window .....	119
Figure 54: PCI Diagnostic Program .....	120
Figure 55: PCI Diagnostic Program – PCI bus info .....	120
Figure 56: Using Windows Device Manager .....	121
Figure 57: Board Firmware Version.....	123
Figure 58: PCI Diagnostic Tool .....	126
Figure 59: CamExpert PoCXP Parameter .....	127
Figure 60: CamExpert Video Status Bar .....	127
Figure 61: Bad vs. Good CXP Connectors .....	128

# Overview

## Product Part Numbers

### Xtium2-CXP PX8 Board

Table 1: Xtium2-CXP PX8 Board Product Numbers

Item	Product Number
Xtium2-CXP PX8 Single	OR-A8X0-XPX10
Xtium2-CXP PX8 Dual	OR-A8X0-XPX20
Xtium2-CXP PX8 Quad	OR-A8X0-XPX40
Xtium2-CXP PX8 Quad CXP6 DIN connectors	OR-A8X6-XPX40
For OEM clients, this manual in printed form is available on request	OC-A8XM-PX8U0

### Xtium2-CXP PX8 Software

Table 2: Xtium2-CXP PX8 Software Product Numbers

Item	Product Number
Sapera LT version 8.70 or later for full feature support (required) <ol style="list-style-type: none"><li>1. Sapera LT: Provides everything needed to build imaging application</li><li>2. Current Sapera compliant board hardware drivers</li><li>3. Sapera documentation (compiled HTML help, pdf)</li></ol>	Free download at the <a href="#">Teledyne DALSA website</a>
(optional) Sapera Processing Imaging Development Library includes over 600 optimized image-processing routines.	<a href="#">Contact Sales at Teledyne DALSA</a>

### Optional Xtium2-CXP PX8 Cables & Accessories

Table 3: Xtium2-CXP PX8 Cables & Accessories

Item	Product Number
<b>DH40-27S cable assembly to blunt end:</b> 6 ft. cable I/O 27 pin Hirose connector to blunt end. This cable assembly connects to J7.	<a href="#">OR-YXCC-27BE2M1</a>
External Signals bracket (OC-X4CC-IOCAB) provides a simple way to bring out the signals from the External Signals Connector J8 to a bracket mounted DB37.	<a href="#">Cable assemblies for I/O connector J8</a>
DH40-27S Connector Kit for Custom Wiring: Comprised of a DH40-27S connector plus screw lock housing kit	<a href="#">OR-YXCC-H270000</a>
Cable assembly to connect to J9 (Board Sync) Connecting 2 boards Connection 3 or 4 boards	<a href="#">OR-YXCC-BSYNC20</a> <a href="#">OR-YXCC-BSYNC40</a>
Power interface cable required when supplying power for PoCXP	<a href="#">OR-YXCC-PWRY00</a>
CXP Cable Information	Refer to <a href="#">CoaXPress Cables</a>

---

# Xtium2-CXP PX8 Frame Grabber Features

- Compatible with CoaXPress (CXP) specification version 2.0 and 1.x (visit <http://jiiia.org/en/> for details on industry standards)
- Models with HDBNC connectors support up to 4 lanes of 12.5 Gbps each (4 cables support 50 Gbps)
- Models with DIN 1.0/2.3 connectors support up to 4 lanes of 6.250 Gbps each (4 cables support 25 Gbps)
- Acquisition of up to 4 independent cameras.
- The specification defines a device discovery methodology that can be automated and which provides plug and play capability
- CoaXPress cameras implement GenICam and associated GenCP, thus resulting in ease of use for Teledyne DALSA or third party cameras
- Uses a PCIe x8 Gen3 slot to maximize transfers to host computer buffers
- Acquire from Monochrome (8/10/12/14/16 bits per pixel), RGB (8/10/12 bits per pixel) CXP cameras, both area scan and line scan
- Acquire from Bayer (8/10/12 bits per pixel) CXP area scan cameras
- Output lookup tables
- Vertical and Horizontal Flip supported on board
- Flat Field and Flat Line correction: pixel replacement using neighborhood pixels
- External Input Triggers and Shaft Encoder inputs, along with Strobe outputs
- Multi-board Sync for trigger events supports simultaneously acquisitions from multiple cameras.
- Supports a number of acquisition events in compliance with "Teledyne DALSA's Trigger to Image Reliability"
- RoHS compliant

See [Technical Specifications](#) for detailed information.

## User Programmable Configurations

Use the Teledyne DALSA Device Manager utility to select firmware for one of the supported modes. Firmware selection is made either during driver installation or manually later on (see [Firmware Update: Manual Mode](#)).

### Quad Channel Model Firmware choices are:

- **One CXP Camera** (*installation default*): Support for one CXP camera of 1, 2 or 4 links (that is, physical CXP cable connections)
- **Two CXP Cameras:** Support for two independent CXP cameras of 1 or 2 links.
- **Three CXP Cameras:** Support for three independent CXP cameras of 1 link, or 2 cameras of 1 link and 1 camera of 2 links.
- **Four CXP Cameras:** Support for four independent CXP cameras of 1 link.

### Dual Channel Model Firmware choices are:

- **One CXP Camera** (*installation default*): Support for one CXP camera of 1, or 2 links (that is, physical CXP cable connections)
- **Two CXP Cameras:** Support for two independent CXP cameras of 1 link.

### Single Channel Model Firmware choices are:

- **One CXP Camera** (*installation default*): Support for one CXP camera of 1 link (that is, physical CXP cable connection)

## ACUPlus: Acquisition Control Unit

ACUPlus consists of a grab controller, one pixel packer and one time base generator per camera input.

ACUPlus acquires variable frame sizes up to 64KB per horizontal line and up to 64K lines per frame. ACUPlus can also capture an infinite number of lines from a line scan camera without losing a single line of data.

## DTE: Intelligent Data Transfer Engine

The Xtium2-CXP PX8 intelligent Data Transfer Engine ensures fast image data transfers between the board and the host computer with zero CPU usage. The DTE provides a high degree of data integrity during continuous image acquisition in a non-real time operating system like Windows. DTE consists of intelligent DMA units with auto-loading Scatter-Gather tables.

## PCI Express x8 Gen3 Interface

The Xtium2-CXP PX8 is a universal PCI Express x8 Gen3 board, compliant with the PCI Express 3.0 specification. The Xtium2-CXP PX8 board achieves transfer rates up to 7.0Gbytes/sec. to host memory. Note that performance can be lower depending on PC and/or programmed configuration.

The Xtium2-CXP PX8 board occupies one PCI Express x8 Gen3 expansion slot and one chassis opening.

### Important:

- To obtain the maximum transfer rate to host memory, make sure the Xtium2-CXP PX8 is in a computer with a Gen3 slot. The board will work in a Gen1 or Gen2 slot, but only with a quarter or half the possible transfer performance respectively.
- The system motherboard BIOS should allow setting the PCIe maximum payload size to 256 or higher. Systems with fixed settings of 128 will limit performance for transfers to host memory.
- If the computer only has a PCI Express x16 slot, test directly (use the supplied [diagnostic tool](#)) or review the computer documentation to know if the Xtium2-CXP PX8 is supported. Computer motherboards may only support x16 graphic video board products in x16 slots.

## Advanced Controls Overview

### Visual Indicators

Xtium2-CXP PX8 features up to 5 LED indicators to facilitate system installation and setup (see [Status LEDs Functional Descriptions](#)). These indicators provide visual feedback on the board status and camera status.

### External Event Synchronization

Trigger inputs and strobe signals precisely synchronize image captures with external events.

### CoaXPress Communication Port

One Sopera LT Acquisition Device per camera input provides access to the CoaXPress camera configuration via the board device driver. The communication port presents a seamless interface to access GenICam camera features.

### Quadrature Shaft Encoder

An important feature for web scanning applications, the Quadrature Shaft Encoder inputs allow synchronized line captures from external web encoders (see [J7- I/O Connector](#) or [Cable assemblies for I/O connector J8](#)). The Xtium2-CXP PX8 provides a TTL or RS-422 input (mutually exclusive) that supports a maximum 5 MHz tick rate.

---

# Development Software Overview

## Sapera LT Library

Sapera LT is a powerful development library for image acquisition and control. Sapera LT provides a single API across all current and future Teledyne DALSA hardware. Sapera LT delivers a comprehensive feature set including program portability, versatile camera controls, flexible display functionality and management, plus easy to use application development wizards. Applications are developed using either C++ or .NET frameworks.

Sapera LT comes bundled with CamExpert, an easy-to-use camera configuration utility to help configure and test parameter settings of devices, and create or modify existing camera configuration files. Sapera LT also includes extensive documentation and compiled demos and example programs with project source code for recent versions of Microsoft Visual Studio®.

## Sapera Processing Library

Sapera Processing is a comprehensive set of C++ classes or .NET classes for image processing and analysis. Sapera Processing offers highly optimized tools for image processing, blob analysis, search (pattern recognition), OCR and barcode decoding.

## About CoaXPress

CoaXPress (CXP) is an asymmetric high-speed point-to-point serial communication standard for the transmission of video and still images, scalable over single or multiple coaxial cables. It supports cable speeds of up to 12.5 Gbps for video, images and data, plus a lower speed uplink up to 40 Mbps for communications and control. Power is also available over the cable ("Power-over-Coax") and cable lengths of greater than 100 m may be achieved.

The CoaXPress standard is hosted by the Japanese Industrial Imaging Association ([JIIA](#)) and has working groups from companies around the world.

# Quick Start Setup & Installation

The following procedure outlines the basic steps required to install the Teledyne DALSA Xtium2-CXP PX8. For complete installation details and information, see [Installing Xtium2-CXP PX8](#).

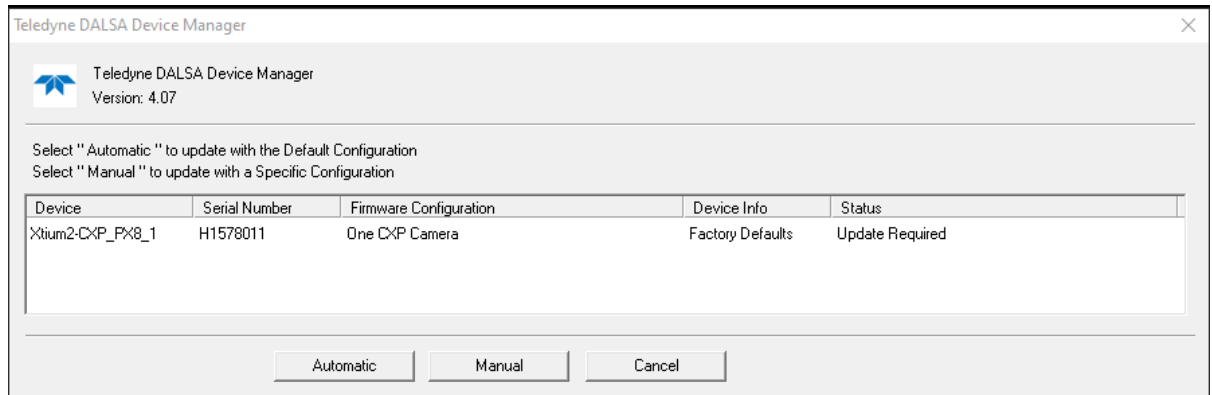
<b>1</b>	<p>Install the Xtium2-CXP PX8 in an available <u>PCIe x8</u> slot on the host computer.</p>						
	<p>Download and install the Sopera LT SDK software from the Teledyne DALSA website. <a href="http://www.teledynedalsa.com/en/products/imaging/vision-software/sopera-lt/download/">www.teledynedalsa.com/en/products/imaging/vision-software/sopera-lt/download/</a></p>						
<b>2</b>	 <table border="1"><thead><tr><th>Description</th><th>Version</th><th>Release date</th></tr></thead><tbody><tr><td><a href="#">Sopera LT SDK (full version) - Free Download</a></td><td>8.32</td><td>2018-06-20</td></tr></tbody></table>	Description	Version	Release date	<a href="#">Sopera LT SDK (full version) - Free Download</a>	8.32	2018-06-20
Description	Version	Release date					
<a href="#">Sopera LT SDK (full version) - Free Download</a>	8.32	2018-06-20					
<b>3</b>	<p>Download and install the Xtium2-CXP PX8 device driver from the Teledyne DALSA website. <a href="http://www.teledynedalsa.com/en/support/downloads-center/device-drivers/">www.teledynedalsa.com/en/support/downloads-center/device-drivers/</a></p>						
							

4

To complete the installation, update the Xtium2-CXP PX8 firmware when prompted (see [Xtium2-CXP PX8 Firmware Update](#)):

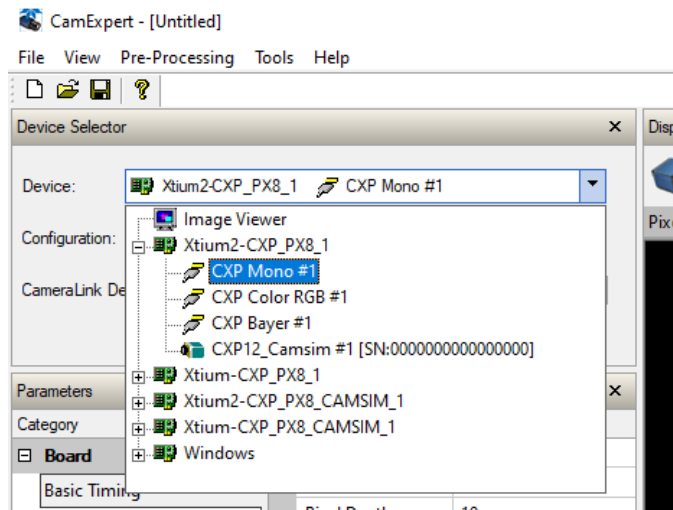
- Select **Automatic** to update the firmware with the default configuration,
- OR
- Select **Manual** to choose an alternate configuration.

Restart the computer when all software and board drivers are installed.



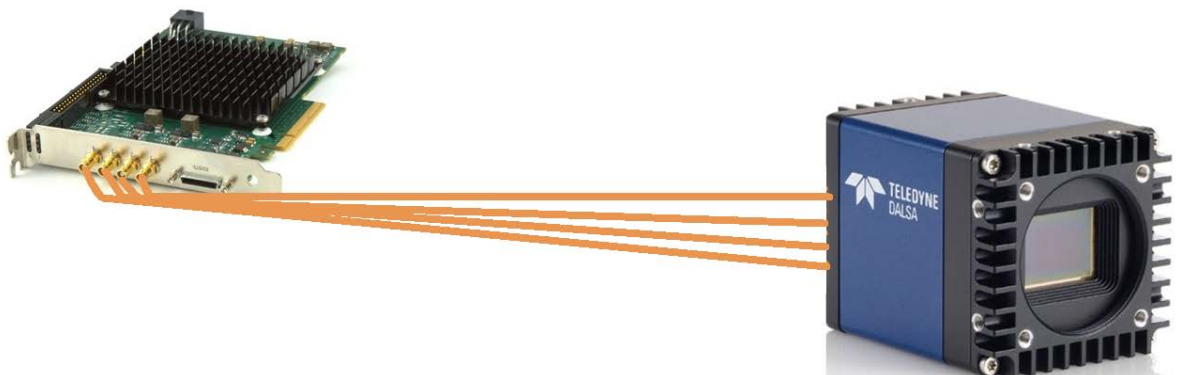
5

Open [Sapera CamExpert](#) to verify the installation; the board should be present in the list of available devices.



6

Connect camera to the board Camera CXP input connector. Ensure camera is properly powered.

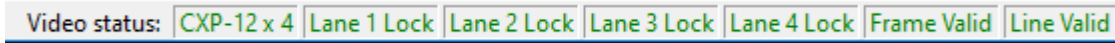


7

When CamExpert detects a camera (as per the CXP device discovery protocol), camera parameters are displayed along with the board parameters.

Category	Parameter	Value
Attached Camera - Xtiu...	Camera Type	Areascan
	Color Type	Monochrome
	Pixel Depth	8
	Data Lanes	4
	Horizontal Active...	4096
	Vertical Active (in...	3072
	Bit Transfer Rate	12.500 Gb/s
	PoCXP	Enable
	PoCXP Status	Active

When properly connected, the video status bar displays camera signals in green.



8

Click **Grab** to acquire a test image to validate the setup.

CamExpert - [Untitled]

Device: Xtiu2-CXP\_PX8\_1 CXP Mono 01

Resolution: 4096 Pixels x 3072 Lines Monochrome 16-bit

Video status: CXP-12 x 4 Lane 1 Lock Lane 2 Lock Lane 3 Lock Lane 4 Lock Frame Valid Line Valid PoCXP PoCXP 2 PoCXP 3 PoCXP 4



9

Modify the board and camera parameters as necessary. When completed, select **File > Save Configuration** to save the camera configuration file.

Save Camera file

Camera Configuration Description

Company Name: No Name

Model Name: No Name

Camera Mode: Default Camera Link HS Line Scan Mono

Configuration: Default Camera Link HS Line Scan Mono

File Information

File name: N\_No\_Name\_Default\_Default

Save as: Camera configuration file (.ccf)

Current: C:\Program Files\Teledyne DALSA\Sapera\CamFiles\

Select Custom Directory

Browse...

Save Cancel

The Xtium2-CXP PX8 can be configured using the parameter settings in this file when using the Sapera LT API in your application to acquire images.

# Installing Xtium2-CXP PX8

---

## Warning! (Grounding Instructions)

Static electricity can damage electronic components. Please discharge any static electrical charge by touching a grounded surface, such as the metal computer chassis, before performing any hardware installation. If you do not feel comfortable performing the installation, please consult a qualified computer technician.



**Important:** Never remove or install any hardware component with the computer power on. Disconnect the power cord from the computer to disable the power standby mode. This prevents the case where some computers unexpectedly power up when a board is installed.

---

## Installation Overview

The installation sequence is as follows:

- Turn off the computer.
- Install the board hardware into an available PCI Express x8 Gen3 slot.
- Turn on the computer.
- Install the Sapera LT Development Library or only its runtime library.
- Install the Xtium2-CXP PX8 Sapera board driver.
- Update the board firmware if required.
- Restart the computer.
- Connect a CXP camera and test.

## Hardware Installation

- Turn the computer off, disconnect the power cord (disables power standby mode), and open the computer chassis to allow access to the expansion slot area.
- Install the Xtium2-CXP PX8 into a free PCI Express x8 Gen3 expansion slot. Note that some computer's x16 slot may support boards such as the Xtium2-CXP PX8, not just display adapters.
- Connect a spare power supply connector to J10 for PoCXP cameras (J10: Power Connector). See Power Cable Assembly OR-YXCC-PWRY00 for information about an adapter for older computers.
- Close the computer chassis and turn the computer on.
- Log into Windows with an administrator account.
- Connect a CXP camera to the C1, C2, C3 and C4 camera connectors after installing Sapera as described below.
- Test with CamExpert.

## Multi-board Sync & I/O Setup

- For multi-board sync applications, see J9: Multi-Board Sync / Bi-directional General I/Os for information on using two to four Xtium2-CXP boards in one computer.

# Sapera LT Library & Xtium2-CXP PX8 Driver Installation

You need to download the Sapera LT SDK and the board device driver:

- **Sapera LT SDK (full version)**, the image acquisition and control SDK for Teledyne DALSA cameras and frame grabbers is available for download from the Teledyne DALSA website: [www.teledynedalsa.com/en/products/imaging/vision-software/sapera-lt/download/](http://www.teledynedalsa.com/en/products/imaging/vision-software/sapera-lt/download/)

Run-time versions are also available for download at this location.



The Sapera LT SDK installation includes compiled demo and example programs, along with project source code, in both C++ and .NET languages, for most Microsoft Visual Studio® development platforms. The Sapera LT ++ and Sapera LT .NET demo source code is found in the Sapera\Demos directory.

- **Teledyne DALSA Device Driver**. All Teledyne DALSA device drivers are available for download from the Teledyne DALSA website: [www.teledynedalsa.com/en/support/downloads-center/device-drivers/](http://www.teledynedalsa.com/en/support/downloads-center/device-drivers/)

## Installation Procedure

Install Sapera LT **before** Teledyne DALSA board drivers.

- Run the Sapera LT SDK executable file; the installation menu is presented.
- The installation program may prompt to restart the computer. It is not necessary to reboot the computer between the installation of Sapera LT and the board driver.
- Run the Xtium2-CXP PX8 device driver executable file; the installation menu is presented.
- During the late stages of the installation, the Xtium2-CXP PX8 firmware update application starts. This is described in detail in the following section.
- Restart the computer when all the software and board drivers are installed.



If Windows displays any unexpected message concerning the board, power off the system and verify the Xtium2-CXP PX8 is installed in the slot properly. You should also note the board's status LED color and compare it to the defined LED states as described in [S: Boot-up/PCIe Status LED](#).

Refer to *Sapera LT User's Manual* for additional details about Sapera LT.

## Xtium2-CXP PX8 Firmware Update

The Device Manager's Firmware Update program automatically executes at the end of the driver installation and on every subsequent restart of the computer. It will determine if the Xtium2-CXP PX8 requires a firmware update. If firmware is required, a dialog opens. This dialog also allows the user to load alternative firmware if available for the Xtium2-CXP PX8.

Note: Administrator rights are required to update the device information and/or firmware.



**Important:** In the rare case of firmware update errors please see [Recovering from a Firmware Update Error](#).

## Firmware Update: Automatic Mode

- Select **Automatic** to update the Xtium2-CXP PX8 firmware.

The Xtium2-CXP PX8 supports various firmware configurations where the default can acquire from a 1, 2 or 4 lane CXP camera.

See [User Programmable Configurations](#) for details on all supported modes, selected via a manual update of alternative firmware.

With multiple Xtium2-CXP PX8 boards in the system, all are updated with new firmware. If any installed Xtium2-CXP PX8 board installed in a system already has the correct firmware version, an update is not required. In the following screen shot, a single Xtium2-CXP PX8 board is installed and ready for a firmware upgrade.

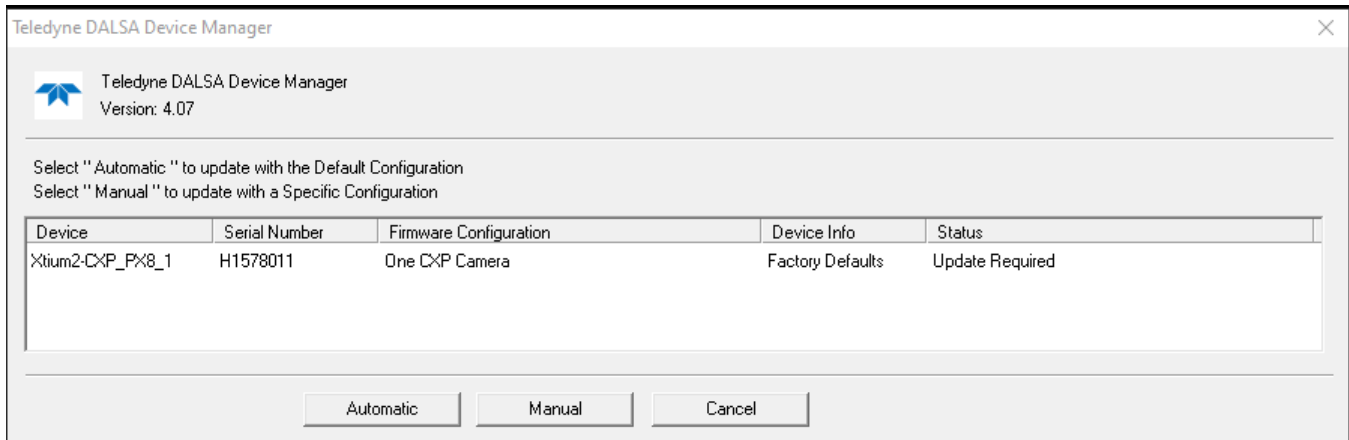


Figure 1: Automatic Firmware Update

## Firmware Update: Manual Mode

- Select **Manual** to load firmware other than the default version or, in the case of multiple Xtium2-CXP PX8 boards in the same system, if each requires a different firmware.

The Device Manager utility opens on the Device Update page, which displays information on all installed Xtium2-CXP PX8 boards, their serial numbers, and their firmware components.

### To perform a manual firmware update

- Select the Xtium2-CXP PX8 to update in the **Device** column (if there are multiple boards in the system).
- From the **Configuration** list, select the firmware version required (typical required or offered to support different CXP cameras).
- Click **Start Update**.

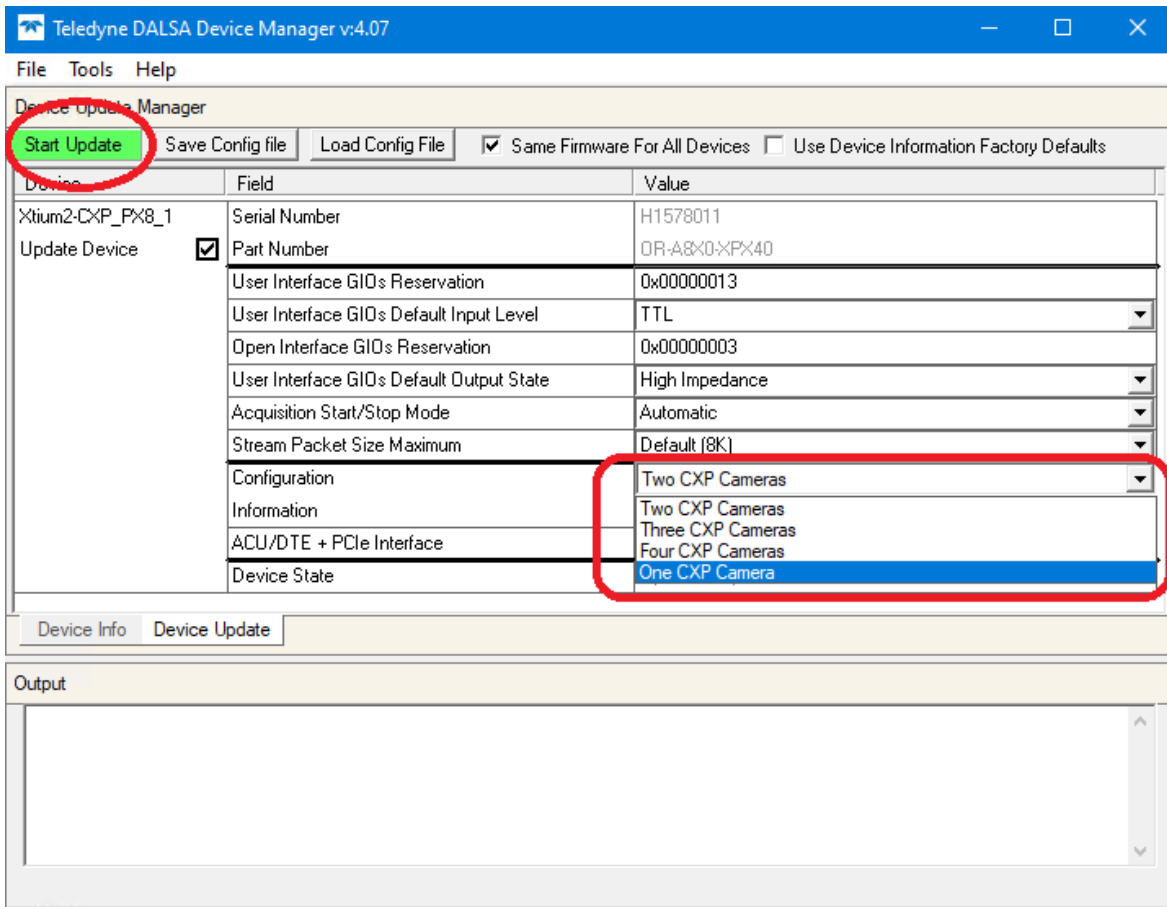


Figure 2: Manual Firmware Update

- The **Output** pane will display the firmware update progress.
- Close the Device Manager program when the device reset complete message is shown.

### ***Executing the Firmware Update program from the Start Menu***

The Xtium2-CXP PX8 Firmware Update program can be executed via the **Start** menu under **Teledyne DALSA Xtium2-CXP PX8 > Firmware Update**.

A firmware change after installation would be required to select a different configuration mode. See [User Programmable Configurations](#).

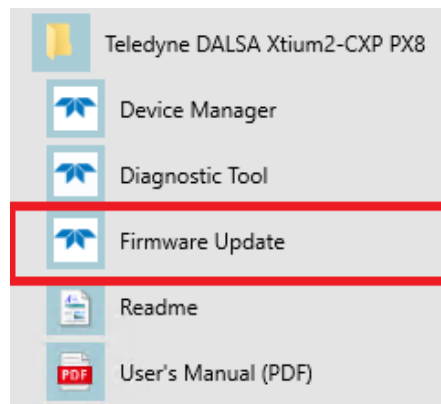


Figure 3: Start Menu Firmware Update Shortcut

---

# Upgrading Sopera or Board Driver

When installing a new version of Sopera or a Teledyne DALSA acquisition board driver in a computer with a previous installation, the current version **must** be uninstalled first.

Described below are two upgrade situations. Note that if the board is installed in a different slot, the new hardware wizard opens. Answer as instructed in the section [Hardware Installation](#).

## Board Driver Upgrade Only

Minor upgrades to acquisition board drivers are distributed as .zip files available in the Teledyne DALSA web site [www.teledynedalsa.com/en/support/downloads-center/device-drivers/](http://www.teledynedalsa.com/en/support/downloads-center/device-drivers/).

These minor upgrades typically do not require a new revision of Sopera. To confirm that the current Sopera version will work with the new board driver:

- Check the new board driver's ReadMe file before installing, for information on the minimum Sopera version required.
- If the ReadMe file does not specify the Sopera version required, contact Teledyne DALSA Technical Support (see [Technical Support](#)).

### To upgrade the board driver only

The procedure assumes Windows 10/11.

1. Logon the computer as an administrator or with an account that has administrator privileges.
2. In the taskbar search box, type *Control Panel* and open it.
3. Select **Programs and Features**.
4. Select Teledyne DALSA Xtium2-CXP PX8 Device Driver and click **Uninstall**.
5. Install the new board driver. Run **Setup.exe** if installing manually from a downloaded driver file.



You cannot install a Teledyne DALSA board driver without Sopera LT installed on the computer.

## Upgrading both Sopera and Board Driver

When upgrading both Sopera and the acquisition board driver, follow the procedure described below.

### To upgrade the board driver and Sopera LT

The procedure assumes Windows 10/11.

1. Logon the computer as an administrator or with an account that has administrator privileges.
2. In the taskbar search box, type *Control Panel* and open it.
3. Select **Programs and Features**.
4. Select Teledyne DALSA Xtium2-CXP PX8 Device Driver and click **Uninstall**.
5. Select Teledyne DALSA Sopera LT and click **Uninstall**.
6. Restart the computer and logon the computer as an administrator again.
7. Install the new versions of Sopera LT and the board driver as in a first-time installation. See [Sopera LT Library & Xtium2-CXP PX8 Driver Installation](#) for installation procedures.

## Preserving Board Parameters during Driver Upgrade

User-defined parameter settings for previously installed boards can be preserved when upgrading a device driver by using an install.ini file as described in [Custom Driver Installation using install.ini](#).

- To apply the settings specified in the install.ini file, select **Automatic** on the Device Manager start-up dialog.
- To verify the settings specified in the install.ini file, select **Manual**; differences between the current device settings are shown in **green** in both the **Device Info** and **Device Update** tabs.

The screenshot shows the 'Device Update Manager' window for 'Xtium2-CXP\_PX8\_1'. The 'Update Device' checkbox is checked. The table below shows the current settings, with green text indicating differences from factory defaults.

Device	Field	Value
Xtium2-CXP_PX8_1	Serial Number	H1578011
Update Device <input checked="" type="checkbox"/>	Part Number	OR-A8X0-XPX40
	User Interface GIOs Reservation	0x00000033
	User Interface GIOs Default Input Level	24V
	Open Interface GIOs Reservation	0x00000003
	User Interface GIOs Default Output State	High Impedance
	Acquisition Start/Stop Mode	Automatic
	Stream Packet Size Maximum	Default (8K)
	Configuration	Two CXP Cameras
	Information	Support for 2 independent CXP cameras of 1 or 2 links each.
	ACU/DTE + PCIe Interface	1.00.01.0017
	Device State	Update Not Required

Figure 4: Device Manager Parameter Setting Differences

Upgrading without an install.ini file requires selecting **Manual** on the Device Manager start-up dialog and setting the required parameters manually.



**Note:** Without an install.ini file, configuration information is not preserved and is always set to factory default.

# Preserving Board Parameters during Board Replacement or System Cloning

When replacing a board in a system or cloning a system configuration using a hard drive image, if the previous device parameter settings differ from the factory default driver settings it is indicated as *User Defined* or *Manual Configuration* in the Teledyne DALSA Device Manager start-up dialog under the **Device Info** column. User-defined settings are specific to the PCI Express slot on the system.

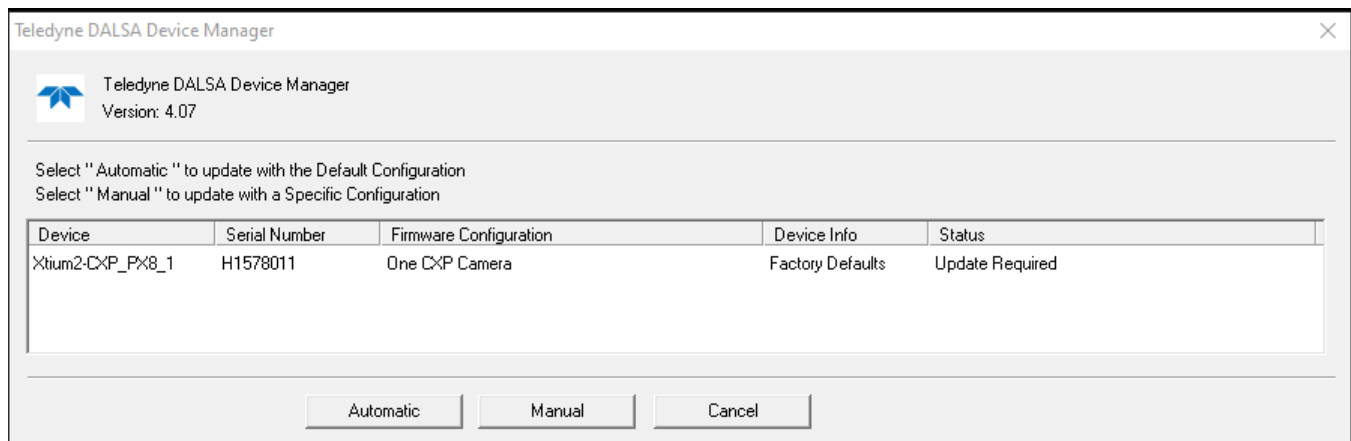


Figure 5: Firmware Update Status

To preserve the user defined parameter settings, select **Manual** and proceed with the update; differences between the current settings are shown in green in both the **Device Info** and **Device Update** tabs.

For systems with multiple boards, if boards use different firmware configurations, first clear the **Same Firmware For All Devices** option (otherwise the configuration specified for the first board according to slot position is applied to all boards in the system).

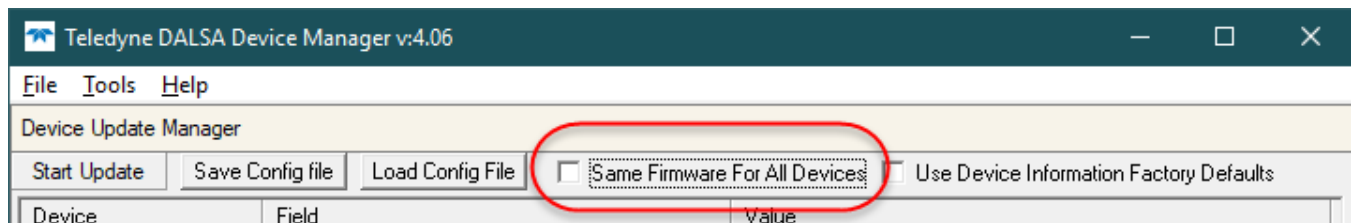


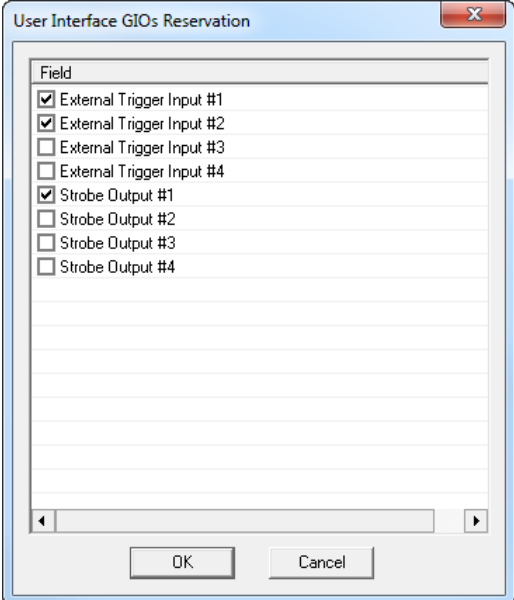
Figure 6: Same Firmware For All Devices Checkbox

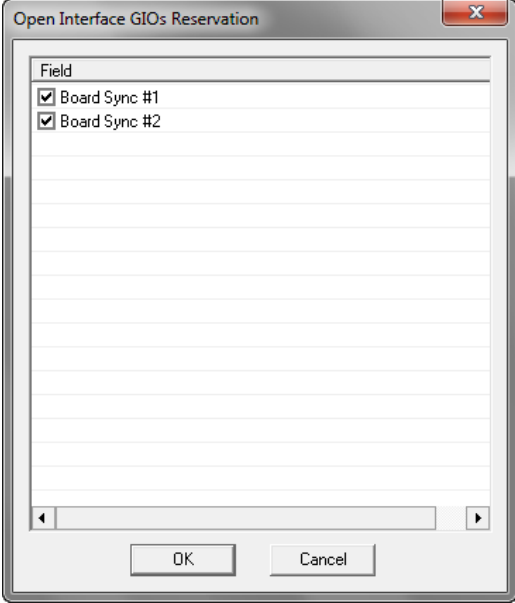
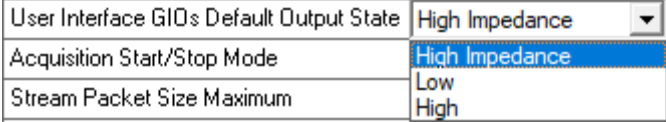



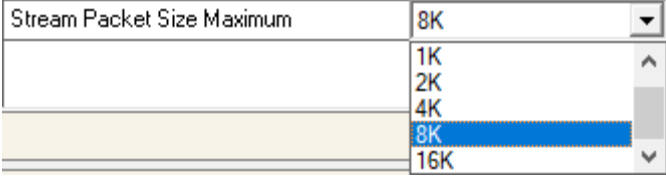


# Information Field Description

Field	Description
Serial Number	[Read-Only]: Serial Number of the board
Hardware ID	[Read-Only]: This field identifies future hardware changes affecting the operation of the board. Currently there are no such changes.
Hardware Configuration	[Read-Only]: This field states the presence or absence of optional components. Possible values are: <ul style="list-style-type: none"> <li>• <b>0x0000000000000001</b></li> </ul> <b>Bit 0:</b> Both Shaft Encoder RS-422 and TTL input is supported .
Video Lanes	[Read-Only]: Indicates the maximum number of video lanes supported by the board. 1CH/OR-A8X0-XPX10: 1 2CH/OR-A8X0-XPX20: 2 4CH/OR-A8X0-XPX40: 4 4CH/OR-A8X6-XPX40: 4
User Interface Outputs	[Read-Only]: Number of available user interface outputs on the board. For this board, the value is 8.
P/N	[Read-Only]: Indicates the part number of the board. OR-A8X0-XPX10: 1CH board OR-A8X0-XPX20: 2CH board OR-A8X0-XPX40: 4CH board OR-A8X6-XPX40: 4CH CXP6 DIN connectors board
P/N Revision	[Read-Only]: Indicates the revision of the part number.
Maximum Bit Rate in Gbps	[Read-Only]: Indicates the maximum bit rate supported by the device. OR-A8X0-XPX10: 12.500 OR-A8X0-XPX20: 12.500 OR-A8X0-XPX40: 12.500 OR-A8X6-XPX40: 6.250
User Data	[Read/Write]: This is a 64-byte general-purpose user storage area. For information on how to read/write this field at the application level, contact Teledyne DALSA Technical Support.

Field	Description								
User Interface GIOs Reservation	<p>[Read/Write]: Use this field to reserve User Interface GIOs for use by the acquisition module. By default, boards are shipped with User Interface General Inputs 1 &amp; 2 reserved for External Triggers and User Interface General Output 1 reserved for Strobe Output.</p> <p>Click on the 'Value' field to open the dialog box shown below. Disable any GIO reservations that are not required. Click <b>OK</b> to update the value field.</p> 								
User Interface GIOs Default Input Level	<p>[Read/Write]: Use this field to select the default input level of the User Interface GIOs. By default, boards are shipped with inputs set for 24V signaling. Note that the input level can also be modified at the application level.</p> <p>Click on the 'Value' field to open the drop selection shown below. Select the input signal level-detection required.</p> <table border="1" data-bbox="521 1224 1182 1371"> <tr> <td>User Interface GIOs Default Input Level</td> <td>24V</td> </tr> <tr> <td>Open Interface GIOs Reservation</td> <td>TTL</td> </tr> <tr> <td>User Interface GIOs Default Output State</td> <td>24V</td> </tr> <tr> <td>Acquisition Start/Stop Mode</td> <td>RS422</td> </tr> </table>	User Interface GIOs Default Input Level	24V	Open Interface GIOs Reservation	TTL	User Interface GIOs Default Output State	24V	Acquisition Start/Stop Mode	RS422
User Interface GIOs Default Input Level	24V								
Open Interface GIOs Reservation	TTL								
User Interface GIOs Default Output State	24V								
Acquisition Start/Stop Mode	RS422								

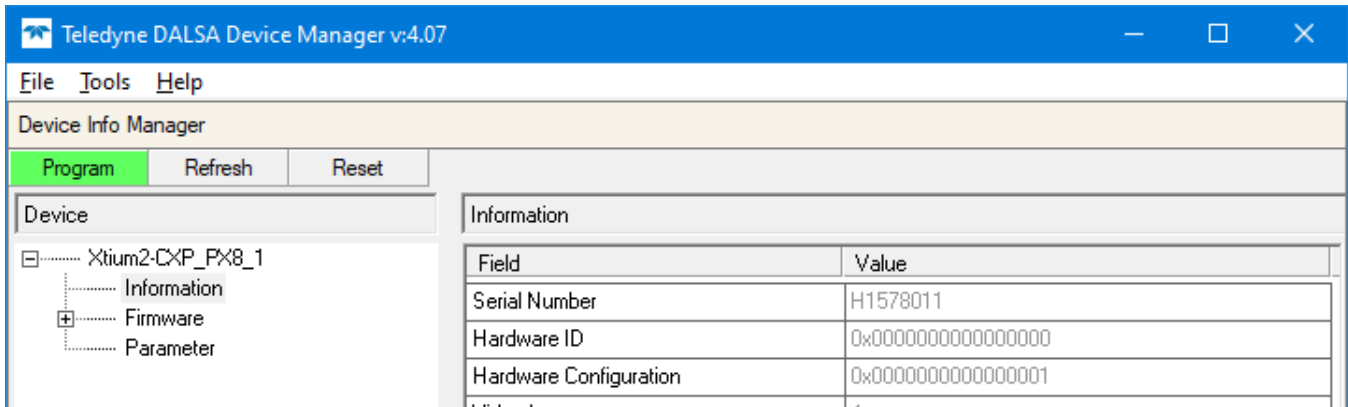
Field	Description
Open Interface GIOs Reservation	<p>[Read/Write]: Use this field to reserve Open Interface GIOs for use by the acquisition module.</p> <p>To specify the open interface GIO reservations, click on the 'Value' field. Disable any GIO reservations that are not required. Click <b>OK</b> to update the value field.</p>  <p>By default, boards are shipped with Open Interface GIOs 1 &amp; 2 reserved for Board Sync 1 &amp;</p>
User Interface GIOs Default Output State	<p>[Read/Write]: Use this field to select the default Output State of the User Interface GIOs.</p> <p>Click on the 'Value' field to select the output state required.</p>  <p>By default, boards are shipped with User Interface General Outputs set to High Impedance.</p> <p>Note that the output state can also be modified at the application level.</p>
Acquisition Start/Stop Mode	<p>[Read/Write]: Use this field to indicate if frame grabber driver will automatically call the AcquisitionStart/AcquisitionStop camera feature upon connecting/disconnecting the transfer respectively.</p> <p>Click on the 'Value' field to open the dialog box show below.</p>  <p>By default, boards are shipped with this option set to 'Automatic'.</p>

Field	Description
Stream Packet Size Maximum	<p>[Read/Write]: Use this field to indicate the maximum stream packet size the frame grabber will allow. A higher value will reduce the overhead of sending video data and can avoid overflow of data.</p> <p>Click on the 'Value' field to open the dialog box show below. By default, boards are shipped with this option set to '8K'.</p> 

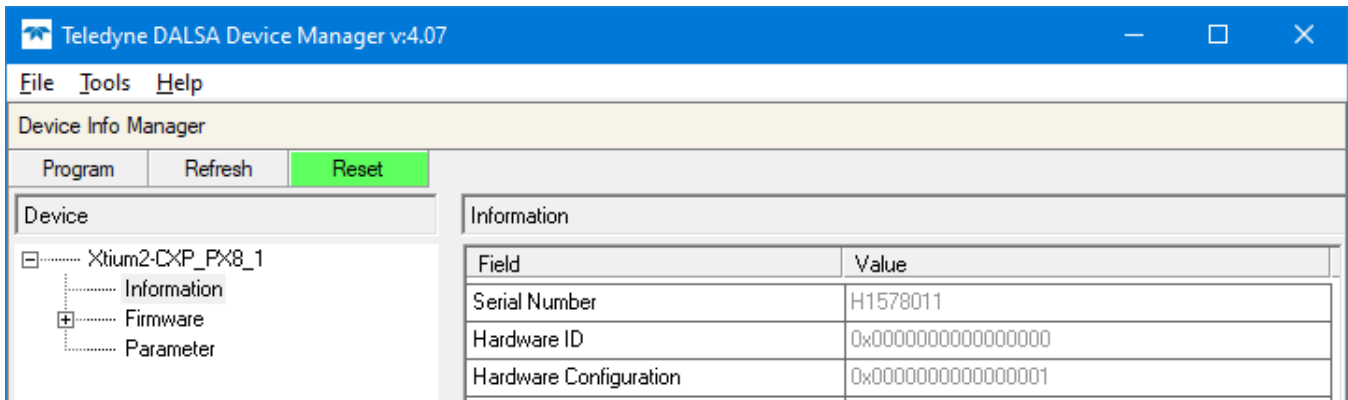
## Changing Device Settings

When device settings are changed, the board must be programmed and reset to effect the changes.

If board programming is required, the **Program** button is displayed in green; click **Program** to start programming.



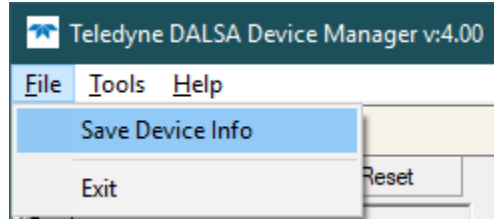
When programming is complete, the **Reset** button is displayed in green; click **Reset** to reset the board.



## Device Information Report

Teledyne DALSA Technical Support may request a device information report file (BoardInfo.txt) to aid in troubleshooting installation or operational problems.

To generate the Xtium2-CXP PX8 device information report file, select **File > Save Device Info**.



*Figure 8: Device Manager File Menu save Device Info Command*

---

# Configuring Sopera

The **Sopera Configuration** program (on the **Start** menu, select **Teledyne DALSA Sopera LT > Sopera Configuration**) allows the user to see all available Sopera servers for the installed Sopera-compatible boards.

The **System** entry represents the system server. It corresponds to the host machine (your computer) and is the only server that should always be present.

## Increasing Contiguous Memory for Sopera Resources

The **Contiguous Memory** section lets the user specify the total amount of contiguous memory (a block of physical memory, occupying consecutive addresses) reserved for the resources needed for **Sopera buffers** allocation and **Sopera messaging**. For both items, the **Requested** value dialog box shows the *CorMem* driver default memory setting while the **Allocated** value displays the amount of contiguous memory allocated successfully. The default values will generally satisfy the needs of most applications.

The *Buffer Allocation (Legacy)* and *Buffer Allocation (64-bit)* value determines the total amount of contiguous memory reserved at boot time for the allocation of dynamic resources used for frame buffer management such as scatter-gather list, DMA descriptor tables plus other kernel needs. We recommend using the *64-bit* choice for the Xtium2-CXP PX8 in order to reserve this memory anywhere in PC memory and not just limited to the 1<sup>st</sup> 4 GB of physical memory as would be the case using the *Legacy* one.

Adjust this value higher if your application generates any out-of-memory error while allocating host frame buffers or when connecting the buffers via a transfer object. You can approximate the worst-case scenario amount of contiguous memory required as follows:

- Calculate the total amount of host memory used for one frame buffer [number of pixels per line \* number of lines \* (2 - if buffer is 10/12/14 or 16 bits)].
- Provide 200 bytes per frame buffer for Sopera buffer resources.
- Provide 64 bytes per frame buffer for DMA metadata. Memory for this data is reserved in chunks of 64 kB blocks.
- Provide 48 bytes per frame buffer for buffer management. Memory for this data is reserved in chunks of 64 kB blocks.
- For each frame buffer DMA table, allocate 24 bytes + 8 bytes for each 4 kB of buffer. For example, for a 120x50x8 image:  $120 \times 50 = 6000 = 1.46 \text{ kB blocks} \rightarrow \text{roundup to 2 blocks of 4kB}$ . Therefore  $24 \text{ bytes} + (2 * 8 \text{ bytes}) = 40 \text{ bytes}$  for DMA tables per frame buffer. Memory for this data is reserved in chunks of 64 kB blocks. If vertical flipping is enabled, one must add 16 bytes per line per buffer. For example, for an image 4080x3072 image:  $16 \text{ bytes} * 3072 = 49152 \text{ bytes}$ .



**Note 1:** Sopera LT reserves the 1<sup>st</sup> 5 MB for its own resources, which includes the 200 bytes per frame buffer mentioned above.

**Note 2:** Contiguous memory can be allocated anywhere in PC memory using the *Buffer Allocation (64-bit)* entry in Sopera Configuration Tool. The driver will use this memory 1<sup>st</sup> for frame buffer DMA tables.

Test for any memory error when allocating host buffers. Simply use the **Buffer** menu of the Sopera Grab demo program (see [Grab Demo Overview](#)) to allocate the number of host buffers required for your acquisition source. Feel free to test the maximum limit of host buffers possible on your host system – the Sopera Grab demo will not crash when the requested number of host frame buffers is not allocated.

The following calculation is an example of the amount of contiguous memory to reserve beyond 5 MB with 80,000 buffers of 2048x1024x8:

a)  $(80000 * 64 \text{ bytes})$

b)  $(80000 * 48 \text{ bytes})$

c)  $(80000 * (24 + (((2048*1024)/4\text{kB}) * 8))) = 314 \text{ MB}$

d) Total = a (rounded up to nearest 64kB) + b (rounded up to nearest 64kB) + c (rounded up to nearest 64kB) = 323MB.

## ***Host Computer Frame Buffer Memory Limitations***

When planning a Sopera application and its host frame buffers used, plus other Sopera memory resources, do not forget the Windows operating system memory needs.

A Sopera application using the preferred *scatter gather buffers* could consume most of the remaining system memory, with a large allocation of frame buffers. If using frame buffers allocated as a *single contiguous memory block*, Windows will limit the allocation dependent on the installed system memory. Use the **Buffer** menu of the [Sopera Grab demo](#) program to allocate host buffer memory until an error message signals the limit allowed by the operating system used.

## ***Contiguous Memory for Sopera Messaging***

The current value for **Sopera messaging** determines the total amount of contiguous memory reserved at boot time for messages allocation. This memory space stores arguments when a Sopera function is called. Increase this value if you are using functions with large arguments, such as arrays and experience any memory errors.



# CamExpert Quick Start

## Interfacing CXP Cameras with CamExpert

CamExpert is the camera-interfacing tool for Teledyne DALSA frame grabber boards supported by the Sopera library. CamExpert generates the Sopera camera configuration file (*yourcamera.ccf*) based on timing and control parameters entered. For backward compatibility with previous versions of Sopera, CamExpert also reads and writes the .cca and .cvi camera parameter files.

Every Sopera demo program starts with a dialog window to select a camera configuration file. Even when using the Xtium2-CXP PX8 with common video signals, a camera file is required. Therefore, CamExpert is typically the first Sopera application run after an installation. Obviously existing .ccf files can be copied to any new board installations when similar cameras are used.

## CamExpert Example with a Monochrome Camera

The image below shows CamExpert controlling the Xtium2-CXP PX8. In this example, the CXP camera has 4 data lanes connected.

When the camera is identified (as per the CXP device discovery protocol), the timing parameters are displayed. The user can test by clicking **Grab**. Descriptions of the CamExpert sections follow the image.

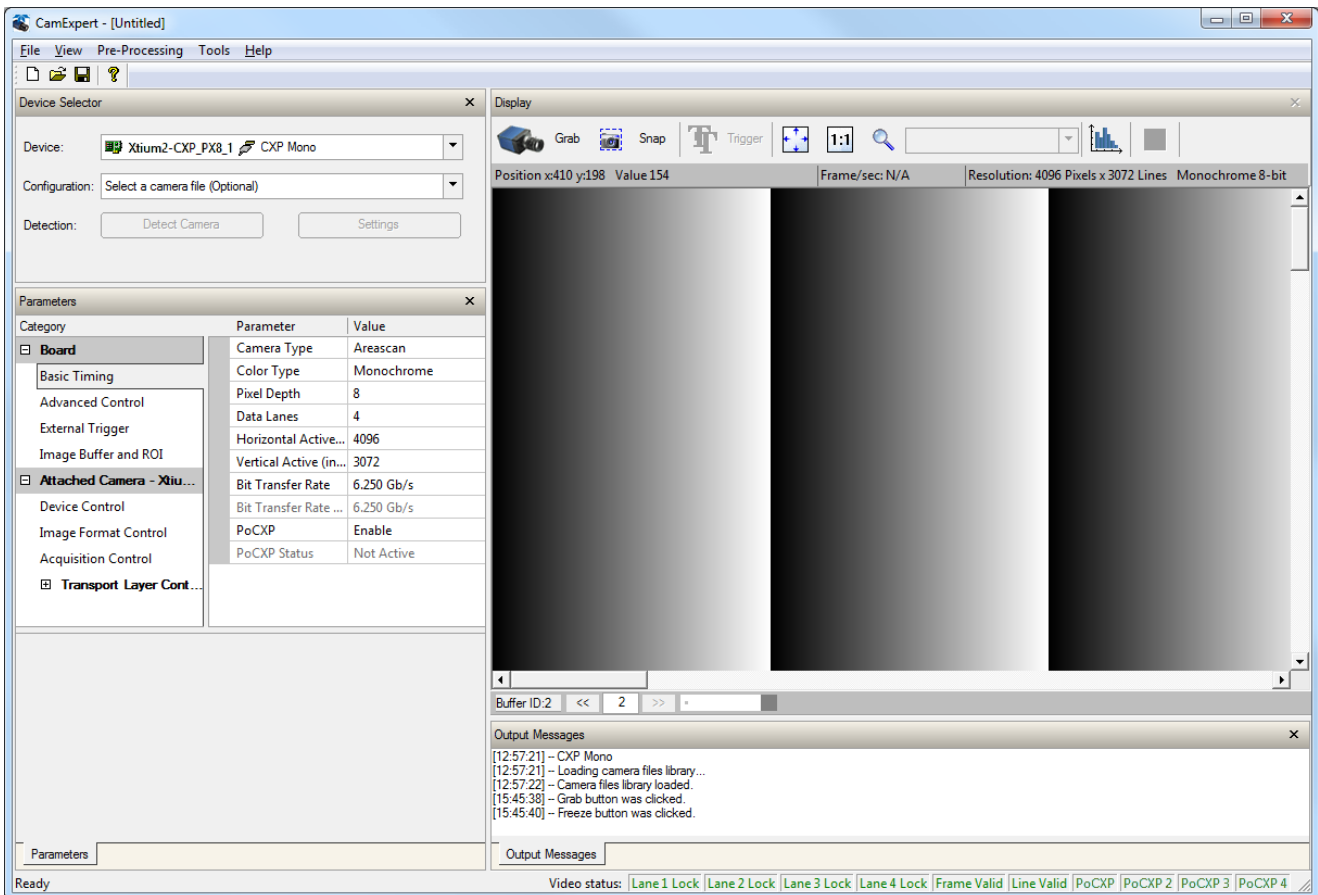


Figure 9: CamExpert Program

CamExpert groups camera features into functional categories. The features shown depend on the frame grabber used and what camera is connected. The values are either the camera defaults or the last stored value when the camera was used. The general descriptions below are not specific to a particular camera.

- **Device Selector:** Select a device and configuration from the lists.
  - **Device:** Select which acquisition device to control and configure a camera file. Required in cases where there are multiple boards in a system and when one board supports multiple acquisition types. Note in this example, the installed Xtium2-CXP PX8 has firmware to support a monochrome or color RGB CoaXPress camera.

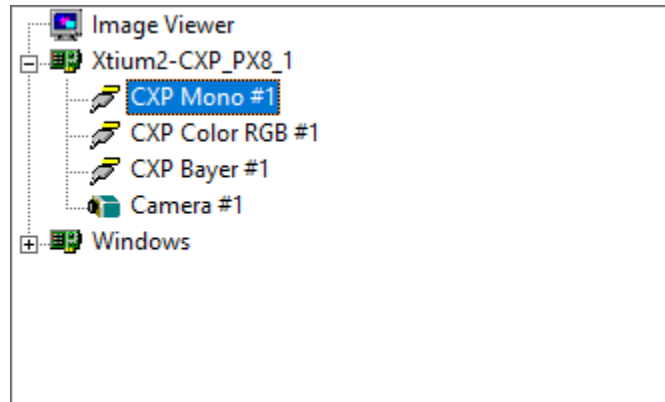


Figure 10: CamExpert Device Tree

- **Configuration:** Select the timing for a specific camera model included with the Sapera installation or a standard video standard. The *User's* subsection is where user created camera files are stored.
- **Parameter:** Select a function category and change parameter values as required. Descriptions for the camera parameters change dependent on the camera.
  - **Basic Timing:** Provides or changes static camera parameters.
  - **Advanced Controls:** Advanced parameters used to select various integration methods, frame trigger type, Camera CXP controls, etc.
  - **External Trigger:** Parameters to configure the external trigger characteristics.
  - **Image Buffer and ROI:** Allows control of the host buffer dimension and format.
- **Display:** An important component of CamExpert is its live acquisition display window, which allows immediate verification of timing or control parameters without the need to run a separate acquisition program. **Grab** starts continuous acquisition (button then toggles to **Freeze** to stop). **Snap** is a single frame grab. **Trigger** is a software trigger to emulate an external source.
- **Output Messages** pane and **Video Status** line: Events and errors are logged for review. Camera connection status is displayed where green indicates connected signals present.

---

# CamExpert Demonstration and Test Tools

The CamExpert utility also includes a number of demonstration features, which make CamExpert the primary tool to configure, test and calibrate your camera and imaging setup. Display tools include image pixel value readout, image zoom, and line profiler.

Functional tools include support for either hardware based or software Bayer filter camera decoding with auto white balance calibration.

## Camera Types & Files

The Xtium2-CXP PX8 supports digital area scan or line scan cameras using the Camera CXP interface standard.

### Camera Files Distributed with Sopera

The Sopera distribution includes camera files (.cca extension) for a selection of Xtium2-CXP PX8 supported cameras (Teledyne DALSA\Sopera\CamFiles). Using the Sopera CamExpert program, you may use the camera files provided to generate a camera configuration file (.ccf) that describes the desired camera and frame grabber configuration.

Teledyne DALSA continually updates a camera application library composed of application information and prepared camera files. Camera files are ASCII text, readable with Windows Notepad on any computer without having Sopera installed.

## Overview of Sopera Acquisition Parameter Files (.ccf or .cca/.cvi)

### Concepts and Differences between the Parameter Files

There are two components to the legacy Sopera acquisition parameter file set: CCA files (also called cam-files) and CVI files (also called VIC files, video input conditioning). The files store respectively video-signal parameters (CCA) and video conditioning parameters (CVI), which in turn simplify programming the frame grabber acquisition hardware for the camera in use.

Since Sopera LT 5.0, acquisition parameter settings are stored in a camera configuration file (.ccf or CCF) that combines the CCA and CVI files into one.

Typically, a camera application will use a CCF file per camera operating mode (or one CCA file in conjunction with several CVI files, where each CVI file defines a specific camera-operating mode). An application can also have multiple CCA/CCF files to support different image format modes supported by the camera or sensor (such as image binning or variable ROI).

### CCF File Details

A CCF file groups the camera (CCA) and frame grabber (CVI) parameters into one file, simplifying configuration file management. This is the default Camera Configuration file used with Sopera LT and CamExpert.

### CCA File Details

Teledyne DALSA distributes camera files using the legacy .cca extension, which contain all parameters describing the camera video signal characteristics and operation modes (what the camera outputs). The Sopera parameter groups within the file are:

- Video format and pixel definition
- Video resolution (pixel rate, pixels per line, lines per frame)
- Synchronization source and timing
- Channels/Taps configuration
- Supported camera modes and related parameters
- External signal assignment

## CVI File Details

Legacy files using the .cvi extension contain all operating parameters related to the frame grabber board - what the frame grabber can actually do with camera controls or incoming video. The Sopera parameter groups within the file are:

- Activate and set any supported camera control mode or control variable.
- Define the integration mode and duration.
- Define the strobe output control.
- Allocate the frame grabber transfer ROI, the host video buffer size and buffer type (RGB888, RGB101010, MONO8, and MONO16).
- Configuration of line/frame trigger parameters such as source (internal via the frame grabber /external via some outside event), electrical format (TTL, RS-422, OPTO-isolated), and signal active edge or level characterization.

## Saving a Camera File

Use CamExpert to save a CCF file usable with any Sopera demo program or user application. An example would be a camera file that sets up parameters for a free running camera (i.e. internal trigger) with exposure settings for a good image with common lighting conditions.

### To save parameters in a CCF file

1. On the **File** menu, select **Save Configuration As**.
2. Add details such as camera information, mode of operation.
3. Change or enter a file name.
4. (Optional). The default folder for user-generated .ccf files is Teledyne DALSA\Sopera\CamFiles\User. You may choose another folder by selecting **Select Custom Directory**, then choosing **Browse**.
5. Click **Save**.

## Camera Interfacing Check List

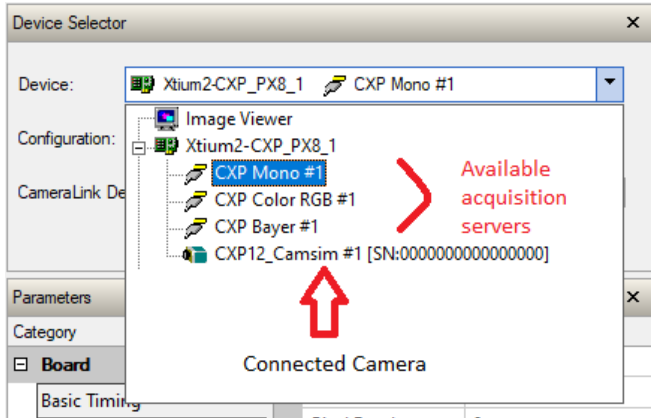
Before interfacing a camera from scratch with CamExpert:

- Confirm that Teledyne DALSA has not already published an application note with camera files [ [www.teledynedalsa.com](http://www.teledynedalsa.com) ].
- Confirm that the correct version or board revision of Xtium2-CXP PX8 is used.
- Confirm that the required firmware is loaded into the Xtium2-CXP PX8.
- Confirm that Sopera does not already have a .cca file for your camera. If there is a .cca file supplied with Sopera, then use CamExpert to generate the .ccf file with default parameter values matching the frame grabber capabilities.
- Check if the Sopera installation has a similar type of camera file. A similar .cca file can be loaded into CamExpert and modified to match timing and operating parameters for your camera; the parameters can then be saved as a .ccf file.
- Finally, if there is no file for your camera, run CamExpert after installing Sopera and the acquisition board driver, select the board acquisition server, and manually enter the camera parameters.

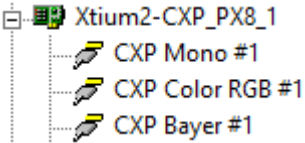
# Using CamExpert with Xtium2-CXP PX8

The Sapera CamExpert tool is the interfacing tool for Xtium2-CXP PX8 frame grabbers and connected cameras; it is supported by the Sapera library and hardware. CamExpert allows a user to test frame grabber and camera functions, and then to save the frame grabber settings as individual camera parameter files on the host system (.ccf).

When an acquisition server is selected, CamExpert only presents parameters supported by the selected device.



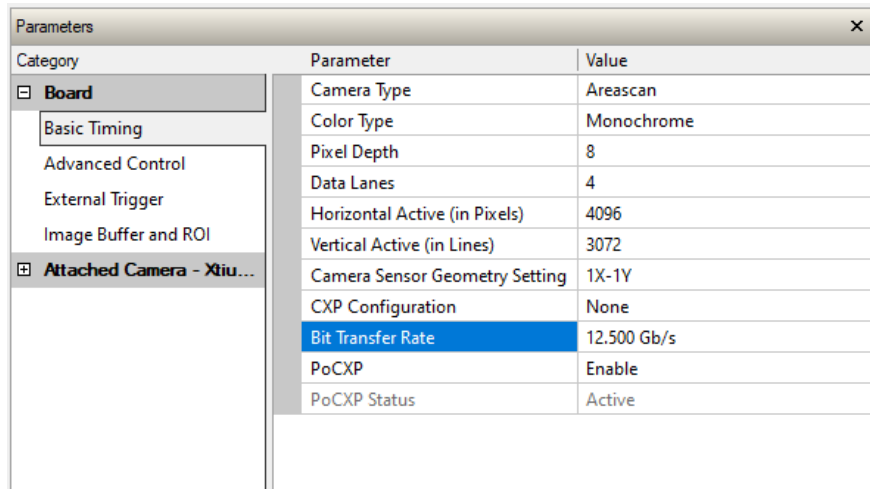
The Xtium2-CXP PX8 firmware supports multiple configurations that include support for single or multiple CXP cameras and provides the following acquisition servers:

Firmware	Acquisition Servers
One CXP Camera (default configuration)	

Depending on the selected server, different parameters may be displayed. For example, with an RGB acquisition server, the Color Type parameter is not displayed since its value is not configurable.

# Basic Timing Category

The Basic Timing category groups parameters such as camera type, the active image size, and other settings related to basic timing.



## Parameter Descriptions

The following table describes the CamExpert Basic Timing category of Spera LT parameters. Acquisition server notes, if applicable, indicate if parameter availability or supported values are dependent on the selected frame grabber acquisition server and acquisition device.

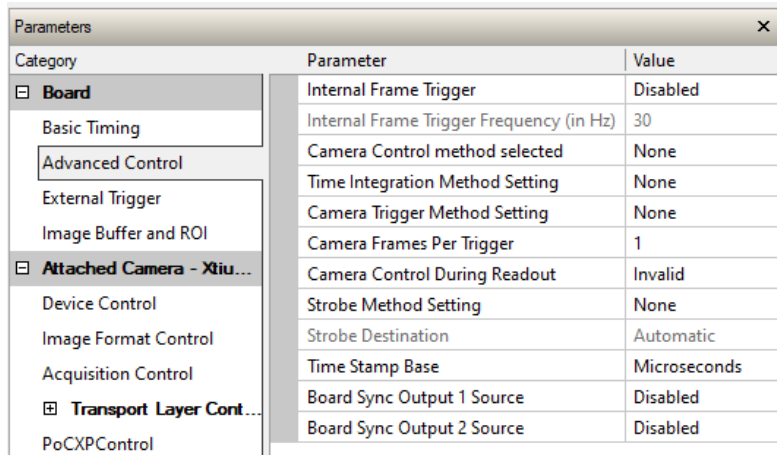
Display Name	Parameter	Description	Notes
Camera Type	<u>CORACO_PRM_SCAN</u>	Video source image type. Possible values are area scan or line scan.	Not shown for Bayer servers (areascan only).
Color Type	<u>CORACO_PRM_VIDEO</u>	Sets the color format of the input source.	Not shown for RGB servers. Monochrome servers support: Monochrome Bayer mosaic
Pixel Depth	<u>CORACO_PRM_PIXEL_DEPTH</u>	Pixel depth (bits per pixel) of the input source.	Monochrome servers support: 8, 10, 12, 14 or 16 bit Bayer and Color servers support: 8, 10 or 12 bit
Data Lanes	<u>CORACO_PRM_DATA_LANES</u>	Number of data lanes output by the camera.	
Horizontal Active (in Pixels)	<u>CORACO_PRM_HACTIVE</u>	Sets the horizontal camera resolution in pixels. This corresponds to the visible part of the image from the camera. Valid range depends on the acquisition module.	
Vertical Active (in Lines)	<u>CORACO_PRM_VACTIVE</u>	Sets the vertical camera resolution in lines per frame. This corresponds to the visible part of the image from the camera. Valid range is 1-16777215.	Not shown for linescan cameras.

Display Name	Parameter	Description	Notes
Camera Sensor Geometry Setting	<u>CORACO_PRM_CHANNEL</u>	Defines the number of channels output by the camera.	
CXP Configuration	<u>CORACO_PRM_CXP_CONFIGURATION</u>	Sets the board's CXP configuration. Possible value is: CORACO_VAL_CXP_CONFIGURATION_DUAL_CHANNEL_ONE_STREAM	
Bit Transfer Rate	<u>CORACO_PRM_BIT_TRANSFER_RATE</u>	Sets the transfer rate between the camera and the frame grabber.	
PoCXP	<u>CORACO_PRM_POCXP_ENABLE</u>	Enables 24V output on the lanes if PoCXP is supported by the camera's connected lane.	
PoCXP Status	<u>CORACO_PRM_SIGNAL_STATUS</u>	Shows the current status of the PoCXP. If at least one lane is powering camera with PoCXP, it will indicate 'Active'.	This is a read-only status.

# Advanced Control Category

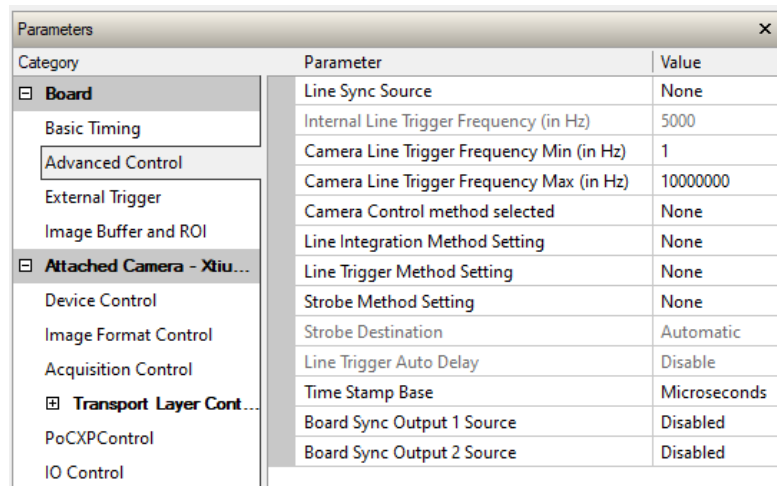
The Advanced Control category groups parameters for configuring camera control signals, board sync outputs and other advanced settings.

## Area Scan Parameters



Category	Parameter	Value
<b>Board</b>	Internal Frame Trigger	Disabled
Basic Timing	Internal Frame Trigger Frequency (in Hz)	30
<b>Advanced Control</b>	Camera Control method selected	None
External Trigger	Time Integration Method Setting	None
Image Buffer and ROI	Camera Trigger Method Setting	None
<b>Attached Camera - Xtiu...</b>	Camera Frames Per Trigger	1
Device Control	Camera Control During Readout	Invalid
Image Format Control	Strobe Method Setting	None
Acquisition Control	Strobe Destination	Automatic
<b>Transport Layer Cont...</b>	Time Stamp Base	Microseconds
PoCXPControl	Board Sync Output 1 Source	Disabled
	Board Sync Output 2 Source	Disabled

## Line Scan Parameters



Category	Parameter	Value
<b>Board</b>	Line Sync Source	None
Basic Timing	Internal Line Trigger Frequency (in Hz)	5000
<b>Advanced Control</b>	Camera Line Trigger Frequency Min (in Hz)	1
External Trigger	Camera Line Trigger Frequency Max (in Hz)	10000000
Image Buffer and ROI	Camera Control method selected	None
<b>Attached Camera - Xtiu...</b>	Line Integration Method Setting	None
Device Control	Line Trigger Method Setting	None
Image Format Control	Strobe Method Setting	None
Acquisition Control	Strobe Destination	Automatic
<b>Transport Layer Cont...</b>	Line Trigger Auto Delay	Disable
PoCXPControl	Time Stamp Base	Microseconds
IO Control	Board Sync Output 1 Source	Disabled
	Board Sync Output 2 Source	Disabled



# Parameter Descriptions

The following table describes the CamExpert Advanced Control category of Sopera LT parameters. Acquisition server notes, if applicable, indicate if parameter availability or supported values are dependent on the selected frame grabber acquisition server and acquisition device.

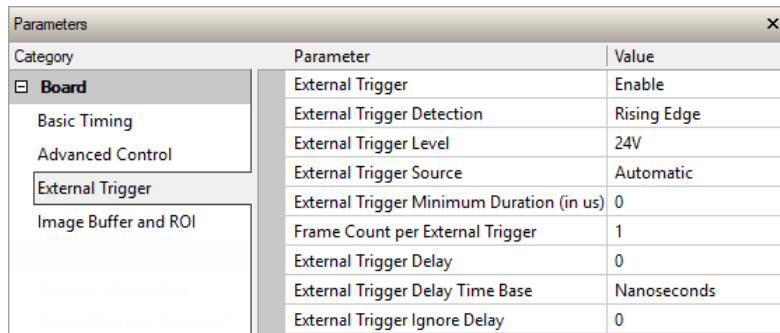
Display Name	Parameter	Description	Notes
Internal Frame Trigger	<a href="#"><u>CORACO_PRM_INT_FRAME_TRIGGER_ENABLE</u></a>	Enables/disables the acquisition device's internal frame trigger. Boolean parameter (TRUE or FALSE).	Applies to area scan cameras only.
Internal Frame Trigger Frequency (in Hz)	<a href="#"><u>CORACO_PRM_INT_FRAME_TRIGGER_FREQ</u></a>	Internal frame trigger frequency in Hz. Set to the required frame rate when using internal frame trigger to control camera acquisition. Valid range is 0.001-41000Hz.	
Line Sync Source	<a href="#"><u>CORACO_PRM_EXT_LINE_TRIGGER_ENABLE</u></a> <a href="#"><u>CORACO_PRM_INT_LINE_TRIGGER_ENABLE</u></a> <a href="#"><u>CORACO_PRM_SHAFT_ENCODER_ENABLE</u></a>	Selects the line trigger source for linescan cameras, unless free-running.	Applies to line scan cameras only.
Internal Line Trigger Frequency (in Hz)	<a href="#"><u>CORACO_PRM_INT_LINE_TRIGGER_FREQ</u></a>	Sets the internal line trigger frequency, in Hz. Applies only when the Line Sync Source is set to Internal Line Trigger.	Applies to line scan cameras only.
Camera Line Trigger Frequency Min (in Hz)	<a href="#"><u>CORACO_PRM_CAM_LINE_TRIGGER_FREQ_MIN</u></a>	Sets the camera's minimum line trigger frequency. Minimum value is 1Hz.	Applies to line scan cameras only.
Camera Line Trigger Frequency Max (in Hz)	<a href="#"><u>CORACO_PRM_CAM_LINE_TRIGGER_FREQ_MAX</u></a>	Sets the camera's maximum line trigger frequency. Maximum value is 10000000 Hz.	Applies to line scan cameras only.
Camera Control method selected	<a href="#"><u>CORACO_PRM_TIME_INTEGRATE_ENABLE</u></a> <a href="#"><u>CORACO_PRM_CAM_TRIGGER_ENABLE</u></a> <a href="#"><u>CORACO_PRM_LINE_TRIGGER_ENABLE</u></a>	Enables or disables an available camera control method. Each supported control method has one or more operating modes to choose from; refer to the parameters: Camera Trigger Method Setting Time Integration Method Setting.	
Time Integration Method Setting	<a href="#"><u>CORACO_PRM_TIME_INTEGRATE_METHOD</u></a> <a href="#"><u>CORACO_PRM_TIME_INTEGRATE_DELAY</u></a>	When the Camera Control method is Time Integration, select and configure the control method required.  Click on the parameter field to open the configuration dialog.	
Camera Trigger Method Setting	<a href="#"><u>CORACO_PRM_CAM_TRIGGER_METHOD</u></a>	When an asynchronous trigger pulse to a camera is required, select and configure the required method.	
Line Integration Method Setting	<a href="#"><u>CORACO_PRM_LINE_INTEGRATE_METHOD</u></a>	Sets the method for controlling the camera's line integration.	Applies to line scan cameras only
Line Trigger Method Setting	<a href="#"><u>CORACO_PRM_LINE_TRIGGER_METHOD</u></a>	Sets the method for line trigger pulse output.	Applies to line scan cameras only
Camera Frames Per Trigger	<a href="#"><u>CORACO_PRM_CAM_FRAMES_PER_TRIGGER</u></a>	Specifies the number of frames output by the camera per trigger; currently not available.	Applies to area scan cameras only.
Camera Control During Readout	<a href="#"><u>CORACO_PRM_CAM_CONTROL_DURING_READOUT</u></a>	Specifies if the camera control signals can be sent during the readout of a frame. Possible values are: <ul style="list-style-type: none"> <li>Valid</li> <li>Invalid</li> <li>Ignore</li> </ul>	
Strobe Method Setting	<a href="#"><u>CORACO_PRM_STROBE_METHOD</u></a> <a href="#"><u>CORACO_PRM_STROBE_ENABLE</u></a> <a href="#"><u>CORACO_PRM_STROBE_DELAY</u></a> <a href="#"><u>CORACO_PRM_STROBE_DURATION</u></a> <a href="#"><u>CORACO_PRM_STROBE_LEVEL</u></a> <a href="#"><u>CORACO_PRM_STROBE_POLARITY</u></a>	When a strobe output signal from the acquisition board is required, select and configure the control method required.  Note, method 1 is only available for areascan camera type; method 3 for line scan only.	
Strobe Destination	<a href="#"><u>CORACO_PRM_STROBE_DESTINATION</u></a>	Specifies which physical output to use for the strobe signal.	
Line Trigger Auto Delay	<a href="#"><u>CORACO_PRM_LINE_TRIGGER_AUTO_DELAY</u></a>	Enables delaying line triggers to a camera based on the selected method. Used to avoid over-triggering a camera.	Applies to line scan cameras only

Display Name	Parameter	Description	Notes
Time Stamp Base	<u>CORACO_PRM_TIME_STAMP_BASE</u>	<p>Sets the counter stamp time base. Possible values are:</p> <ul style="list-style-type: none"> <li>• Microseconds</li> <li>• Line Counts</li> <li>• External line trigger or shaft encoder</li> <li>• Shaft Encoder</li> <li>• 100 Nanoseconds</li> </ul>	
Board Sync Output 1 Source	<u>CORACO_PRM_BOARD_SYNC_OUTPUT1_SOURCE</u>	<p>Specifies the signal to output on board sync output 1. This parameter permits the synchronization of two acquisition devices using a signal from one acquisition device and synching the second acquisition device with it.</p>	
Board Sync Output 2 Source	<u>CORACO_PRM_BOARD_SYNC_OUTPUT2_SOURCE</u>	<p>Specifies the signal to output on board sync output 2. This parameter permits the synchronization of two acquisition devices using a signal from one acquisition device and synching the second acquisition device with it.</p>	

# External Trigger Category

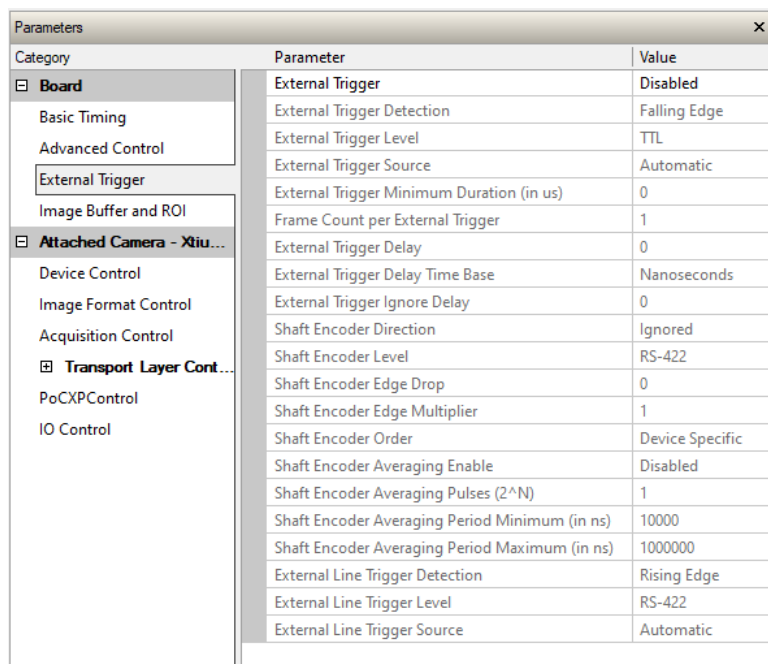
The External category groups parameters for configuring an external trigger for controlling image acquisition.

## Area Scan Parameters



Category	Parameter	Value
<input checked="" type="checkbox"/> Board	External Trigger	Enable
Basic Timing	External Trigger Detection	Rising Edge
Advanced Control	External Trigger Level	24V
External Trigger	External Trigger Source	Automatic
Image Buffer and ROI	External Trigger Minimum Duration (in us)	0
	Frame Count per External Trigger	1
	External Trigger Delay	0
	External Trigger Delay Time Base	Nanoseconds
	External Trigger Ignore Delay	0

## Line Scan Parameters



Category	Parameter	Value
<input checked="" type="checkbox"/> Board	External Trigger	Disabled
Basic Timing	External Trigger Detection	Falling Edge
Advanced Control	External Trigger Level	TTL
External Trigger	External Trigger Source	Automatic
Image Buffer and ROI	External Trigger Minimum Duration (in us)	0
	Frame Count per External Trigger	1
	External Trigger Delay	0
	External Trigger Delay Time Base	Nanoseconds
	External Trigger Ignore Delay	0
<input checked="" type="checkbox"/> Attached Camera - Xtiu...	Shaft Encoder Direction	Ignored
Device Control	Shaft Encoder Level	RS-422
Image Format Control	Shaft Encoder Edge Drop	0
Acquisition Control	Shaft Encoder Edge Multiplier	1
<input checked="" type="checkbox"/> Transport Layer Cont...	Shaft Encoder Order	Device Specific
PoCXPControl	Shaft Encoder Averaging Enable	Disabled
IO Control	Shaft Encoder Averaging Pulses (2^N)	1
	Shaft Encoder Averaging Period Minimum (in ns)	10000
	Shaft Encoder Averaging Period Maximum (in ns)	1000000
	External Line Trigger Detection	Rising Edge
	External Line Trigger Level	RS-422
	External Line Trigger Source	Automatic

# Parameter Descriptions

The following table describes the CamExpert External Trigger category of Sopera LT parameters.

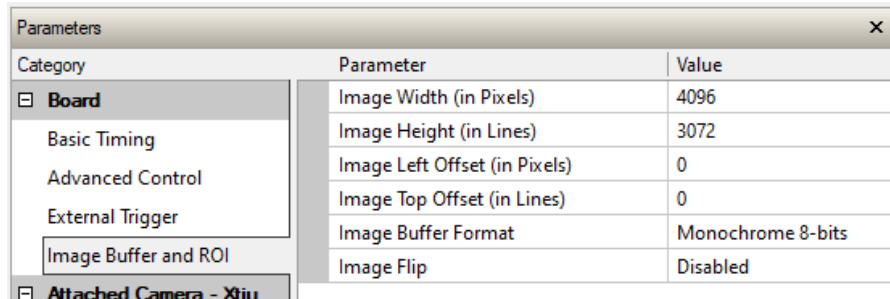
Display Name	Parameter	Description								
External Trigger	<a href="#">CORACO_PRM_EXT_TRIGGER_ENABLE (area scan)</a> <a href="#">CORACO_PRM_EXT_FRAME_TRIGGER_ENABLE (line scan)</a>	Enables/disables external trigger on the acquisition board. When enabled, the acquisition board acquires an image frame from the camera after receiving the trigger. Boolean parameter (TRUE or FALSE).								
External Trigger Detection	<a href="#">CORACO_PRM_EXT_TRIGGER_DETECTION (area scan)</a> <a href="#">CORACO_PRM_EXT_FRAME_TRIGGER_DETECTION (line scan)</a>	Defines the signal detected that generates an external trigger event to the acquisition device.  Two types of trigger are available: <i>Level Trigger: Active Low / High</i>  Logic level (Low/High) on the trigger input enables continuous image capture until the trigger input is set to opposite logic .  <i>Edge Trigger: Rising / Falling edge</i>  Edge transition of a trigger pulse captures one image frame.  Line scan cameras also support: <i>Dual-Input Trigger Rising Edge / Dual-Input Trigger Falling Edge</i>								
External Trigger Level	<a href="#">CORACO_PRM_EXT_TRIGGER_LEVEL (area scan)</a> <a href="#">CORACO_PRM_EXT_FRAME_TRIGGER_LEVEL (line scan)</a>	Specifies the electrical level of the external trigger connected to the acquisition board.  Possible values: <table border="1" data-bbox="893 898 1458 1035"> <tr> <td>TTL</td> <td>single-ended logic signal</td> </tr> <tr> <td>RS-422</td> <td>balanced logic signal</td> </tr> <tr> <td>12V</td> <td>single-ended logic signal</td> </tr> <tr> <td>24V</td> <td>single-ended logic signal</td> </tr> </table>	TTL	single-ended logic signal	RS-422	balanced logic signal	12V	single-ended logic signal	24V	single-ended logic signal
TTL	single-ended logic signal									
RS-422	balanced logic signal									
12V	single-ended logic signal									
24V	single-ended logic signal									
External Trigger Source	<a href="#">CORACO_PRM_EXT_TRIGGER_SOURCE (area scan)</a> <a href="#">CORACO_PRM_EXT_FRAME_TRIGGER_SOURCE (line scan)</a>	Specifies the physical input source the external frame trigger is connected to or which trigger input is used on the acquisition device.  Note: to assign the external trigger source to a GPIO it must be reserved; By default, boards are shipped with User Interface General Inputs 1 & 2 reserved for External Triggers and User Interface General Outputs 1 & 2 reserved for Strobe Outputs.  Refer to <a href="#">Information Field Description</a> for more information on using the Teledyne DALSA Device Manager tool to reserve GPIOs.								
External Trigger Minimum Duration (in $\mu$ s)	<a href="#">CORACO_PRM_EXT_TRIGGER_DURATION</a>	Minimum external trigger pulse duration (in $\mu$ s), needed for the pulse to be acknowledged by the acquisition device. If the duration of the pulse is shorter, the pulse is ignored.  This feature is useful for trigger pulse debouncing. If the value is '0', no validation is performed								
Frame Count per External Trigger	<a href="#">CORACO_PRM_EXT_TRIGGER_FRAME_COUNT</a>	Number of images to acquire upon receiving an external trigger. Valid range is 1-262142.  Note, infinite frame count (-1) is not supported.								
External Trigger Delay	<a href="#">CORACO_PRM_EXT_TRIGGER_DELAY</a>	Sets the delay between the reception of the trigger signal and the start of the image acquisition. Units are specified by the External Trigger Delay Time Base parameter.								
External Trigger Delay Time Base	<a href="#">CORACO_PRM_EXT_TRIGGER_DELAY_TIME_BASE</a>	Sets the external trigger delay time base. Possible values: <ul style="list-style-type: none"> <li>• Line Counts</li> <li>• Nanoseconds</li> <li>• External Line Trigger or Shaft Encoder</li> <li>• Shaft Encoder</li> </ul>								

Display Name	Parameter	Description
External Trigger Ignore Delay	<u>CORACO_PRM_EXT_TRIGGER_IGNORE_DELAY</u>	Sets the time delay, in $\mu\text{sec}$ , where if another external trigger occurs, it is ignored. Valid range is 0-42949672. The start of the delay (time '0') is the end of the next vertical sync for analog cameras, or the beginning of the next frame valid for digital cameras, following a valid external trigger.
Shaft Encoder Direction	<u>CORACO_PRM_SHAFT_ENCODER_DIRECTION</u>	Selects the direction of the shaft encoder that increments/decrements the acquisition device encoder counter.  Support of dual phase encoders might require that the direction of motion be considered. This is the case where system vibrations and/or conveyor backlash can cause the encoder to momentarily travel backwards. The acquisition device must in those cases count the reverse steps and subtract the forward steps such that only pulses after the reverse count reaches zero are considered valid.
Shaft Encoder Level	<u>CORACO_PRM_SHAFT_ENCODER_LEVEL</u>	Specifies the level of the signal input to the shaft encoder.
Shaft Encoder Edge Drop	<u>CORACO_PRM_SHAFT_ENCODER_DROP</u>	Number of shaft encoder signal edges dropped between active shaft encoder triggers.  Use the pulse drop feature to reduce the acquisition rate without reducing the shaft encoder trigger rate.
Shaft Encoder Edge Multiplier	<u>CORACO_PRM_SHAFT_ENCODER_MULTIPLY</u>	Number of signal edges generated internally on the acquisition board for each external shaft encoder signal edge.  Use when video acquisitions are controlled by an external shaft encoder trigger but multiple acquisitions are needed from each trigger.
Shaft Encoder Order	<u>CORACO_PRM_SHAFT_ENCODER_ORDER</u>	Specifies the order of the drop/multiply operation of the shaft encoder.
Shaft Encoder Averaging Enable	<u>CORACO_PRM_SHAFT_ENCODER_AVERAGING_ENABLE</u>	Enables/Disables averaging of the shaft encoder signal edges received.
Shaft Encoder Averaging Pulses (2 <sup>N</sup> )	<u>CORACO_PRM_SHAFT_ENCODER_AVERAGING_PULSES</u>	Specifies the number of shaft encoder signal edges used to make an average.
Shaft Encoder Averaging Period Minimum (in ns)	<u>CORACO_PRM_SHAFT_ENCODER_AVERAGING_PERIOD_MIN</u>	Minimum time between 2 shaft encoder signal edges for the pulses to be averaged. If minimum time is not respected, the average engine will do a clean restart.
Shaft Encoder Averaging Period Maximum (in ns)	<u>CORACO_PRM_SHAFT_ENCODER_AVERAGING_PERIOD_MAX</u>	Maximum time between 2 shaft encoder signal edges for the pulses to be averaged. If the maximum time is not respected, the average engine will do a clean restart.
External Line Trigger Detection	<u>CORACO_PRM_EXT_LINE_TRIGGER_DETECTION</u>	Select the signal detected (rising edge/falling edge) that generates an external line trigger to the acquisition device.
External Line Trigger Level	<u>CORACO_PRM_EXT_LINE_TRIGGER_LEVEL</u>	Specifies the level of the signal input to the external line trigger input.
External Line Trigger Source	<u>CORACO_PRM_EXT_LINE_TRIGGER_SOURCE</u> <u>CORACO_PRM_EXT_LINE_TRIGGER_ENABLE</u>	Specifies the physical input source the external line trigger is connected to on the acquisition device, in the case where the acquisition device has more than one input.  Line scan cameras typically use the shaft encoder signals as the acquisition board line trigger.  The 'Automatic' choice selects the trigger normally used with the acquisition module, in the case of multiple modules – multiple trigger inputs.

# Image Buffer and ROI Category

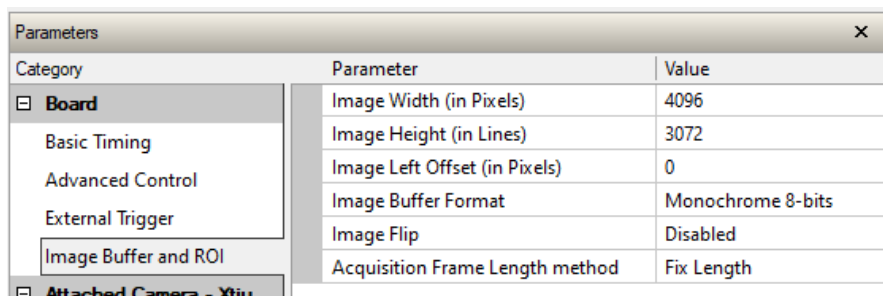
The Image Buffer and ROI category groups parameters for the configuring the image buffer format, size and offset settings, as well as image flipping.

## Area Scan Parameters



Category	Parameter	Value
<b>Board</b>	Image Width (in Pixels)	4096
Basic Timing	Image Height (in Lines)	3072
Advanced Control	Image Left Offset (in Pixels)	0
External Trigger	Image Top Offset (in Lines)	0
<b>Image Buffer and ROI</b>	Image Buffer Format	Monochrome 8-bits
Attached Camera - Xtiu...	Image Flip	Disabled

## Line Scan Parameters



Category	Parameter	Value
<b>Board</b>	Image Width (in Pixels)	4096
Basic Timing	Image Height (in Lines)	3072
Advanced Control	Image Left Offset (in Pixels)	0
External Trigger	Image Buffer Format	Monochrome 8-bits
<b>Image Buffer and ROI</b>	Image Flip	Disabled
Attached Camera - Xtiu...	Acquisition Frame Length method	Fix Length

## Parameter Descriptions

The following table describes the CamExpert Image Buffer and ROI category of Sapera LT parameters. Acquisition server notes, if applicable, indicate if parameter availability or supported values are dependent on the selected frame grabber acquisition server and acquisition device.

Display Name	Parameter	Description	Notes
Image Width (in Pixels)	<a href="#"><u>CORACO_PRM_CROP_WIDTH</u></a>	<p>Cropped width of the acquisition image, in pixels; this parameter defines the width of the image transferred to the frame buffer.</p> <p>The maximum width is the active horizontal of the image source (see the Horizontal Active parameter in the <a href="#"><u>Basic Timing</u></a> category).</p> <p>Cropping increments depend on the selected acquisition server; CamExpert automatically adjusts numerical entries to valid increments.</p>	Note: image data is not scaled.
Image Height (in Lines)	<a href="#"><u>CORACO_PRM_CROP_HEIGHT</u></a>	<p>Cropped height of the acquisition image, in lines; this parameter defines the vertical dimension of the image transferred to the frame buffer.</p> <p>The maximum height is the active vertical width of the image source (see the Vertical Active parameter in the <a href="#"><u>Basic Timing</u></a> category).</p> <p>Cropping increments depend on the selected acquisition server; CamExpert automatically adjusts numerical entries to valid increments.</p>	Note: image data is not scaled.
Image Left Offset (in Pixels)	<a href="#"><u>CORACO_PRM_CROP_LEFT</u></a>	<p>Number of pixels to crop from the left side of the acquisition image before transfer to the frame buffer.</p> <p>The maximum left offset is the active horizontal width of the image source less one increment step.</p> <p>Cropping increments depend on the selected acquisition server; CamExpert automatically adjusts numerical entries to valid increments.</p>	Note: image data is not scaled.
Image Top Offset (in Lines)	<a href="#"><u>CORACO_PRM_CROP_TOP</u></a>	<p>Number of lines to crop from the top of the acquisition image before transfer to the frame buffer.</p> <p>The maximum top offset is the active vertical height of the image source less one increment step.</p> <p>Cropping increments are acquisition hardware dependent; CamExpert automatically adjusts numerical entries to valid increments.</p>	Note: image data is not scaled.
Image Buffer Format	<a href="#"><u>CORACO_PRM_OUTPUT_FORMAT</u></a>	Data format for the acquisition image transfer to the frame buffer.	The data buffer format is dependent on the selected acquisition server; for details refer to the <a href="#"><u>CORACO_PRM_OUTPUT_FORMAT</u></a> parameter description
Image Flip	<a href="#"><u>CORACO_PRM_FLIP</u></a>	<p>Enables real-time on-board horizontal image flip function.</p> <p>The Xtium2-CXP PX8 also supports a vertical flip operation using <a href="#"><u>CORXFER_PRM_FLIP</u></a>.</p>	
Acquisition Frame Length method	<a href="#"><u>CORACO_PRM_FRAME_LENGTH</u></a>	Specifies if the image acquired will have a fixed or variable length in height.	Valid on in line scan.

---

# Using the Flat Field Correction Tool

Flat Field Correction is the process of eliminating small gain differences between pixels in a sensor array. That sensor when exposed to a uniformly lit field will have no gray level differences between pixels when calibrated flat field correction is applied to the image. The CamExpert Flat Field tool functions with hardware supporting flat field processing.

## Xtium2-CXP PX8 Flat Field Support

The Xtium2-CXP PX8 supports hardware based real-time Flat Field Correction when used with a monochrome video source. The Xtium2-CXP PX8 supports one method for pixel replacement:

- Neighborhood Replacement: a bad pixel is replaced with the average of its 2 neighbors on the same video line.
- Note that the CXP Flat Field algorithm handles all cases of bad pixels, either on the video frame edge or the neighboring pixels.

### *Loading the Required Camera File*

Select the required camera configuration file for the connected camera. Verify the acquisition with the live grab function. Make camera adjustments to get good images.

## Set up Dark and Bright Acquisitions with the Histogram Tool

Before performing calibration, verify the acquisition with a live grab. Also at this time, make preparations to grab a flat light gray level image, required for the calibration, such as a clean evenly lighted white wall or non-glossy paper with the lens slightly out of focus. Ideally, a controlled diffused light source aimed directly at the lens should be used. Note the lens iris position for a bright but not saturated image. Additionally, check that the lens iris closes well or have a lens cover to grab the dark calibration image.

### *Verify a Dark Acquisition*

Close the camera lens iris and cover the lens with a lens cap. Using CamExpert, click on the grab button and then the histogram button. The following figure shows a typical histogram for a very dark image (8-bit acquisition).



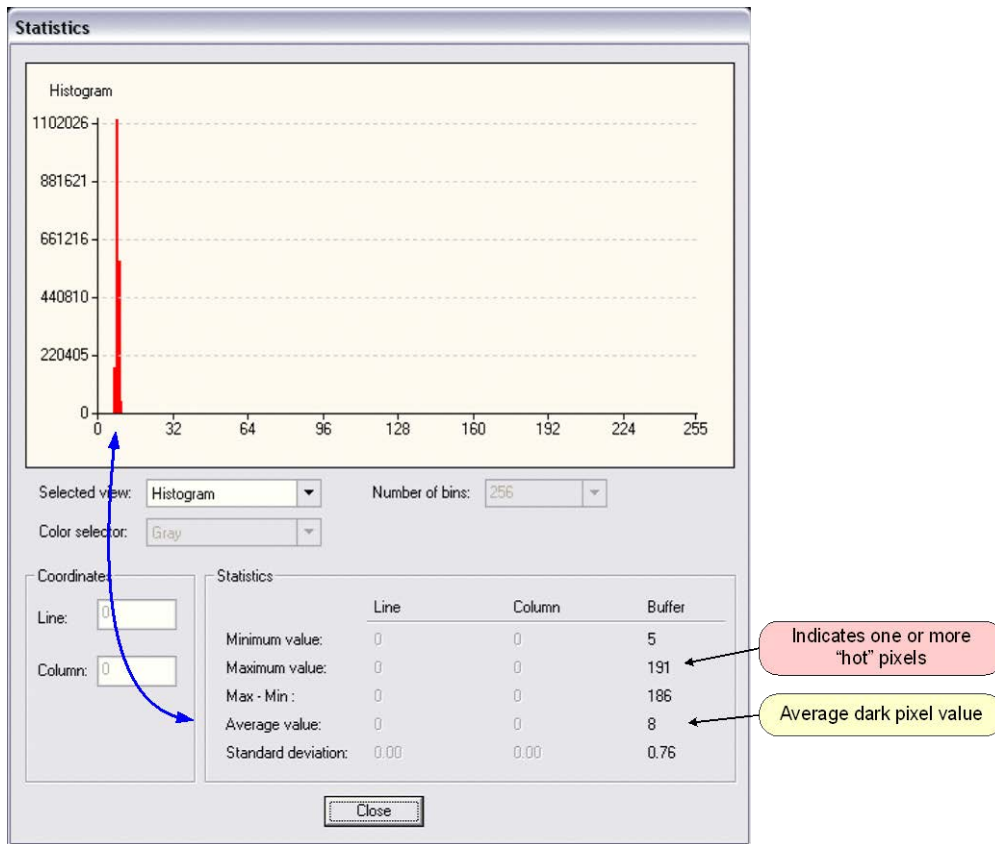


Figure 11: CamExpert Histogram of Dark Image

---

**Important:** In this example, the **average** pixel value for the frame is close to black. Also note that most sensors will show a much higher maximum pixel value due to one or more "hot pixels". The sensor specification accounts for a small number of hot or stuck pixels (pixels that do not react to light over the full dynamic range specified for that sensor).

---

### Verify a Bright Acquisition

Aim the camera at a diffused light source or evenly lit white wall with no shadows falling on it. Using CamExpert, click on the grab button and then the histogram button. Use the lens iris to adjust for a bright gray approximately around a pixel value of 200 (for 8-bit pixels). The following figure shows a typical histogram for a bright gray image.

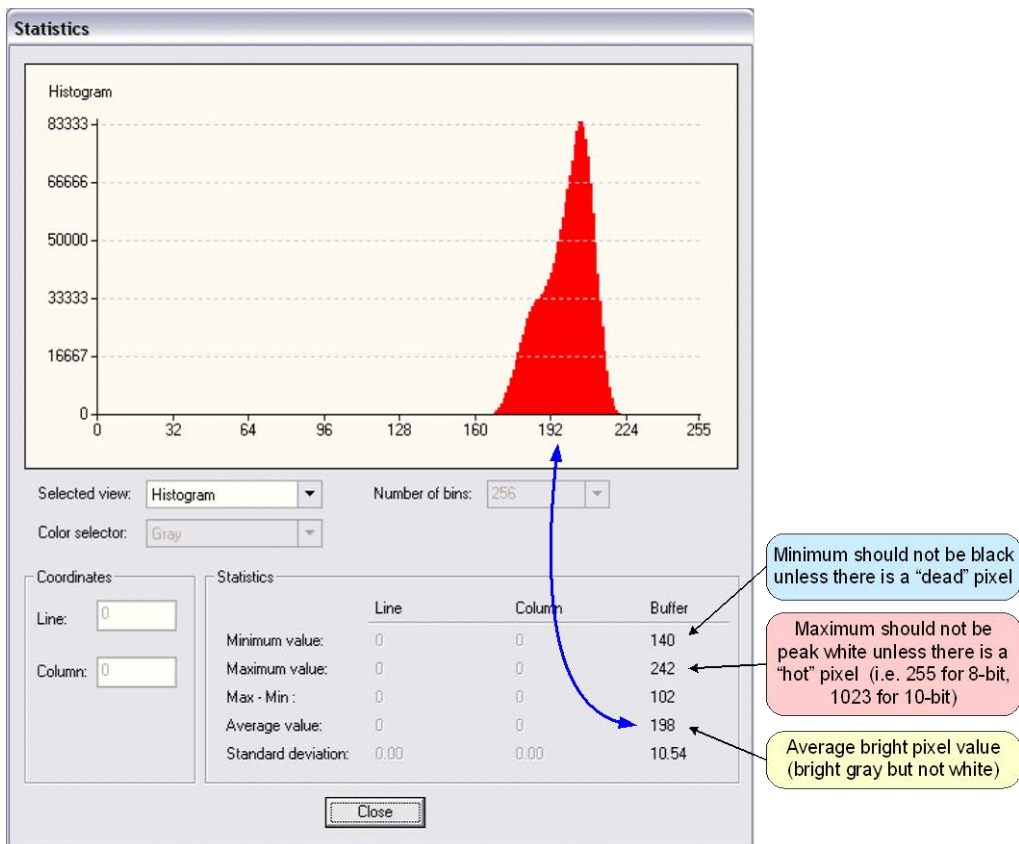


Figure 12: CamExpert Histogram of Bright Image

**Important:** In this example, the **average** pixel value for the frame is bright gray. Also note that sensors may show a much higher maximum or a much lower minimum pixel value due to one or more "hot or dead pixels". The sensor specification accounts for a small number of hot, stuck, or dead pixels (pixels that do not react to light over the full dynamic range specified for that sensor).

Once the bright gray acquisition setup is done, note the camera position and lens iris position so as to be able to repeat it during the calibration procedure.

## Flat Field Correction Calibration Procedure

Calibration is the process of taking two reference images, one of a black field – one of a light gray field (not saturated), to generate correction data for images captured by the CCD. Each CCD pixel data is modified by the correction factor generated by the calibration process, so that each pixel now has an identical response to the same illumination.

Start the Flat Field calibration tool via the CamExpert menu bar: **Pre-Processing > Flat Field Correction > Calibration**.

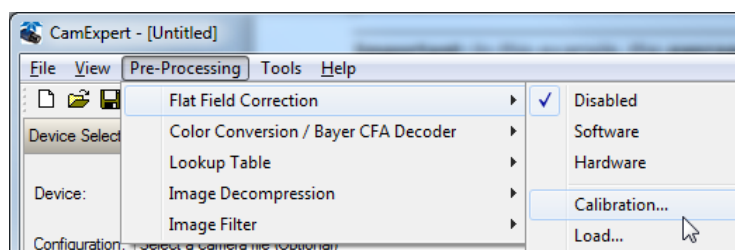


Figure 13: CamExpert Flat Field Correction Menu Command

## Flat Field Correction Dialog

The Flat Field Correction dialog provides a three-step process to acquire two reference images and then save the flat field correction data for the camera used. To aid in determining if the reference images are valid, a histogram tool is provided so that the user can review the images used for the correction data.

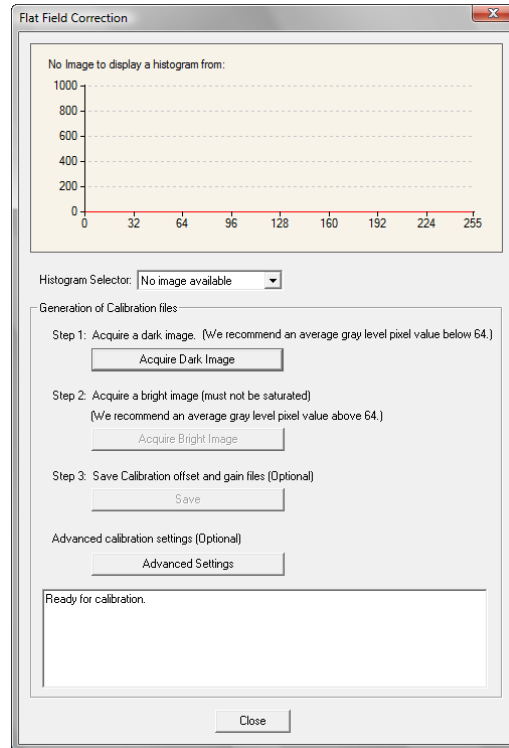


Figure 14: CamExpert Flat Field Correction Dialog

- Setup the camera to capture a uniform black image. Black paper with no illumination and the camera lens' iris closed to minimum can provide such a black image.
- Click on **Acquire Dark Image**. The flat field demo will grab a video frame, analyze the pixel gray level spread, and present the statistics. The desired black reference image should have pixel values less than 20. If acceptable, accept the image as the black reference.
- Setup the camera to acquire a uniform white image (but not saturated white). Even illumination on white paper can be used, with a minimum gray level of 128. It is preferable to prepare for the white level calibration before the calibration procedure.
- Click on **Acquire Bright Image**. The flat field demo will grab a video frame, analyze the pixel gray level spread, and present the statistics. The captured gray level for all pixels should be greater than 128. If acceptable, accept the image as the white reference.
- Click on **Save**. The flat field correction data is saved as a TIF image with a file name of your choice (such as camera name and serial number).

## Using Flat Field Correction

On the CamExpert menu bar, enable Flat Field correction (**Pre-Processing > Flat Field Correction > Hardware** or **Software**). Now when doing a live grab or snap, the incoming image is corrected by the current flat field calibration data for each pixel.

Use the command **Pre-Processing > Flat Field Correction > Load** to load in a flat field correction image from previous saved calibration data. CamExpert allows saving and loading calibration data for all cameras used with the imaging system.

---

# Using the Bayer Filter Tool

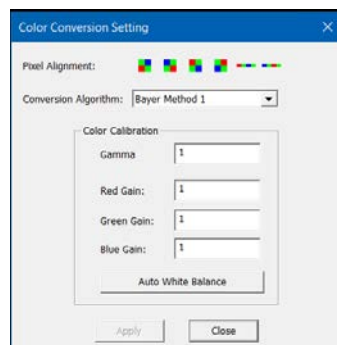
CamExpert supports the use of Bayer Filter cameras by providing a tool to select the Bayer filter mosaic pattern and to perform an auto white balance. Color calibration can then be manually fine-tuned with RGB gain and gamma adjustments.

The CamExpert Bayer filter tool supports using either software or hardware based decoding. With boards that have Bayer filter decoding in hardware, CamExpert directly controls the hardware for high performance real-time acquisitions from Bayer filter cameras. When standard acquisition boards are used, CamExpert performs software Bayer filter decoding using the host system processor.

## Bayer Filter White Balance Calibration Procedure

The following procedure uses the hardware Bayer filter support (Bayer Decoder firmware loaded) and any supported Bayer color camera. It is assumed that CamExpert was used to generate a camera file with correct camera timing parameters.

- On the CamExpert menu bar, select **Pre-Processing > Color Conversion/Bayer CFA Decoder > Setting**. If the frame grabber has Bayer support, the menu should show **Hardware** selected by default.



- Click **Grab** to start acquisition.
- Aim and focus the camera. The camera should see an area of white or place white paper in front of the object being imaged.
- Click on one of the four Bayer pixel alignment patterns to match the camera (best color before calibration). Typically, the CamExpert default is correct for a majority of cameras.
- Adjust the lens iris to reduce the exposure brightness so that the white image area is now darker. Make certain that no pixel in the white area is saturated.
- Use the mouse left button to click and drag a ROI enclosing a portion of the white area.
- Click **Auto White Balance**. CamExpert will make RGB gain adjustments.
- Open the camera iris to have a correctly exposed image.
- Review the image for color balance.
- Manually make additional adjustments to the RGB gain values. Fine-tune the color balance to achieve best results. Adjust the gamma factor to optionally improve the display.
- Stop the live acquisition and save the camera file (which now contains the Bayer RGB calibration information). Note that the gamma factor is not saved because it is not a Sapera parameter but only a display tool.

### **Using the Bayer Filter**

A Sapera application, when loading the camera file parameters, will have the RGB gain adjustment values. The application can incorporate a calibration menu for RGB adjustments as required.

# Sapera Demo Applications

The Sapera Explorer application is the fastest way to access the demo programs, code samples, examples and other info provided with Sapera LT.

## To open Sapera Explorer

- On the **Start** menu, select **Teledyne DALSA Sapera LT > Sapera Explorer**.

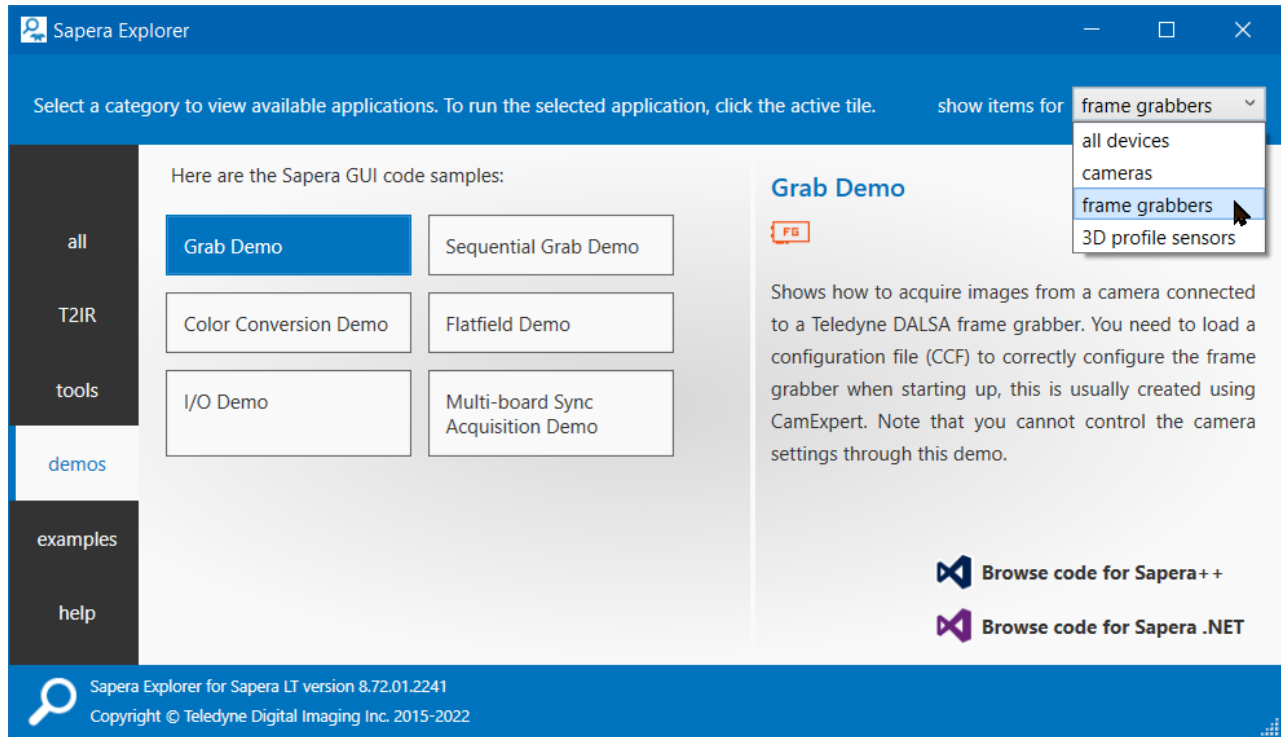


Figure 15: The Sapera Explorer application

All demo programs are available as a compiled binary; source code is provided for both C++ and .NET projects using Visual Studio 2013/2015/2017/2019.

Table 4: Demos Workspace Details

<b>Program file</b>	...\\...\\Sapera\\Demos\\Binaries\\GrabDemo.exe
<b>Visual C++ Solution</b>	...\\...\\Sapera\\Demos\\Classes\\Vc\\SapDemos_2013.sln ...\\...\\Sapera\\Demos\\Classes\\Vc\\SapDemos_2015.sln ...\\...\\Sapera\\Demos\\Classes\\Vc\\SapDemos_2017.sln ...\\...\\Sapera\\Demos\\Classes\\Vc\\SapDemos_2019.sln
<b>Visual .NET Solution</b>	...\\...\\Sapera\\Demos\\NET\\SapNETCSDemos_2013.sln ...\\...\\Sapera\\Demos\\NET\\SapNETCSDemos_2015.sln ...\\...\\Sapera\\Demos\\NET\\SapNETCSDemos_2017.sln ...\\...\\Sapera\\Demos\\NET\\SapNETCSDemos_2019.sln ...\\...\\Sapera\\Demos\\NET\\SapNETCSDemos_2019.Core.sln
<b>Remarks</b>	This demo is based on Sapera LT classes. See the Sapera User's and Reference manuals for more information.

---

# Grab Demo Overview

The Grab Demo program demonstrates the basic acquisition functions included in the Sopera library (Sopera LT 8.7). The program either allows you to acquire images, in continuous (grab) or in one-time (snap) mode, while adjusting the acquisition parameters. The program code may be extracted for use within your own application.

## Using the Grab Demo

### To open the Grab Demo program

- In **Sopera Explorer**, on the left pane select **Demos**, then double-click **Grab Demo** (see Figure 15).

Alternately, from the **Start** menu, select **Teledyne DALSA Sopera LT > Sopera++ Demos (Executables)**, which will open the folder where **GrabDemo.exe** is located.

### Acquisition Configuration Window

When using frame grabbers, the demo program first displays the Acquisition Configuration window, where you can select from the available Sopera acquisition servers and input devices present on the selected server.

- From the **Acquisition Server** list, select and installed Sopera acquisition server (installed Teledyne DALSA acquisition hardware using Sopera drivers).
- From the **Acquisition Device** list, select an available input device on the selected driver.
- Click **Browse** to select the required camera configuration file for the connected camera. Sopera camera files contain timing parameters and video conditioning parameters. The default folder for camera configuration files is the same used by the CamExpert utility to save user generated or modified camera files.

Use CamExpert program to generate the camera configuration file based on timing and control parameters entered. The CamExpert live acquisition window allows immediate verification of those parameters. CamExpert reads both Sopera \*.cca and \*.cvi for backward compatibility with the original Sopera camera files.

### Grab Demo Main Window

The Grab Demo program provides basic acquisition controls for the selected frame grabber. The loaded camera file (.ccf) defines the frame buffer defaults.

Refer to the Sopera LT Getting Started Manual for Frame Grabbers (OC-SAPM-INTRO), chapter **Demos and Examples**, for more information on the Grab Demo and other programs provided with Sopera LT.

# Xtium2-CXP PX8 Reference

## Block Diagram

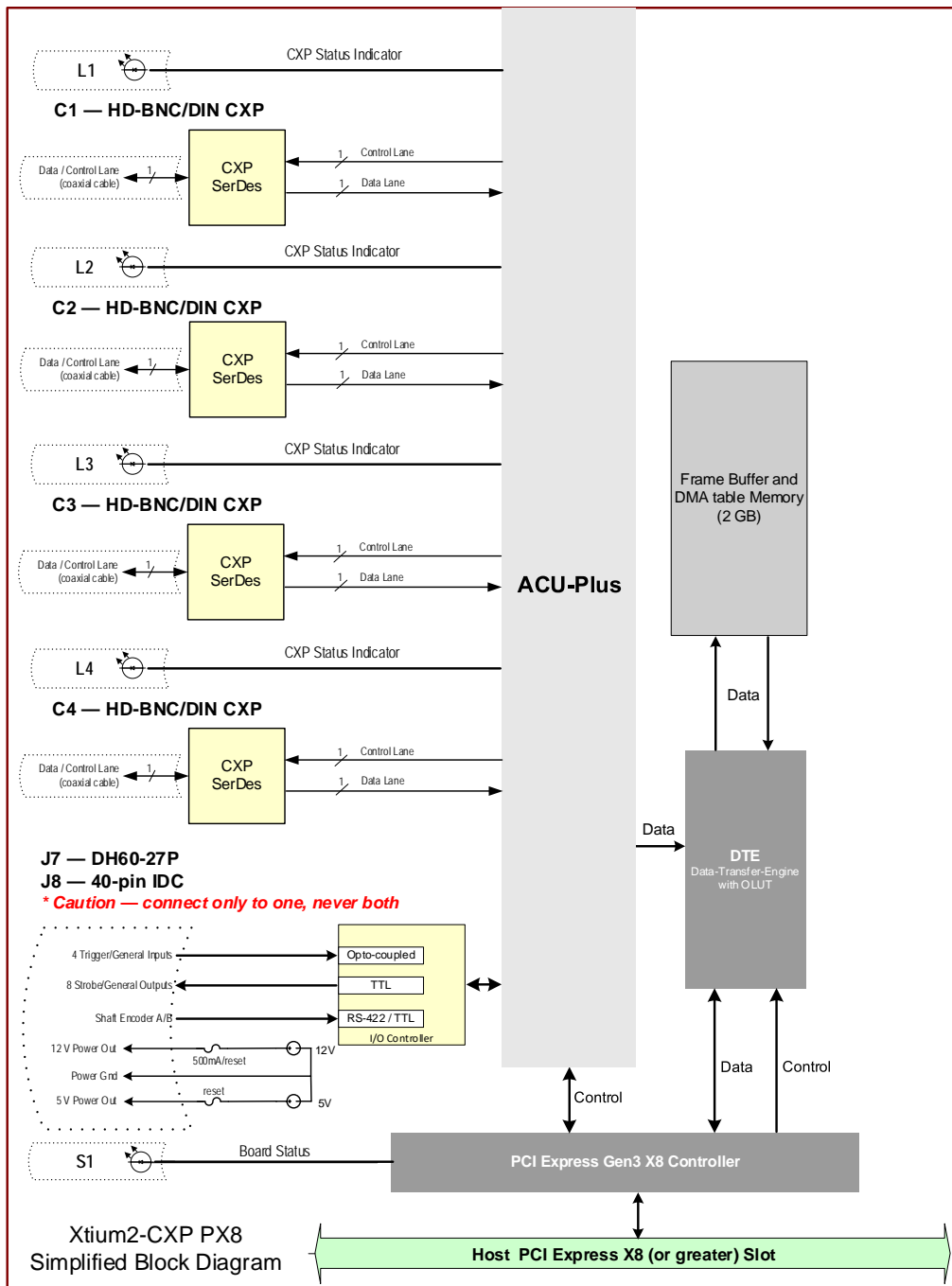


Figure 16: Xtium2-CXP PX8 Block Diagram

# Xtium2-CXP Flow Diagram

The following diagram represents the sequence in which the camera data acquired is processed through the Xtium2-CXP.

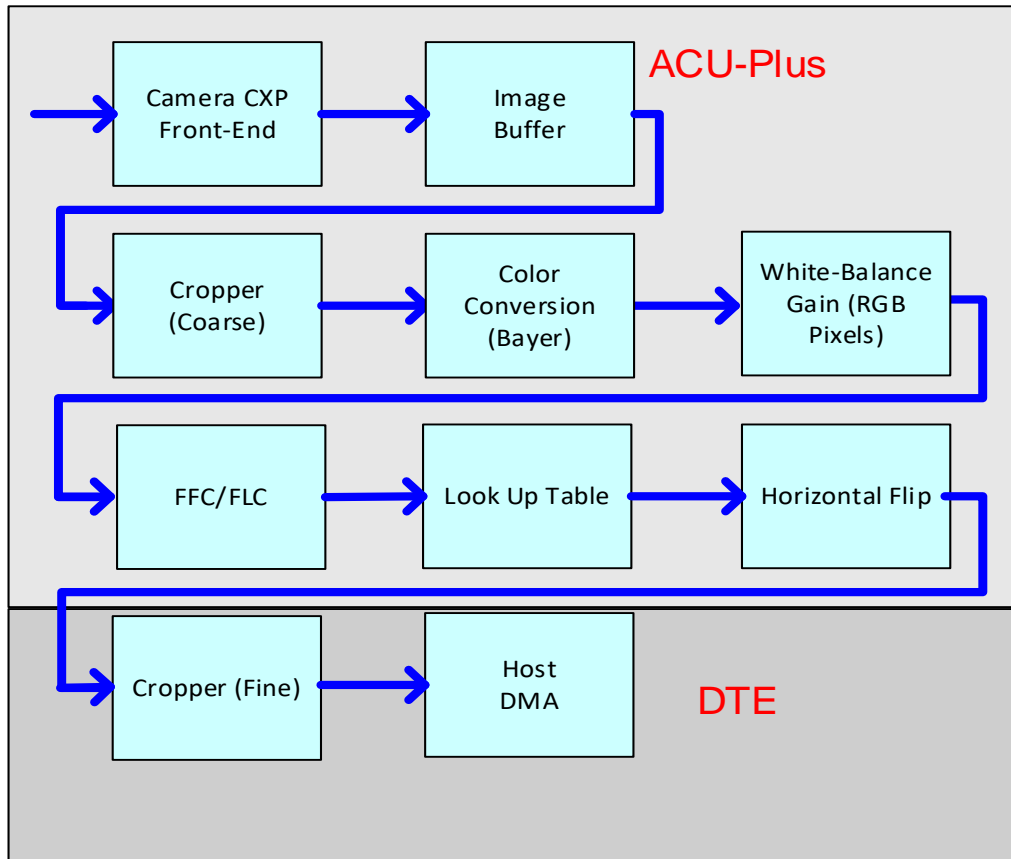


Figure 17: Xtium2-CXP Flow Diagram

- **Camera CXP Front End:** Extracts the video data packets from the Camera CXP port(s).
- **Image Buffer:** Stores the video data using the model of video frames.
- **Cropper (Coarse):** Horizontal cropper used when reading out from the memory.
- **Color Conversion:** When enabled for particular cameras, converts Bayer video data into RGB data.
- **White Balance Gain:** Applies White Balance Gain to RGB data.
- **FFC/FLC:** Flat Field/Flat Line correction. Applies to Monochrome data only.
- **Lookup Tables:** Apply lookup table transformation to the image.
- **Horizontal Flip:** Performs the line data flip process.
- **Cropper (Fine):** Crops the resulting image when used, using an 8-byte resolution.
- **Host DMA:** Transfers the data from frame grabber into the host buffer memory. This module will also perform the vertical flip if enabled.



# Line Trigger Source Selection for Line scan Applications

Line scan imaging applications require some form of external event trigger to synchronize line scan camera exposures to the moving object. This synchronization signal is either an external trigger source (one exposure per trigger event) or a shaft encoder source composed of a single or dual phase (also known as a quadrature) signal.

The Xtium2-CXP PX8 shaft encoder inputs provide additional functionality with pulse drop, pulse multiply, and pulse direction support.

The following table describes the line-trigger source types supported by the Xtium2-CXP PX8. Refer to the Sopera Acquisition Parameters Reference Manual (OC-SAPM-APR00) for descriptions of the Sopera parameters.

## CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_SOURCE – Parameter Values Specific to the Xtium2-CXP PX8

Table 5: CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_SOURCE – Parameter Values

PRM Value	Input used as: External Line Trigger	Input used as: External Shaft Encoder
	<i>if</i> CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE = <i>true</i>	<i>if</i> CORACQ_PRM_SHAFT_ENCODER_ENABLE = <i>true</i>
<b>0</b>	From Shaft Encoder Phase A	From Shaft Encoder Phase A & B
<b>1</b>	From Shaft Encoder Phase A	From Shaft Encoder Phase A
<b>2</b>	From Shaft Encoder Phase B	From Shaft Encoder Phase B
<b>3</b>	n/a	From Shaft Encoder Phase A & B
<b>4</b>	From Board Sync #1	n/a
<b>5</b>	From Board Sync #2	n/a

### CVI/CCF File Parameters Used

- External Line Trigger Source = parameter value
- External Line Trigger Enable = true/false
- Shaft Encoder Enable = true/false

# Shaft Encoder Interface Timing

## Dual Balanced Shaft Encoder RS-422 Inputs:

- Input Phase A:
  - Connector J7: Pin 3 (Phase A +) & Pin 2 (Phase A -)
  - Connector J8: Pin 5 (Phase A +) & Pin 6 (Phase A -)
- Input Phase B:
  - Connector J7: Pin 6 (Phase B+) & Pin 5 (Phase B-)
  - Connector J8: Pin 7 (Phase B +) & Pin 8 (Phase B -)
- See [J7: External I/O Signals Connector \(Female DH60-27P\)](#) for complete connector signal details) and [J8: Internal I/O Signals Connector \(40-pin TST-120-01-G-D\)](#).

Web inspection systems with variable web speeds typically provide one or two synchronization signals from a web mounted encoder to coordinate trigger signals. These trigger signals are used by the acquisition linescan camera. The Xtium2-CXP PX8 supports single or dual phase shaft encoder signals. Dual encoder signals are typically 90 degrees out of phase relative to each other and provide greater web motion resolution.

## Example using any Encoder Input with Pulse-drop Counter

When enabled, the triggered camera acquires one scan line for each shaft encoder pulse-edge. To optimize the web application, a second Sopera parameter defines the number of triggers to skip between valid acquisition triggers. The figure below depicts a system where a valid camera trigger is any pulse edge from either shaft encoder signal. After a trigger, the two following triggers are ignored (as defined by the Sopera pulse drop parameter).

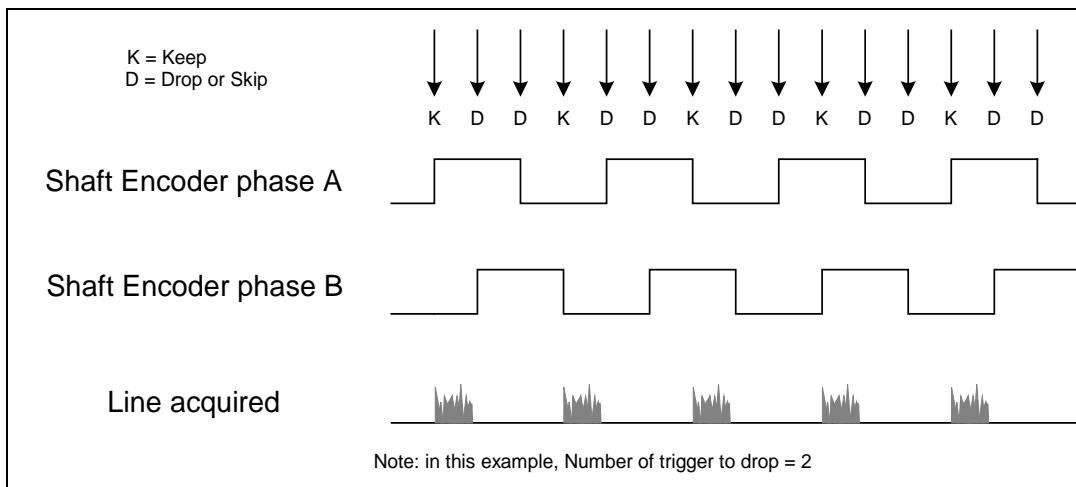


Figure 18: Encoder Input with Pulse-drop Counter

## Example using Sequential Encoder Input

Support of a dual phase encoder should consider the direction of motion of one phase signal to the other. Such a case might exist where system vibrations and/or conveyor backlash can cause the encoder to briefly travel backwards. The acquisition device must in those cases count the reverse steps and subtract the forward steps such that only pulses after the reverse count reaches zero are considered. By using the event "Shaft Encoder Reverse Counter Overflow", an application can monitor an overflow of this counter. The maximum count that can be reached by the counter is returned by the capability `CORACO_CAP_SHAFT_ENCODER_REVERSE_COUNT_MAX`. Reading the parameter `CORACO_PRM_SHAFT_ENCODER_REVERSE_COUNT` returns the current count value and writing any value to this parameter will reset the count to 0.

Also, if a maximum line rate camera trigger source is a high jitter shaft encoder, the parameter CORACQ\_PRM\_LINE\_TRIGGER\_AUTO\_DELAY can be used to automatically delay line triggers to avoid over-triggering a camera, and thus not miss a line. Note that some cameras integrate this feature. See also the [Acquisition Events](#) “Line Trigger Too Fast” that can be enabled when using the ‘auto delay’ feature.

The example figure below shows shaft encoder signals with high jitter. If the acquisition is triggered when phase B follows phase A, with jitter present phase B may precede phase A. Use of the *Shaft Encoder Direction* parameter will prevent false trigger conditions.

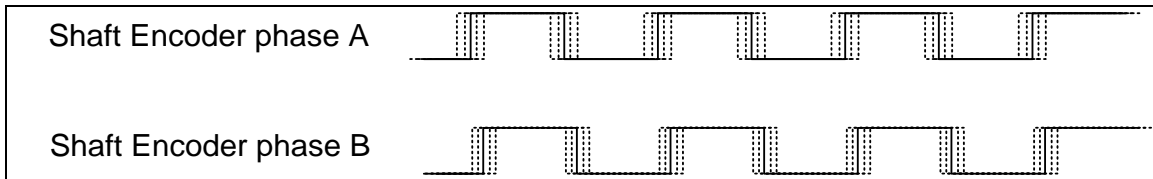


Figure 19: Using Shaft Encoder Direction Parameter



**Note:** Modify camera file parameters easily with the Sapera CamExpert program.

### CVI/CCF File Parameters Used

**Shaft Encoder Enable** = X, where:

- If X = 1, Shaft Encoder is enabled
- If X = 0, Shaft Encoder is disabled

**Shaft Encoder Pulse Drop** = X, where:

- X = number of trigger pulses ignored between valid triggers

**Shaft Encoder Pulse Multiply** = X, where:

- X = number of trigger pulses generated for each shaft encoder pulses

**Shaft Encoder Pulse Drop/Multiply Order** = X, where:

- If X = 1, the drop operation will be done first, followed by the multiplier operation
- If X = 0 or 2, the multiplier operation will be done first, followed by the drop operation

**Shaft Encoder Direction** = X, where:

- X = 0, Ignore direction
- X = 1, Forward steps are detected by pulse order A/B (forward motion)
- X = 2, Forward steps are detected by pulse order B/A (reverse motion)

**Shaft Encoder Level** = X, where:

- X = 1, TTL
- X = 2, RS-422



**Note:** For information on camera configuration files, see the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

---

# Virtual Frame Trigger for Line Scan Cameras

When using line scan cameras, a frame buffer is allocated in host system memory to store captured video lines. To control when a video line is stored as the first line in this “virtual” frame buffer, an external frame trigger signal is used.

For **fixed length** frames, the Sopera vertical cropping parameter controls the number of lines sequentially grabbed and stored in the virtual frame buffer.

For **variable length** frames, the External Frame Trigger (when a level or dual input type is selected) controls the number of lines sequentially grabbed up to the maximum of lines in the virtual frame buffer.

For both fixed and variable length frames, choosing an active low/high or dual input permits grabbing multiple consecutive images as long as the chosen signal is active. This action is also called “rolling over” to the next buffer. When choosing a single rising or falling edge, a single frame will be acquired; there is never any roll over.

External Frame Trigger Detection	Fixed Frame	Variable Frame
Active Low/High	Roll Over	Roll Over
Rising/Falling Edge	No Roll Over	No Roll Over
Dual Input Rising/Falling Edge	Roll Over	Roll Over

## Virtual Frame Trigger Timing Diagram

The virtual frame trigger signal (generated by some external event) connects to the Xtium2-CXP PX8 trigger input.

- Virtual frame trigger can be differential (RS-422) or single ended (TTL, 12V, or 24V) industry standard, and be rising or falling edge active, active high or low, or double pulse rising or falling edge.
- In this example, virtual frame trigger control is configured for rising edge trigger.
- Virtual frame trigger connects to the Xtium2-CXP PX8 via the External Trigger Input 1 & 2 inputs.
- Camera control signals are active at all times. These continually trigger the camera acquisition in order to avoid corrupted video lines at the beginning of a virtual frame.
- The camera control signals are either timing controls on Xtium2-CXP PX8 shaft encoder inputs, or line triggers generated internally by the Xtium2-CXP PX8.
- The Sopera vertical cropping parameter specifies the number of lines captured.

## Synchronization Signals for a 10 Line Virtual Frame

The following timing diagram shows the relationship between External Frame Trigger input, External Shaft Encoder input (one phase used with the second terminated), and camera control output to the camera.

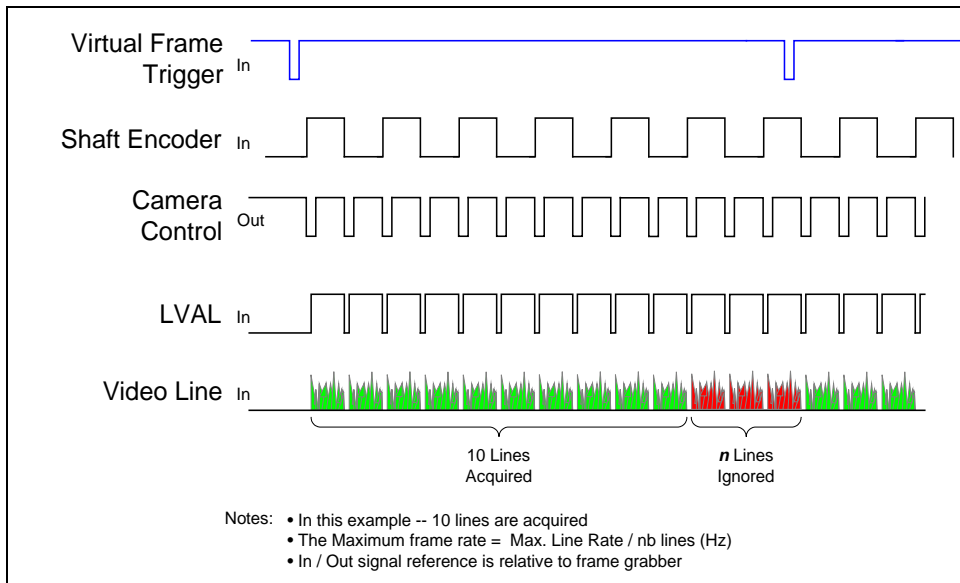


Figure 20: Synchronization Signals for a 10 Line Virtual Frame

## Synchronization Signals for Fixed Frame Length Acquisition

A trigger event is only generated when a grab is active; when not grabbing no trigger events are generated. When a frame is complete, the frame grabber checks for the specified active trigger level and, if present, grabs the next frame; otherwise, it waits for the next detected active trigger level.

In the following diagrams:

"T" indicates a valid external trigger event (SapAcquisition::EventExternalTrigger).  
 "Ignored" is an ignored event (SapAcquisition::EventExternalTriggerIgnored).

such that

$Ignored + T = \text{total triggers received by frame grabber}$

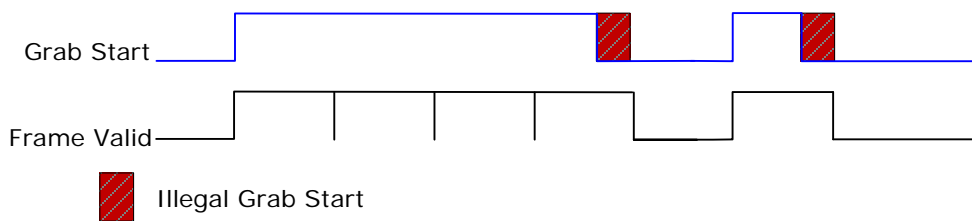


Figure 21: Line scan, Fixed Frame, No Trigger

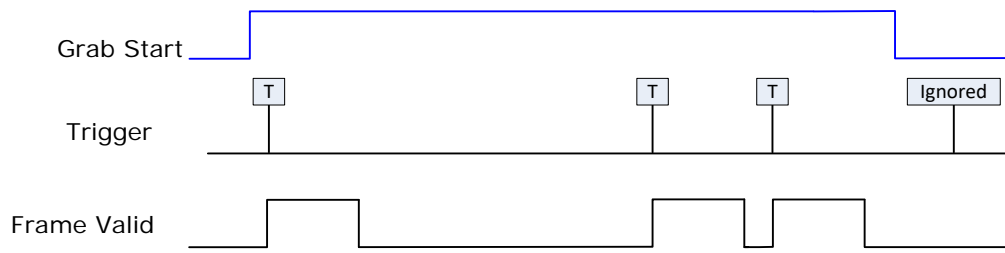


Figure 22: Line scan, Fixed Frame, Edge Trigger

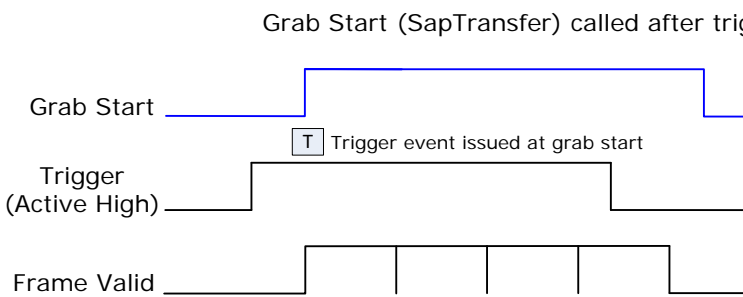
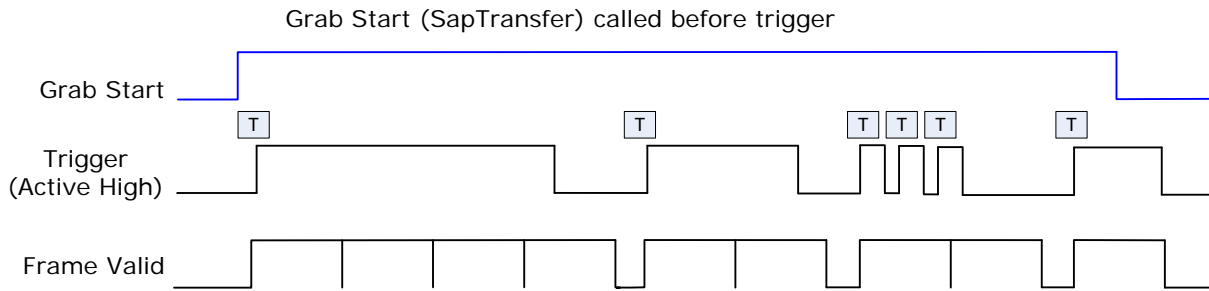


Figure 23: Line scan, Fixed Frame, Level Trigger (Roll-Over to Next Frame)

## Synchronization Signals for Variable Frame Length Acquisition

For variable length frames, trigger ignored events are not issued (SapAcquisition::EventExternalTriggerIgnored); a valid trigger event always initiates either a frame start or frame end.

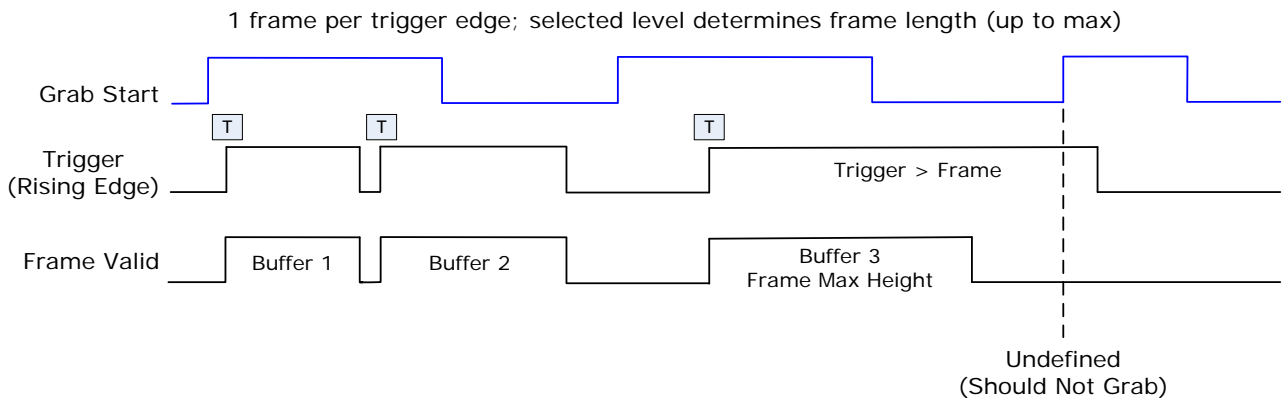


Figure 24: Line scan, Variable Frame, Edge Trigger (Active High determines Frame Length)

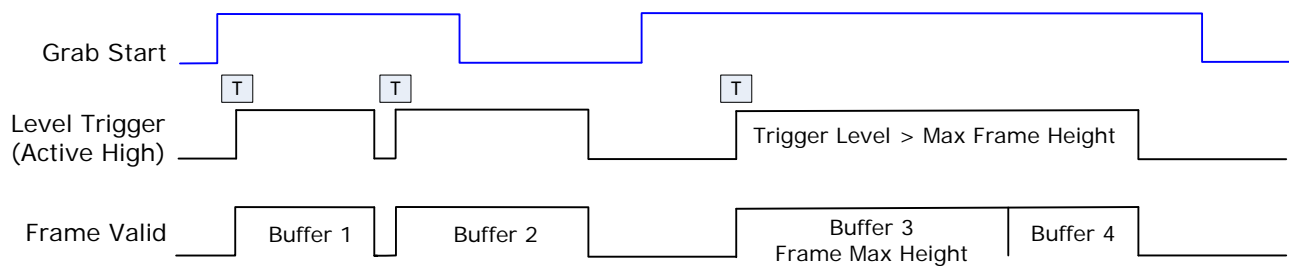


Figure 25: Line scan, Fixed Frame, Level Trigger (Roll-Over)

### CVI File (VIC) Parameters Used

The VIC parameters listed below provide the control functionality for virtual frame reset. Sopera applications load pre-configured CVI files or change VIC parameters during runtime.



**Note:** Sopera camera file parameters are easily modified by using the CamExpert program.

**External Frame Trigger Enable** =  $X$ , where: (with Virtual Frame Trigger enabled)

- If  $X = 1$ , External Frame Trigger is enabled
- If  $X = 0$ , External Frame Trigger is disabled

**External Frame Trigger Detection** =  $Y$ , where: (with Virtual Frame Trigger edge select)

- If  $Y = 1$ , External Frame Trigger is active low
- If  $Y = 2$ , External Frame Trigger is active high
- If  $Y = 4$ , External Frame Trigger is active on rising edge
- If  $Y = 8$ , External Frame Trigger is active on falling edge
- If  $Y = 32$ , External Frame Trigger is dual-input rising edge
- If  $Y = 64$ , External Frame Trigger is dual-input falling edge



**Note:** For dual-input triggers, Trigger Input #1 signals the start of the frame trigger, Trigger Input #2 signals the end of the frame trigger.

**External Frame Trigger Level** =  $Z$ , where: (with Virtual Frame Trigger signal type)

- If  $Z = 1$ , External Frame Trigger is a TTL signal
- If  $Z = 2$ , External Frame Trigger is differential signal (RS-422)
- If  $Z = 8$ , External Frame Trigger is a 24V signal
- If  $Z = 64$ , External Frame Trigger is a 12V signal



**Note:** For information on camera configuration files, see the Sopera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

---

# Sapera Acquisition Methods

Sapera acquisition methods define the control and timing of the camera and frame grabber board. Various methods are available, grouped as:

- Camera Trigger Methods (method 1 supported)
- Line Trigger Methods (method 1)
- Line Integration Methods (method 3 supported)
- Time Integration Methods (method 1 supported)
- Strobe Methods (method 1, 3 and 4 supported)

Refer to the Sapera LT Acquisition Parameters Reference manual (OC-SAPM-APR00) for detailed information concerning camera and acquisition control methods.



---

# Trigger to Image Reliability

Trigger-to-image reliability incorporates all stages of image acquisition inside an integrated controller to increase reliability and simplify error recovery. The trigger-to-image reliability model brings together all the requirements for image acquisition to a central management unit. These include signals to control camera timing, on-board frame buffer memory to compensate for PCI bus latency, and comprehensive error notification. If the Xtium2-CXP PX8 detects a problem, the application can take appropriate action to return to normal operation.

The Xtium2-CXP PX8 is designed with a robust ACU (Acquisition and Control Unit). The ACU monitors in real-time, the acquisition state of the input plus the DTE (Data Transfer Engine) which transfers image data from on-board memory into PC memory. In general, these management processes are transparent to end-user applications. With the Xtium2-CXP PX8, applications ensure trigger-to-image reliability by monitoring events and controlling transfer methods as described below:

## Supported Events and Transfer Methods

Listed below are the supported acquisition and transfer events. Event monitoring is a major component to the Trigger-to-Image Reliability framework.

### *Acquisition Module Events*

Acquisition events pertain to the acquisition module. They provide feedback on the image capture phase.

- **External Trigger (Used/Ignored)**  
Generated when the external trigger pin is asserted, which indicates the start of the acquisition process. There are two types of external trigger events: 'Used' or 'Ignored'. Following an external trigger, if the event generates a captured image, an External Trigger Used event will be generated (CORACQ\_VAL\_EVENT\_TYPE\_EXTERNAL\_TRIGGER).  
If there is no captured image, an External Trigger Ignored event will be generated (CORACQ\_VAL\_EVENT\_TYPE\_EXTERNAL\_TRIGGER\_IGNORED). An external trigger event is ignored if the event rate is higher than the possible frame rate of the camera.  
When using an active high/low or double pulse rising/falling edge trigger detection, the 2<sup>nd</sup> pulse will generate the External Trigger End event (CORACQ\_VAL\_EVENT\_TYPE\_EXTERNAL\_TRIGGER\_END).
- **Start of Frame**  
Event generated during acquisition, with the detection of the start of a video frame by the board acquisition hardware. The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_START\_OF\_FRAME.
- **End of Frame**  
Event generated during acquisition, with the detection of the end of a video frame by the board acquisition hardware. The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_END\_OF\_FRAME.
- **Data Overflow**  
The Data Overflow event indicates that there is not enough bandwidth for the acquired data transfer without loss. Data Overflow would occur with limitations of the acquisition module and should never occur.  
The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_DATA\_OVERFLOW.
- **Frame Valid**  
Event generated on detection of the start of a video frame by the board acquisition hardware. Acquisition does not need to be active; therefore, this event can verify a valid signal is connected. The Sopera event value is: CORACQ\_VAL\_EVENT\_TYPE\_VERTICAL\_SYNC.

- **Link Lock/Unlock)**  
Event generated on the transition from locking or not locking, of the required lanes. The Sopera event values are:  
CORACQ\_VAL\_EVENT\_TYPE\_LINK\_LOCK  
CORACQ\_VAL\_EVENT\_TYPE\_LINK\_UNLOCK.
- **Frame Lost**  
The Frame Lost event indicates that an acquired image failed to transfer to on-board memory. An example is if there are no free on-board buffers available for the new image. This may be the case if the image transfer from onboard buffers to host PC memory is not sustainable due to bus bandwidth issues or no host buffers are available to receive an image.  
The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_FRAME\_LOST.
- **External Line Trigger Too Slow**  
Event which indicates that the detected shaft encoder input tick rate is too slow for the device to take into account the specified shaft encoder multiplier value. The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_EXT\_LINE\_TRIGGER\_TOO\_SLOW.
- **Line Trigger Too Fast**  
Event which indicates a previous line-trigger did not generate a complete video line from the camera. Note that due to jitter associated with using shaft encoders, the acquisition device can delay a line trigger if a previous line has not yet completed. This event is generated if a second line trigger comes in while the previous one is still pending. This event is generated once per virtual frame. The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_LINE\_TRIGGER\_TOO\_FAST.
- **Shaft Encoder Reverse Count Overflow**  
Event which indicates that the shaft encoder has travelled in the opposite direction expected and that the number of pulses encountered during that travel has exceeded the acquisition device counter. The acquisition device will thus not be able to skip the appropriate number of pulses when the expected direction is detected. The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_SHAFT\_ENCODER\_REVERSE\_COUNT\_OVERFLOW
- **Camera Missed Trigger**  
Event which indicates that the frame grabber did not receive an acknowledge from the camera on the previous trigger message sent. The Sopera event value is CORACQ\_VAL\_EVENT\_TYPE\_CAMERA\_MISSED\_TRIGGER
- **Link Error**  
Event which indicates that an error has occurred on one or more of the lanes. Information about the source of the link error and the number of occurrences of this error can be retrieved using the SapAcqCallbackInfo class.
  - **GetGenericParam0:** returns the source of the error:
    - 1: CRC Error
    - 2: 8B/10B Error
    - 3: Packet Buffer Overflow
    - 4: Packet Size Error
  - **GetGenericParam1:** returns a bitfield indicating which lane(s) generated the error
    - Bit 0 = Lane 1, Bit 1= Lane 2, ...
  - **GetCustomSize:** returns 4 \* UINT32
  - **GetCustomData:** returns the number of errors per lane. There are 4 entries, each entry being a UINT32.
  - **Note:** 8B/10B error is the only error that is per lane. CRC error, Packet BufferOverflow and Packet Size Error is per camera and will always be linked to the master lane of the camera.

## Acquisition Device Events

Acquisition Device events are related to a camera connected to the frame grabber. They provide feedback on camera feature changes and camera events.

- **Feature Value Changed**

Generated when the value of a camera feature is changed.

Note: Value for this event type is: 0.

- **GetGenericParam0**: returns the index of the feature that was changed.  
Note: A value of -1 (ie. 0xFFFFFFFF) means that all of the features have changed. You will usually receive this value when a camera is connected.
- **GetHostTimeStamp**: returns a 64-bit value representing the time at which the host received the event. The time base of the value is in CPU clock.

- **Device Event**

Generated when the frame grabber receives a CXP event from the camera.

Note: Value for this event type is: 2.

- **GetGenericParam0**: returns an 8-bit packet tag ID, incremented by 1 for each new event packet sent by the camera.
- **GetGenericParam1**: returns a 16-bit CXP Device Event Info as per CXP specifications. It represents the 1<sup>st</sup> WORD of a CXP event message.
  - 0..11: 12-bit field specifying the event source.
  - 12:13: 2-bit field. Reserved. Set to 0.
  - 14:15: 2-bit field specifying the event Namespace.
    - 0 = GenICam Event ID.
    - 1 = CoaXPress Specific Event ID (reserved for future use).
    - 2 = Device Specific Event ID.
    - 3 = Reserved for future use.
- **GetCustomSize**: 16-bit value returning the number of data bytes for this event message.
- **GetCustomData**: returns the event message data.
- **GetHostTimeStamp**: returns a 64-bit value representing the time at which the host received the event. The time base of the value is in CPU clock.
- **GetAuxTimeStamp**: returns a 64-bit value representing the time stamp of the CXP event message as per CXP specifications.

## ***Transfer Events***

Transfer events are those related to the transfer module. Transfer events provide feedback on image transfer from onboard memory frame buffers to PC memory frame buffers.

- **Start of Frame**  
Start of Frame event generated when the first image pixel is transferred from on-board memory into PC memory.  
The Sopera event value is CORXFER\_VAL\_EVENT\_TYPE\_START\_OF\_FRAME.
- **End of Frame**  
End of Frame event generated when the last image pixel is transferred from on-board memory into PC memory.  
The Sopera event value is CORXFER\_VAL\_EVENT\_TYPE\_END\_OF\_FRAME.
- **End of Line**  
The End of Line event is generated after a video line is transferred to a PC buffer.  
The Sopera event value is CORXFER\_VAL\_EVENT\_TYPE\_END\_OF\_LINE.
- **End of N Lines**  
The End of N Lines event is generated after a set number of video lines are transferred to a PC buffer. The Sopera event value is CORXFER\_VAL\_EVENT\_TYPE\_END\_OF\_NLINES.
- **End of Transfer**  
End of Transfer event generated at the completion of the last image transfer from on-board memory into PC memory. Issue a stop command to the transfer module to complete a transfer (if transfers are already in progress). If a frame transfer of a fixed number of

images is requested, the transfer module will stop transfer automatically. The Sapera event value is CORXFER\_VAL\_EVENT\_TYPE\_END\_OF\_TRANSFER.

## **Trigger Signal Validity**

The ACU ignores external trigger signal noise with its programmable debounce control. Program the debounce parameter for the minimum pulse duration considered as a valid external trigger pulse. For more information, see [Note 1: General Inputs / External Trigger Inputs Specifications](#).

## **Supported Transfer Cycling Methods**

The Xtium2-CXP PX8 supports the following transfer modes, which are either synchronous or asynchronous.

Images are accumulated in on-board memory in a FIFO type manner. On-board memory can get filled up if the rate at which the images are acquired is greater than the rate at which the DMA engine can write them to host buffer memory. On-board memory can also get filled-up if there are no more empty buffers available to transfer the on-board images.

When no memory is available for a new image to be stored in on-board memory, the image is discarded and a CORACO\_VAL\_EVENT\_TYPE\_FRAME\_LOST or trash buffer callback is generated. If a CORACO\_VAL\_EVENT\_TYPE\_FRAME\_LOST occurs when host buffers are available, it can indicate a problem with the PX4 bus bandwidth.

If image buffers are constructed using a trash buffer (SapBufferWithTrash using a transfer cycle mode with trash), when no host buffers are available and no memory is available for a new image to be stored in on-board memory, the SapXferCallBackInfo::IsTrash (C++) function or SapXferNotifyEventsArgs.Trash (.NET) property returns true. If a trash callback function has been registered during construction of the SapTransfer object, it will be executed when a trash event occurs.

When stopping the image acquisition, the event CORXFER\_VAL\_EVENT\_TYPE\_END\_OF\_TRANSFER will occur once all images currently in the on-board memory are transferred to host buffer memory. Note that if the application does not provide enough empty buffers, the Xtium event will not occur and an acquisition abort will be required.

- CORXFER\_VAL\_CYCLE\_MODE\_SYNCHRONOUS\_WITH\_TRASH  
Before cycling to the next buffer in the list, the transfer device will check the next buffer's state. If its state is full, the transfer will keep the image in on-board memory until the next buffer's state changes to empty. If the on-board memory gets filled, trash callbacks will be generated.
- CORXFER\_VAL\_CYCLE\_MODE\_SYNCHRONOUS\_NEXT\_EMPTY\_WITH\_TRASH  
When starting an acquisition, the buffer list is put in an empty buffer queue list in the exact order they were added to the transfer. Whenever a user sets a buffer to empty, it is added to the empty buffer queue list, so that after cycling once through the original buffer list, the buffers acquired into will follow the order in which they are put empty by the user. So in this mode, the on-board images will be transferred to host buffer memory as long as there are buffers in the empty buffer queue list. If no buffers are available on the host and the on-board memory gets filled, trash callbacks will be generated.
- CORXFER\_VAL\_CYCLE\_MODE\_ASYNCHRONOUS  
The transfer device cycles through all buffers in the list without concern about the buffer state.

The following table describes the possible buffer states and resulting behavior.

Table 6: Buffer states.

Trash Buffer (cycling mode with trash)	Xtium On-Board Memory State	Host Sapera Buffer State	Resulting Event
NO	Empty buffer available (at least 1)	Empty buffer available (at least 1)	Normal acquisition events
NO	Empty buffer available (at least 1)	Full	Acquire into Xtium on-board memory
NO	Full	Empty buffer available (at least 1)	Frame Lost Event
NO	Full	Full	Frame Lost Event
YES	Empty buffer available (at least 1)	Empty buffer available (at least 1)	Normal acquisition events
YES	Empty buffer available (at least 1)	Full	Acquire into Xtium on-board memory
YES	Full	Empty buffer available (at least 1)	Frame Lost Event
YES	Full	Full	Trash Callback

By default, the buffer state (empty or full) is automatically managed by Sapera LT; it can be managed manually by the user if necessary.

# Output LUT Availability

The following table defines the supported output LUT (look up tables) for the Xtium2-CXP PX8. Note that unsupported modes are not listed.

Table 7: Output LUT Availability

Number of Digital Bits	Output Pixel Format	LUT Format	Notes*
8	MONO 8	8-in, 8-out	8 bits in 8 LSBs of 16-bit
8	MONO 16	8-in, 16-out	
10	MONO 8	10-in, 8-out	
10	MONO 16	10-in, 16-out	10 bits in 10 LSBs of 16-bit
12	MONO 8	12-in, 8-out	8 MSB
12	MONO 16	12-in, 16-out	12 bits in 12 LSBs of 16-bit
8 x 3 (RGB)	RGB888 RGB8888 RGBP8	8-in, 8-out	
10 x 3 (RGB)	RGB888 RGB8888 RGB101010 RGB161616 RGB16161616	10-in, 8-out 10-in, 8-out 10-in, 10-out 10-in, 10-out 10-in, 16-out	10 bits in 10 LSBs of 16-bit
12 x 3 (RGB)	RGB888 RGB8888 RGB101010 RGB161616 RGB16161616	12-in, 8-out 12-in, 8-out 12-in, 10-out 12-in, 16-out 12-in, 16-out	12 bits in 12 LSBs of 16-bit

\*When no LUTs are available or LUTs are disabled, the data is packed in the LSBs of the target destination.

---

# Metadata: Theory of Operation

The following provides additional details on the metadata implementation.

## Metadata Data Structure

The Xtium2-CXP PX8 supports metadata at the end of each line when enabled through the parameter `CORACQ_PRM_META_DATA`. The metadata consists of 64 bytes. The content of the metadata represents a snapshot of the state of the frame grabber at the beginning of each LVAL received.

```
typedef struct
{
    ULONGLONG shaftEncoderCount;
    ULONGLONG lineCount;
    ULONGLONG lineTriggerCount;
    ULONGLONG timeStamp;
    ULONG frameCounter;
    UCHAR generalInputs;
    UCHAR generalOutputs;
    UCHAR biDirectionalIOs;
    UCHAR reserved[25];
} MX4_METADATA, *PMX4_METADATA;
```

- **shaftEncoderCount**: 64-bit counter of pulses received on the shaft encoder. This is a 'machine counter' that increments in one direction (forward) and decrements (reverse) in the opposite direction.
- **lineCount**: 64-bit counter of line valid (LVAL) received.
- **lineTriggerCount**: 64-bit counter of line triggers sent to the camera.
- **timeStamp**: 64-bit counter of the frame grabber on-board timestamp. See also `CORACQ_PRM_TIME_STAMP_BASE` and `CORACQ_PRM_TIME_STAMP`.
- **frameCounter**: 32-bit counter of frames received. This represents the frame number that the line belongs to.
- **generalInputs**: status of the general inputs (for example, Low, bit = 0 or High, bit = 1).
- **generalOutputs**: status of the general outputs (for example, Low, bit = 0 or High, bit = 1).
- **biDirectionalIOs**: status of the bi-directional I/Os (for example, Low, bit = 0 or High, bit = 1).
- **reserved**: 25 bytes reserved for future usage.

## Clearing Metadata Counters

To clear (reset) the metadata counters to zero (0), use the `CORACQ_PRM_META_DATA_CLEAR` parameter.

## Metadata Example

For a demo application showing this feature, please contact Teledyne DALSA technical support.

---

# Flat Field Correction: Theory of Operation

The following provides additional details on the Flat Field Correction and Flat Line Correction (FFC/FLC) implementation.

## Flat Field Correction Lists

The Xtium2-CXP PX8 supports defining more than one Flat Field Correction (FFC) / Flat Line Correction (FLC) data sets. Using the Xfer parameter `CORXFER_PRM_FLATFIELD_CYCLE_MODE`, the user can decide to cycle automatically through the list of FFC/FLC sets by setting the parameter to `CORXFER_VAL_FLATFIELD_CYCLE_MODE_AUTOMATIC`, or select a specific FFC/FLC set from the list by setting the parameter to `CORXFER_VAL_FLATFIELD_CYCLE_MODE_OFF` and selecting the FFC/FLC index to use with the parameter `CORACQ_PRM_FLAT_FIELD_SELECT`.

While the cycling mode is set to off, users can upload new coefficients to an inactive FFC set even when grabbing. When cycling automatically, the FFC/FLC sets are selected in a round-robin fashion, changing at the beginning of every new frame.

The architecture of the Xtium2-CXP PX8 is such that the FFC/FLC data sets are independent of the host buffers. In automatic mode, the FFC/FLC sets are chosen in a round-robin fashion as images are acquired. So if using the Xfer cycling mode Synchronous with Trash, it is recommended that the number of host buffers be a multiple of the number of FFC/FLC in the list in order to maintain the FFC/FLC relationship with the Host buffers.

- When the FFC/FLC cycle mode automatic is active, reset the acquisition module to start on the 1<sup>st</sup> FFC/FLC data set of the selected list as follows:
  - Disconnect/Reconnect the transfer (assuming 1<sup>st</sup> buffer is empty).
  - Selecting a set using the `CORACQ_PRM_FLAT_FIELD_SET_SELECT` parameter will choose the 1<sup>st</sup> FFC/FLC in the list of the selected set.
- When the FFC/FLC cycle mode automatic is active, start the acquisition module to start on a specific FFC/FLC of the selected list as follows:
  - While acquisition is stopped, by selecting an Xfer pair [ACQ, Buffer]. The index of the FFC/FLC will be selected based on the modulo of the number of FFC/FLC in the list with respect to the [ACQ, Buffer] index pair.

## Flat Field Correction Sets

The concept of sets allows a user to define multiple lists of FFC/FLC correction data. The FFC/FLC API allows users to allocate and pre-program those FFC/FLC sets. When acquiring images, the board driver will cycle through the FFC/FLC list of the selected set. During that operation, users can upload new FFC/FLC data to non-active sets without any ill effects.

When changing the active set while grabbing, the new active set will be switched when the current cycling of the current list is completed.

### ***Xtium2-CXP PX8 specific limitations***

- Software driver permits the creation of up to 16 FFC/FLC sets.
- Software driver permits the use of up to 16 sets.
- When the FFC cycling mode is off, the concept of sets is not used. Whichever a FFC index is chosen using `CORACQ_PRM_FLAT_FIELD_SELECT`, it will be used independently of the set it belongs to.



- Upload of any FFC data is permitted at any time, even while grabbing. If an upload is done to an FFC index of the currently select set while grabbing, then the resulting acquired image will be undefined.
- When changing FFC cycling mode, the acquisition must be stopped.

## ***Programming the sets***

The following scheme is used to program FFC/FLC data within a set:

```
// select an active set
CorAcqSetPrm( hAcq, CORAQ_PRM_FLAT_FIELD_SET_SELECT, 0);

// Create 4 new FFC that will be part of the currently active set '0'
For( i = 0; i < 4; i++)
{
CorAcqNewFlatfield( hAcq, pFlatfieldNumber); // Will create FFC #1, #2, #3, #4
}

// select an active set
CorAcq SetPrm( hAcq, CORAQ_PRM_FLAT_FIELD_SET_SELECT, 1);

// Create 4 new FFC that will be part of the currently active set '1'
For( i = 0; i < 4; i++)
{
CorAcqNewFlatfield( hAcq, pFlatfieldNumber); // Will create FFC #5, #6, #7, #8
}
```

# Xtium2-CXP PX8 Supported Parameters

The tables below describe the Sapera capabilities supported by the Xtium2-CXP PX8. Unless specified, each capability applies to all configuration modes and all acquisition modes.

The information here is subject to change. The application needs to verify capabilities. New board driver releases may change product specifications.

Sapera describes the Xtium2-CXP PX8 family as:

- Board Server: Xtium2-CXP\_PX8\_1
- Acquisition Module: *dependent on firmware used*

## Camera Related Capabilities

Table 8: Camera Related Capabilities

Capability	Values
CORACQ_CAP_CONNECTOR_TYPE	CORACQ_VAL_CONNECTOR_TYPE_CXP (0x20)

## Camera Related Parameters

Table 9: Camera Related Parameters

Parameter		Values
CORACQ_PRM_CHANNEL		CORACQ_VAL_CHANNEL_SINGLE (0x1) CORACQ_VAL_CHANNEL_DUAL (0x2)
CORACQ_PRM_FRAME		CORACQ_VAL_FRAME_PROGRESSIVE (0x2)
CORACQ_PRM_INTERFACE		CORACQ_VAL_INTERFACE_DIGITAL (0x2)
CORACQ_PRM_SCAN		CORACQ_VAL_SCAN_AREA (0x1) CORACQ_VAL_SCAN_LINE (0x2)
CORACQ_PRM_SIGNAL		CORACQ_VAL_SIGNAL_DIFFERENTIAL (0x2)
CORACQ_PRM_VIDEO	<i>Mono</i>	CORACQ_VAL_VIDEO_MONO (0x1) CORACQ_VAL_VIDEO_BAYER (0x10)
	<i>RGB</i>	CORACQ_VAL_VIDEO_RGB (0x8) CORACQ_VAL_VIDEO_RGBY (0x40)
	<i>Bayer</i>	CORACQ_VAL_VIDEO_BAYER (0x10)
CORACQ_PRM_PIXEL_DEPTH	<i>Mono</i>	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8 8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO16 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO16 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO8 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_MONO16 14 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO16 16 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO16
	<i>RGB</i>	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI16 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI16
	<i>Bayer</i>	8 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10 10 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI16 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI8 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI10 12 bits, # LUT = 1, LUT format = CORDATA_FORMAT_COLORNI16
CORACQ_PRM_VIDEO_STD		CORACQ_VAL_VIDEO_STD_NON_STD (0x1)
CORACQ_PRM_FIELD_ORDER		CORACQ_VAL_FIELD_ORDER_NEXT_FIELD (0x4)
CORACQ_PRM_HACTIVE	<i>Mono</i>	min = 32 pixel max = 65536 pixel step = 1 pixel
	<i>Bayer</i>	min = 32 pixel max = 65536 pixel step = 1 pixel
	<i>RGB</i>	min = 32 pixel max = 21844 pixel step = 1 pixel

Parameter		Values
CORACQ_PRM_VACTIVE		min = 1 line max = 16777215 line step = 1 line
CORACQ_PRM_TIME_INTEGRATE_METHOD		CORACQ_VAL_TIME_INTEGRATE_METHOD_1 (0x1)
CORACQ_PRM_CAM_TRIGGER_METHOD		CORACQ_VAL_CAM_TRIGGER_METHOD_1 (0x1)
CORACQ_PRM_CAM_TRIGGER_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_CAM_TRIGGER_DURATION		min = 5 µsec max = 85899345 µs step = 1 µsec
CORACQ_PRM_CAM_NAME	Mono RGB Bayer	Default Camera CXP Area Scan Mono Default Camera CXP Area Scan Color Default Camera CXP Bayer Area Scan Color
CORACQ_PRM_LINE_INTEGRATE_METHOD		CORACQ_VAL_LINE_INTEGRATE_METHOD_3 (0x4)
CORACQ_PRM_LINE_TRIGGER_METHOD		CORACQ_VAL_LINE_TRIGGER_METHOD_1 (0x1)
CORACQ_PRM_LINE_TRIGGER_POLARITY		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_LINE_TRIGGER_DELAY		min = 0 nsec max = 4294967295 nsec step = 1 nsec
CORACQ_PRM_LINE_TRIGGER_DURATION		min = 5000 nsec max = 4294967295 nsec step = 1 nsec
CORACQ_PRM_TAPS		Max = 1 tap
CORACQ_PRM_TAP_1_DIRECTION		CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40)
CORACQ_PRM_TAP_2_DIRECTION		CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_DU (0x8) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10) CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x20) CORACQ_VAL_TAP_DIRECTION_FROM_BOT (0x40) * Used by Channel #2
CORACQ_PRM_CHANNELS_ORDER		CORACQ_VAL_CHANNELS_ORDER_NORMAL (0x1) CORACQ_VAL_CHANNELS_ORDER_REVERSE (0x2)
CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MIN		1 Hz
CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MAX		10000000 Hz
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MIN		1 µs
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MAX		85899345 µs
CORACQ_PRM_CAM_IO_CONTROL (*)		
CORACQ_PRM_LINE_INTEGRATE_DELAY		min = 0 nsec max = 4294967295 nsec step = 1 nsec
CORACQ_PRM_COLOR_ALIGNMENT	Bayer	CORACQ_VAL_COLOR_ALIGNMENT_GB_RG (0x1) CORACQ_VAL_COLOR_ALIGNMENT_BG_GR (0x2) CORACQ_VAL_COLOR_ALIGNMENT_RG_GB (0x4) CORACQ_VAL_COLOR_ALIGNMENT_GR_BG (0x8)
CORACQ_PRM_CAM_CONTROL_DURING_READOUT		CORACQ_VAL_CAM_CONTROL_DURING_READOUT_INVALID (0x0) CORACQ_VAL_CAM_CONTROL_DURING_READOUT_VALID (0x01) CORACQ_VAL_CAM_CONTROL_DURING_READOUT_IGNORE (0x2)
CORACQ_PRM_DATA_LANES		min = 1 lane, max = 1, 2 or 4 lanes depending of board model and configuration selected
CORACQ_PRM_CXP_CONFIGURATION		CORACQ_VAL_CXP_CONFIGURATION_DUAL_CHANNEL_ONE_STREAM (0x1)

Parameter	Values
CORACQ_PRM_BIT_TRANSFER_RATE	1.250 Gbps 2.500 Gbps 3.125 Gbps 5.000 Gbps 6.250 Gbps 10.000 Gbps 12.500 Gbps * 10.000 and 12.500 availability is dependent on the board model.

## VIC Related Parameters

Table 10: VIC Related Parameters

Parameter	Values
CORACQ_PRM_CAMSEL	Mono CAMSEL_MONO = from 0 to 0 RGB CAMSEL_RGB = from 0 to 0 Bayer
CORACQ_PRM_CROP_LEFT	Mono min = 0 pixel max = 131040 pixel step = 4 pixel Bayer RGB min = 0 pixel max = 32736 pixel step = 8 pixel
CORACQ_PRM_CROP_TOP	min = 0 line max = 16777215 line step = 1 line
CORACQ_PRM_CROP_WIDTH	Mono min = 32 pixel max = 131072 pixel step = 4 pixel Bayer min = 32 pixel max = 32768 pixel step = 4 pixel RGB min = 32 pixel max = 32768 pixel step = 1 pixel (Maximum allowed is 128 kB, so maximum in pixels is dependent on the output pixel depth.)
CORACQ_PRM_CROP_HEIGHT	min = 1 line max = 16777215 line step = 1 line
CORACQ_PRM_DECIMATE_METHOD	CORACQ_VAL_DECIMATE_DISABLE (0x1)
CORACQ_PRM_LUT_ENABLE	TRUE FALSE
CORACQ_PRM_LUT_NUMBER	Default = 0
CORACQ_PRM_STROBE_ENABLE	TRUE FALSE
CORACQ_PRM_STROBE_METHOD	CORACQ_VAL_STROBE_METHOD_1 (0x1) CORACQ_VAL_STROBE_METHOD_3 (0x4) CORACQ_VAL_STROBE_METHOD_4 (0x8)
CORACQ_PRM_STROBE_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_STROBE_DURATION	min = 1 $\mu$ s max = 85899345 $\mu$ s step = 1 $\mu$ s
CORACQ_PRM_STROBE_DELAY	min = 0 $\mu$ s max = 85899345 $\mu$ s step = 1 $\mu$ s
CORACQ_PRM_TIME_INTEGRATE_ENABLE	TRUE FALSE
CORACQ_PRM_TIME_INTEGRATE_DURATION	min = 5 $\mu$ s max = 85899345 $\mu$ s step = 1 $\mu$ s

Parameter		Values
CORACQ_PRM_CAM_TRIGGER_ENABLE		TRUE FALSE
CORACQ_PRM_OUTPUT_FORMAT	<i>Mono</i>  <i>RGB</i>  <i>Bayer</i>	CORACQ_VAL_OUTPUT_FORMAT_MONO8 CORACQ_VAL_OUTPUT_FORMAT_MONO16  CORACQ_VAL_OUTPUT_FORMAT_RGB8888 CORACQ_VAL_OUTPUT_FORMAT_RGB888 CORACQ_VAL_OUTPUT_FORMAT_RGB101010 CORACQ_VAL_OUTPUT_FORMAT_RGB161616 CORACQ_VAL_OUTPUT_FORMAT_RGB16161616 CORACQ_VAL_OUTPUT_FORMAT_RGBP8 (8-bit only) CORACQ_VAL_OUTPUT_FORMAT_RGBP16 (10 and 12-bit only)  CORACQ_VAL_OUTPUT_FORMAT_RGB8888 CORACQ_VAL_OUTPUT_FORMAT_RGB888 CORACQ_VAL_OUTPUT_FORMAT_RGB101010 CORACQ_VAL_OUTPUT_FORMAT_RGB161616 CORACQ_VAL_OUTPUT_FORMAT_RGB16161616 CORACQ_VAL_OUTPUT_FORMAT_RGBP8 (8-bit only) CORACQ_VAL_OUTPUT_FORMAT_RGBP16 (10 and 12-bit only) CORACQ_VAL_OUTPUT_FORMAT_MONO8 CORACQ_VAL_OUTPUT_FORMAT_MONO16
CORACQ_PRM_EXT_TRIGGER_ENABLE		CORACQ_VAL_EXT_TRIGGER_OFF (0x1) CORACQ_VAL_EXT_TRIGGER_ON (0x8)
CORACQ_PRM_VIC_NAME	<i>Mono</i> <i>RGB</i> <i>Bayer</i>	Default Camera CXP Area Scan Mono Default Camera CXP Area Scan Color Default Camera CXP Bayer Area Scan Color
CORACQ_PRM_LUT_MAX		1
CORACQ_PRM_EXT_TRIGGER_DETECTION		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2) CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8)
CORACQ_PRM_LUT_FORMAT	<i>Mono</i> <i>RGB</i> <i>Bayer</i>	Default = CORDATA_FORMAT_MONO8 Default = CORDATA_FORMAT_COLORNI8
CORACQ_PRM_LINE_INTEGRATE_ENABLE		TRUE FALSE
CORACQ_PRM_LINE_INTEGRATE_DURATION		min = 5000 nsec max = 4294967295 nsec step = 1 nsec
CORACQ_PRM_LINE_TRIGGER_ENABLE		TRUE FALSE
CORACQ_PRM_EXT_FRAME_TRIGGER_ENABLE		TRUE FALSE
CORACQ_PRM_EXT_FRAME_TRIGGER_DETECTION		CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2) CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8) CORACQ_VAL_DOUBLE_PULSE_RISING_EDGE (0x20) CORACQ_VAL_DOUBLE_PULSE_FALLING_EDGE (0x40) CORACQ_VAL_DOUBLE_PULSE_RISING_EDGE_ORDER_REVERSE (0x80) CORACQ_VAL_DOUBLE_PULSE_FALLING_EDGE_ORDER_REVERSE (0x100)
CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE		TRUE FALSE
CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION		CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8)
CORACQ_PRM_SNAP_COUNT		Not Available
CORACQ_PRM_INT_LINE_TRIGGER_ENABLE		TRUE FALSE
CORACQ_PRM_INT_LINE_TRIGGER_FREQ		Default = 5000 Hz
CORACQ_PRM_BIT_ORDERING		CORACQ_VAL_BIT_ORDERING_STD (0x1)
CORACQ_PRM_EXT_TRIGGER_LEVEL		CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2) CORACQ_VAL_LEVEL_12VOLTS (0x040) CORACQ_VAL_LEVEL_24VOLTS (0x8)

Parameter	Values
CORACQ_PRM_STROBE_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1)
CORACQ_PRM_EXT_FRAME_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2) CORACQ_VAL_LEVEL_12VOLTS (0x040) CORACQ_VAL_LEVEL_24VOLTS (0x8)
CORACQ_PRM_EXT_LINE_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MIN	8 Hz
CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MAX	500000 Hz
CORACQ_PRM_MASTER_MODE	Not available
CORACQ_PRM_SHAFT_ENCODER_DROP	min = 0 tick max = 254 tick step = 1 tick
CORACQ_PRM_SHAFT_ENCODER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_TRIGGER_FRAME_COUNT	min = 1 frame max = 16777214 frame step = 1 frame
CORACQ_PRM_INT_FRAME_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_INT_FRAME_TRIGGER_FREQ	min = 1 millihertz max = 41 000 000 millihertz step = 1 millihertz
CORACQ_PRM_STROBE_DELAY_2	Not Available
CORACQ_PRM_FRAME_LENGTH	CORACQ_VAL_FRAME_LENGTH_FIX (0x1) CORACQ_VAL_FRAME_LENGTH_VARIABLE (0x2)
CORACQ_PRM_FLIP	CORACQ_VAL_FLIP_OFF (0x00) CORACQ_VAL_FLIP_HORZ (0x01)
CORACQ_PRM_EXT_TRIGGER_DURATION	min = 0 µs max = 255 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_DELAY	min = 0 µs max = 85899345 µs step = 1 µs
CORACQ_PRM_CAM_TRIGGER_DELAY	min = 0 µs max = 85899345 µs step = 1 µs
CORACQ_PRM_SHAFT_ENCODER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_LUT_NENTRIES	8-bit/pixel component 256 entries 10-bit/pixel component 1024 entries 12-bit/pixel component 4096 entries 14/16-bit/pixel component 0 entries
CORACQ_PRM_EXT_FRAME_TRIGGER_SOURCE (*)	min = 0 max = 7 step = 1
CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE (*)	min = 0 max = 5 step = 1
CORACQ_PRM_EXT_TRIGGER_SOURCE (*)	min = 0 max = 7 step = 1
CORACQ_PRM_SHAFT_ENCODER_MULTIPLY	min = 1 max = 32 step = (2 <sup>N</sup> )
CORACQ_PRM_EXT_TRIGGER_DELAY	min = 0 max = 16777215 step = 1
CORACQ_PRM_EXT_TRIGGER_DELAY_TIME_BASE	CORACQ_VAL_TIME_BASE_LINE_VALID (0x4) CORACQ_VAL_TIME_BASE_LINE_TRIGGER (0x8) CORACQ_VAL_TIME_BASE_SHAFT_ENCODER (0x40) CORACQ_VAL_TIME_BASE_NS (0x80)

Parameter		Values
CORACQ_PRM_COLOR_DECODER_ENABLE	Mono RGB Bayer	Not Available TRUE FALSE
CORACQ_PRM_COLOR_DECODER_METHOD	Bayer	CORACQ_VAL_COLOR_DECODER_METHOD_1 (0x1)
CORACQ_PRM_WB_GAIN	RGB Bayer	min = 100000 max = 900000 step = 1
CORACQ_PRM_WB_GAIN_RED	RGB Bayer	min = 100000 max = 900000 step = 1
CORACQ_PRM_WB_GAIN_GREEN	RGB Bayer	min = 100000 max = 900000 step = 1
CORACQ_PRM_WB_GAIN_BLUE	RGB Bayer	min = 100000 max = 900000 step = 1
CORACQ_PRM_EXT_TRIGGER_IGNORE_DELAY		min = 0 max = 85899345 step = 1
CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE (*)		min = 0 max = 6 step = 1
CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE (*)		min = 0 max = 6 step = 1
CORACQ_PRM_EXT_TRIGGER_SOURCE_STR		[0] = Automatic [1] = External Trigger #1 [2] = External Trigger #2 [3] = Board Sync #1 [4] = Board Sync #2 [5] = Software Trigger [6] = External Trigger #3 [7] = External Trigger #4
CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE_STR		[0] = Automatic [1] = Shaft Encoder Phase A [2] = Shaft Encoder Phase B [3] = Shaft Encoder Phase A & B [4] = Board Sync #1 [5] = Board Sync #2
CORACQ_PRM_VERTICAL_TIMEOUT_DELAY		Not Available
CORACQ_PRM_POCP_ENABLE		TRUE FALSE
CORACQ_PRM_SHAFT_ENCODER_DIRECTION		CORACQ_VAL_SHAFT_ENCODER_DIRECTION_IGNORE (0x00) CORACQ_VAL_SHAFT_ENCODER_DIRECTION_FORWARD (0x01) CORACQ_VAL_SHAFT_ENCODER_DIRECTION_REVERSE (0x02) CORACQ_VAL_SHAFT_ENCODER_DIRECTION_RESCAN (0x4) CORACQ_VAL_SHAFT_ENCODER_DIRECTION_COUNT (0x8)
CORACQ_PRM_LINE_TRIGGER_AUTO_DELAY		CORACQ_VAL_LINE_TRIGGER_AUTO_DELAY_DISABLE (0x0) CORACQ_VAL_LINE_TRIGGER_AUTO_DELAY_FREQ_MAX (0x2)
CORACQ_PRM_TIME_STAMP_BASE		CORACQ_VAL_TIME_BASE_US (0x1) CORACQ_VAL_TIME_BASE_LINE_VALID (0x4) CORACQ_VAL_TIME_BASE_LINE_TRIGGER (0x8) CORACQ_VAL_TIME_BASE_SHAFT_ENCODER (0x40) CORACQ_VAL_TIME_BASE_100NS (0x200)
CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE_STR		[0] = Disabled [1] = External Frame Trigger [2] = Reserved [3] = External Trigger Ignore Region [4] = Shaft Encoder Before Mult/Drop [5] = Shaft Encoder After Mult/Drop [6] = Internal Line Trigger

Parameter	Values
CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE_STR	[0] = Disabled [1] = External Frame Trigger [2] = Reserved [3] = External Trigger Ignore Region [4] = Shaft Encoder Before Mult/Drop [5] = Shaft Encoder After Mult/Drop [6] = Internal Line Trigger
CORACQ_PRM_SHAFT_ENCODER_ORDER	CORACQ_VAL_SHAFT_ENCODER_ORDER_AUTO (0X0) CORACQ_VAL_SHAFT_ENCODER_ORDER_DROP_MULTIPLY (0X1) CORACQ_VAL_SHAFT_ENCODER_ORDER_MULTIPLY_DROP (0X2)  * For auto mode, the order is multiply/drop.
CORACQ_PRM_CAM_FRAMES_PER_TRIGGER	min = 0 max = 65534 step = 1
CORACQ_PRM_LINE_INTEGRATE_TIME_BASE	CORACQ_VAL_TIME_BASE_NS (0X80)
CORACQ_PRM_EXT_TRIGGER_IGNORE_REGION_DURATION	min = 0 $\mu$ s max = 6553 $\mu$ s step = 1 $\mu$ s
CORACQ_PRM_STROBE_DESTINATION (*)	min = 0 max = 4 step = 1
CORACQ_PRM_STROBE_DESTINATION_STR	[0] = Automatic [1] = Strobe #1 [2] = Strobe #2 [3] = Strobe #3 [4] = Strobe #4
CORACQ_PRM_SHAFT_ENCODER_AVERAGING_ENABLE	TRUE FALSE
CORACQ_PRM_SHAFT_ENCODER_AVERAGING_PULSES	max 'N' = 8 (ie 2**N Pulses)
CORACQ_PRM_SHAFT_ENCODER_AVERAGING_PERIOD_MIN	50 nsec
CORACQ_PRM_SHAFT_ENCODER_AVERAGING_PERIOD_MAX	2000000 nsec
CORACQ_PRM_HDR_ENABLE	Not Available

## ACQ Related Parameters

Table 11: Acquisition Related Parameters

Parameter	Values
CORACQ_PRM_LABEL	Mono CXP Mono RGB CXP Color RGB
CORACQ_PRM_EVENT_TYPE	CORACQ_VAL_EVENT_TYPE_START_OF_FRAME CORACQ_VAL_EVENT_TYPE_END_OF_FRAME CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC CORACQ_VAL_EVENT_TYPE_FRAME_LOST CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED CORACQ_VAL_EVENT_TYPE_EXT_LINE_TRIGGER_TOO_SLOW CORACQ_VAL_EVENT_TYPE_LINK_ERROR CORACQ_VAL_EVENT_TYPE_SHAFT_ENCODER_REVERSE_COUNT_OVERFLOW CORACQ_VAL_EVENT_TYPE_LINE_TRIGGER_TOO_FAST CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_END



Parameter		Values
CORACQ_PRM_EVENT_TYPE_EX		CORACQ_VAL_EVENT_TYPE_START_OF_FRAME CORACQ_VAL_EVENT_TYPE_END_OF_FRAME CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC CORACQ_VAL_EVENT_TYPE_FRAME_LOST CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED CORACQ_VAL_EVENT_TYPE_EXT_LINE_TRIGGER_TOO_SLOW CORACQ_VAL_EVENT_TYPE_LINK_ERROR CORACQ_VAL_EVENT_TYPE_SHAFT_ENCODER_REVERSE_COUNT_OVERFLOW CORACQ_VAL_EVENT_TYPE_LINE_TRIGGER_TOO_FAST CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_END CORACQ_VAL_EVENT_TYPE_LINK_LOCK CORACQ_VAL_EVENT_TYPE_LINK_UNLOCK CORACQ_VAL_EVENT_TYPE_CAMERA_MISSED_TRIGGER
CORACQ_PRM_SIGNAL_STATUS		CORACQ_VAL_SIGNAL_HSYNC_PRESENT CORACQ_VAL_SIGNAL_VSYNC_PRESENT CORACQ_VAL_SIGNAL_POWER_PRESENT CORACQ_VAL_SIGNAL_POCP_ACTIVE CORACQ_VAL_SIGNAL_POCP_ACTIVE_2 CORACQ_VAL_SIGNAL_POCP_ACTIVE_3 CORACQ_VAL_SIGNAL_POCP_ACTIVE_4 CORACQ_VAL_SIGNAL_LINK_LOCK CORACQ_VAL_SIGNAL_LANE1_LOCK CORACQ_VAL_SIGNAL_LANE2_LOCK CORACQ_VAL_SIGNAL_LANE3_LOCK CORACQ_VAL_SIGNAL_LANE4_LOCK CORACQ_VAL_SIGNAL_DATA_LANES
CORACQ_PRM_FLAT_FIELD_ENABLE	Mono RGB Bayer	TRUE / FALSE Not available
CORACQ_CAP_FLAT_FIELD_OFFSET	8-bit Mono 10-bit Mono 12-bit Mono 14-bit Mono 16-bit Mono	min = 0 max = 255 step = 1 min = 0 max = 1023 step = 1 min = 0 max = 4095 step = 1 min = 0 max = 16383 step = 1 Not Available
CORACQ_CAP_FLAT_FIELD_GAIN	8-bit Mono 10-bit Mono 12-bit Mono 14-bit Mono 16-bit Mono	min = 0 max = 255 step = 1 min = 0 max = 1023 step = 1 min = 0 max = 4095 step = 1 min = 0 max = 16383 step = 1 Not Available
CORACQ_CAP_FLAT_FIELD_GAIN_DIVISOR	8-bit Mono 10-bit Mono 12-bit Mono 14-bit Mono 16-bit Mono	0x80 0x200 0x800 0x2000 Not Available
CORACQ_PRM_FLAT_FIELD_PIXEL_REPLACEMENT_METHOD		CORACQ_VAL_FLAT_FIELD_PIXEL_REPLACEMENT_METHOD_2 (Pixel replacement is done by averaging the 2 neighborhood pixels. When one of the neighbors is not available (border image pixels, the pixel is simply replaced with the available neighbor)

Parameter	Values
CORACQ_PRM_FLAT_FIELD_SET_SELECT	min = 0 max = 16 step = 1
CORACQ_PRM_TIME_STAMP	Available
CORACQ_PRM_IMAGE_FILTER_ENABLE	Not Available
CORACQ_PRM_SHAFT_ENCODER_REVERSE_COUNT	Max = 65536 ticks
CORACQ_PRM_META_DATA	CORACQ_VAL_META_DATA_PER_LINE_RIGHT (0x2)
CORACQ_PRM_SHAFT_ENCODER_STATUS	CORACQ_VAL_SHAFT_ENCODER_STATUS_DIRECTION_FORWARD / CORACQ_VAL_SHAFT_ENCODER_STATUS_DIRECTION_REVERSE (0x1) CORACQ_VAL_SHAFT_ENCODER_STATUS_TOO_SLOW (0x2) CORACQ_VAL_SHAFT_ENCODER_STATUS_REVERSE_COUNT_OVERFLOW (0x4)
CORACQ_PRM_SHAFT_ENCODER_COUNT	Available
CORACQ_PRM_META_DATA_CLEAR	Available

## Transfer Related Capabilities

Table 12: Transfer Related Capabilities

Capability	Values
CORXFER_CAP_NB_INT_BUFFERS	CORXFER_VAL_NB_INT_BUFFERS_AUTO (0x2)
CORXFER_CAP_MAX_XFER_SIZE	4294967040 Bytes
CORXFER_CAP_MAX_FRAME_COUNT	16777215 Frames
CORXFER_CAP_COUNTER_STAMP_AVAILABLE	FALSE
CORXFER_CAP_TRANSFER_SYNC	CORXFER_VAL_TRANSFER_SYNC_SUPPORTED (0x1)

## Transfer Related Parameters

Table 13: Transfer Related Parameters

Parameter	Values
CORXFER_PRM_EVENT_TYPE CORXFER_PRM_EVENT_TYPE_EX	CORXFER_VAL_EVENT_TYPE_START_OF_FRAME CORXFER_VAL_EVENT_TYPE_END_OF_FRAME CORXFER_VAL_EVENT_TYPE_END_OF_LINE CORXFER_VAL_EVENT_TYPE_END_OF_NLINES CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER
CORXFER_PRM_START_MODE	CORXFER_VAL_START_MODE_ASYNCHRONOUS (0x0) CORXFER_VAL_START_MODE_SYNCHRONOUS (0x1) CORXFER_VAL_START_MODE_HALF_ASYNCHRONOUS (0x2) CORXFER_VAL_START_MODE_SEQUENTIAL (0x3)
CORXFER_PRM_CYCLE_MODE	CORXFER_VAL_CYCLE_MODE_ASYNCHRONOUS (0x0) CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_WITH_TRASH (0x2) CORXFER_VAL_CYCLE_MODE_OFF (0x3) CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_NEXT_EMPTY_WITH_TRASH (0x5)
CORXFER_PRM_FLIP	CORXFER_VAL_FLIP_OFF (0x0) CORXFER_VAL_FLIP_VERT (0x2)
CORXFER_PRM_INT_BUFFERS	* Depends on acquired image size. By default driver will optimize the number of on-board buffers.
CORXFER_PRM_EVENT_COUNT_SOURCE	CORXFER_VAL_EVENT_COUNT_SOURCE_DST (0x1) CORXFER_VAL_EVENT_COUNT_SOURCE_SRC (0x2)
CORXFER_PRM_BUFFER_TIMESTAMP_MODULE	CORXFER_VAL_BUFFER_TIMESTAMP_MODULE_ACQ (0x1) CORXFER_VAL_BUFFER_TIMESTAMP_MODULE_XFER (0x13)
CORXFER_PRM_BUFFER_TIMESTAMP_EVENT (ACQ Related)	CORACQ_VAL_EVENT_TYPE_START_OF_FRAME (0x80000) CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER (0x1000000)
CORXFER_PRM_BUFFER_TIMESTAMP_EVENT (XFER Related)	CORXFER_VAL_EVENT_TYPE_END_OF_FRAME (0x800000)
CORXFER_PRM_LINE_MERGING	CORXFER_VAL_LINE_MERGING_AUTO (0x0) CORXFER_VAL_LINE_MERGING_OFF (0x2)

## General Outputs #1: Related Capabilities (for GIO Module #0)

Outputs available on connector J7 and J8.

Table 14: GIO-0 Related Capabilities

Capability	Values
CORGIO_CAP_IO_COUNT	8 I/Os
CORGIO_CAP_DIR_OUTPUT	0xff
CORGIO_CAP_DIR_TRISTATE	0xff
CORGIO_CAP_EVENT_TYPE	Not Available
CORGIO_CAP_READ_ONLY	0x01 (* depends on strobe outputs reserved for acquisition device)

## General Outputs #1: Related Parameters (for GIO Module #0)

Table 15: GIO-0 Related Parameters

Parameter	Values
CORGIO_PRM_LABEL	General Outputs #1
CORGIO_PRM_DEVICE_ID	0
CORGIO_PRM_OUTPUT_TYPE	CORGIO_VAL_OUTPUT_TYPE_LVTTL (0x20)
CORGIO_PRM_CONNECTOR	CORGIO_VAL_CONNECTOR_1 (0x1)

## General Inputs #1: Related Capabilities (for GIO Module #1)

Inputs available on connector J7 and J8.

Table 16: GIO-1 Related Capabilities

Capability	Values
CORGIO_CAP_IO_COUNT	4 I/Os
CORGIO_CAP_DIR_OUTPUT	0x0
CORGIO_CAP_DIR_TRISTATE	0x0
CORGIO_CAP_EVENT_TYPE	CORGIO_VAL_EVENT_TYPE_RISING_EDGE (0x1) CORGIO_VAL_EVENT_TYPE_FALLING_EDGE (0x2)
CORGIO_CAP_READ_ONLY	0x03 (* depends on external trigger inputs reserved for acquisition device)

## General Inputs #1: Related Parameters (for GIO Module #1)

Table 17: GIO-1 Related Parameters

Parameter	Values
CORGIO_PRM_LABEL	General Inputs #1
CORGIO_PRM_DEVICE_ID	1
CORGIO_PRM_INPUT_LEVEL	CORGIO_VAL_INPUT_LEVEL_TTL (0x1) CORGIO_VAL_INPUT_LEVEL_422 (0x2) CORGIO_VAL_INPUT_LEVEL_24VOLTS (0x8) CORGIO_VAL_INPUT_LEVEL_12VOLTS (0x40)
CORGIO_PRM_CONNECTOR	CORGIO_VAL_CONNECTOR_1 (0x1)

## Bidirectional General I/Os: Related Capabilities (for GIO Module #2)

These I/Os are available on connector J9

Table 18: GIO-1 Related Parameters

Capability	Values
CORGIO_CAP_IO_COUNT	8 I/Os
CORGIO_CAP_DIR_OUTPUT	0xff
CORGIO_CAP_DIR_TRISTATE	0xff
CORGIO_CAP_EVENT_TYPE	Not Available
CORGIO_CAP_READ_ONLY	0x03 (* depends on board syncs reserved for acquisition device)

## Bidirectional General I/Os: Related Parameters (for GIO Module #2)

Table 19: GIO-2 Related Parameters

Parameter	Values
CORGIO_PRM_LABEL	Bidirectional General I/Os #1
CORGIO_PRM_DEVICE_ID	2
CORGIO_PRM_OUTPUT_TYPE	CORGIO_VAL_OUTPUT_TYPE_LVTTL (0x20)
CORGIO_PRM_INPUT_LEVEL	CORGIO_VAL_INPUT_LEVEL_LVTTL (0x20)
CORGIO_PRM_CONNECTOR	CORGIO_VAL_CONNECTOR_2 (0x2)

# Sapera Servers and Resources

A Sapera Server is an abstract representation of a physical device like a frame-grabber or camera. When using the SapAcquisition or SapAcqDevice constructors, the location parameter specifies the server to use to create the object. Use the Sapera Configuration utility to find the names and indices of all Sapera servers in your system.

In Sapera LT all frame grabbers are configured using the SapAcquisition class. All CXP cameras are GenCP compliant and are configured in Sapera LT using the SapAcqDevice class.



**Note:** Currently, CXP cameras do not have their own server, therefore it is available under the Xtium\_CXP server. For example, in CamExpert the Xtium server displays both the frame grabber and camera resources.

## The following table describes the Xtium2-CXP PX8 board

Table 20: Xtium2-CXP PX8 - Servers and Resources

Servers		Resources		
Name	Type	Name	Index	Description
Xtium2-CXP_PX8_1 (1 Camera)	Acquisition Module	CXP Mono #1	0	CXP Mono Camera
		CXP Color RGB #1	1	CXP RGB Camera
		CXP Bayer #1	2	CXP Bayer Camera
	Acquisition Device	<Device Name> [SN: <Serial Number>] *Name of camera	0	CXP Camera connected to respective Camera #
Xtium2-CXP_PX8_1 (2 Cameras)	Acquisition Module	CXP Mono #1	0	CXP Mono Camera
		CXP Mono #2	1	
		CXP Color RGB #1	2	CXP RGB Camera
		CXP Color RGB #2	3	
		CXP Bayer #1	4	CXP Bayer Camera
		CXP Bayer #2	5	
	Acquisition Device	<Device Name> [SN: <Serial Number>] *Name of camera	0 1	CXP Camera connected to respective Camera #
Xtium2-CXP_PX8_1 (3 Cameras)	Acquisition Module	CXP Mono #1	0	CXP Mono Camera
		CXP Mono #2	1	
		CXP Mono #3	2	
		CXP Color RGB #1	3	CXP RGB Camera
		CXP Color RGB #2	4	
		CXP Color RGB #3	5	
		CXP Bayer #1	6	CXP Bayer Camera
		CXP Bayer #2	7	
		CXP Bayer #3	8	
	Acquisition Device	<Device Name> [SN: <Serial Number>] *Name of camera	0 1 2	CXP Camera connected to respective Camera #

Servers	Resources			
Name	Type	Name	Index	Description
Xtium2-CXP_PX8_1 (4 Cameras)	Acquisition Module	CXP Mono #1	0	CXP Mono Camera
		CXP Mono #2	1	
		CXP Mono #3	2	
		CXP Mono #4	3	
		CXP Color RGB #1	4	CXP RGB Camera
		CXP Color RGB #2	5	
		CXP Color RGB #3	6	
		CXP Color RGB #4	7	
		CXP Bayer #1	8	CXP Bayer Camera
		CXP Bayer #2	9	
		CXP Bayer #3	10	
	CXP Bayer #4	11		
	Acquisition Device	<Device Name>	0	CXP Camera connected to respective Camera #
		[SN: <Serial Number>]	1	
		*Name of camera	2	
		3		
All	GIO Module	General Outputs #1	0	8 General Outputs
		General Inputs #1	1	4 General Inputs
		Bidirectional General I/Os #1	2	8 Bidirectional General I/Os

# Technical Specifications

## Xtium2-CXP PX8 Board Specifications

### Digital Video Input & Controls

Table 21: Board Specifications

<b>Input Type</b>	CoaXPress Specifications Rev 2.0 and 1.x compatible
<b>Common Pixel Formats</b>	8, 10, 12, 14 and 16-bit mono, 8, 10 and 12-bit RGB and Bayer
<b>Scanning</b>	Area scan and Line scan
<b>Resolution</b>  <i>note: these are Xtium2-CXP PX8 maximums, not CoaXPress specifications</i>	Horizontal Minimum: 32 pixels per lane  Horizontal Maximum: 64kBs/line (Mono or Color)  Vertical Minimum: 1 line  Vertical Maximum: up to 65536 lines—for area scan sensors infinite line count—for line scan sensors
<b>Bit Transfer Rate</b>	1.250 Gbps, 2.500 Gbps, 3.125 Gbps, 5.000 Gbps, 6.250 Gbps, 10 Gbps and 12.5 Gbps
<b>Image Buffer</b>	Available with 2 GB
<b>Bandwidth to Host System</b>	Approximately 6.8 GB/s (maximum obtained is dependent on firmware loaded and PC characteristics)
<b>Controls</b>	Compliant with Teledyne DALSA Trigger-to-Image Reliability framework Comprehensive event notifications Timing control logic for camera triggers and strobe signals 4 opto-coupled general inputs where 2 are shared acquisition trigger inputs (RS-422/TTL/12V/24V) Trigger inputs are programmable as active high or low (edge or level trigger, at maximum input frequency of 100 KHz) External trigger latency less than 100 nsec 8 LVTTTL general Outputs where 1 is shared as Strobe Output Quadrature (phase A & B) shaft encoder inputs for external web synchronization: TTL or RS-422 input (mutually exclusive) maximum frequency is 5 MHz Supports multi-camera synchronization of 2 to 4 boards I/O available on a DH60-27P connector (J7) and on 40-pin TST-120-01-G-D (J8)
<b>Processing</b>  <i>Dependent on user loaded firmware configuration</i>	Output Lookup Table Flat Field/Flat Line Correction Bayer Mosaic Filter

---

# Host System Requirements

## Xtium2-CXP PX8 Dimensions

Approximately 6.5 in. (14 cm) wide by 4 in. (10 cm) high

## General System Requirements for the Xtium2-CXP PX8

- PCI Express Gen3 x8 slot compatible;  
(will work in Gen1 or Gen2 x8 slot with reduced bandwidth to host)
- On some computers the Xtium2-CXP PX8 may function installed in a x16 slot. The computer documentation or direct testing by the user is required.
- Xtium2-CXP PX8 operates correctly when installed in a multi-processor system (including Hyper-Threading multi-core processors).

## Operating System Support

Windows 10, in either 32-bit or 64-bit, and Windows 11 64-bit.

## Environment

Table 22: Environment Specifications

<b>Ambient Temperature</b>	10° to 50°C (operation) -40° to 75°C (storage)
<b>Relative Humidity</b>	5% to 90% non-condensing (operating) 0% to 95% (storage)
<b>MTBF @40°C</b>	62 years



Note: Ensure adequate airflow for proper functioning of the board across the entire temperature range of 10 – 50°C. We recommend airflow measuring 80 LFM (linear feet per minute) across the surface of the board.

## Power Requirements while grabbing

Table 23: Power Specifications

+3.3 Vdc	10 W
+12 Vdc	13 W



---

# EMC Declarations of Conformity

Copies of the Declarations of Conformity documents are available on the product page on the [Teledyne DALSA website](#) or by request.

## FCC Statement of Conformance

This equipment complies with Part 15 of the FCC rules. Operation is subject to the following conditions:

- The product may not cause harmful interference; and
- The product must accept any interference received, including interference that may cause undesired operation.

### ***FCC Class A Product***

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at their expense.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This equipment is intended to be a component of a larger industrial system.

## CE Declaration of Conformity

Teledyne Dalsa declares that this product complies with applicable standards and regulations.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This product is intended to be a component of a larger system and must be installed as per instructions to ensure compliance.

# Connector and Switch Locations

## Xtium2-CXP PX8 Board Layout Drawing

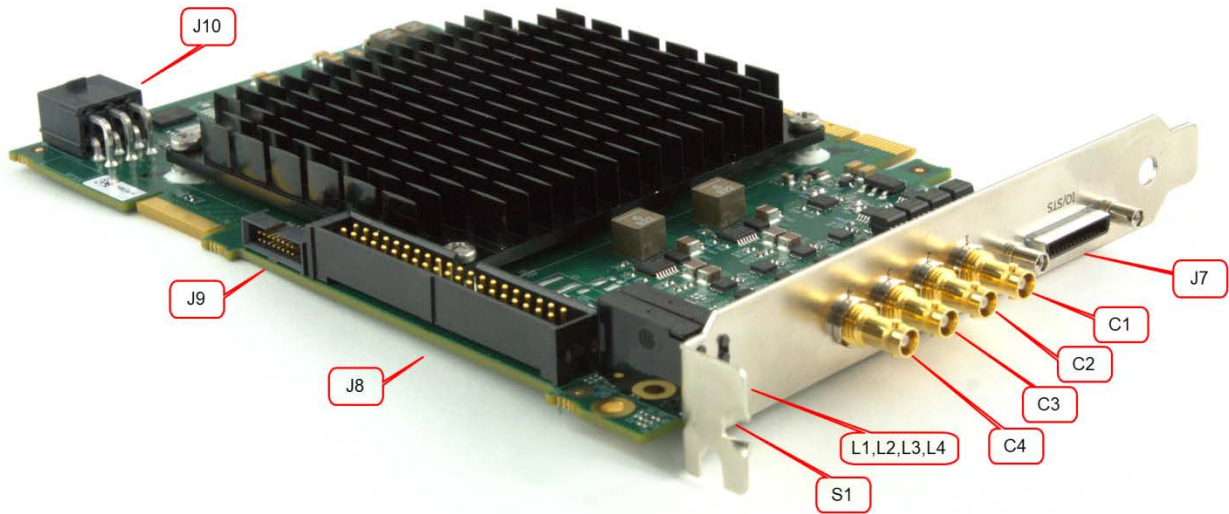


Figure 26: Board Layout

## Connector / LED Description List

The following table lists components on the Xtium2-CXP PX8 board. Detailed information concerning the connectors/LEDs follows this summary table.

Table 24: Board Connector List

Location	Description	Location	Description
<u>J7</u>	External I/O Signals connector (DH60-27P)	<u>J9</u>	Multi Board Sync
<u>S1</u>	Boot-up/PCIe Status LED (refer to text)	<u>J10</u>	PC power for PoCXP usage
<u>C1, C2, C3, C4</u>	Camera CXP Input Connectors	P1	PCIe x8 computer bus connector (Gen3 compliant slot preferred)
<u>L1, L2, L3, L4</u>	Camera CXP status LEDs	P2	Reserved
<u>J8</u>	Internal I/O Signals connector (40-pin TST-120-01-G-D)		

---

# Connector and Switch Specifications

## Xtium2-CXP PX8 End Bracket Detail

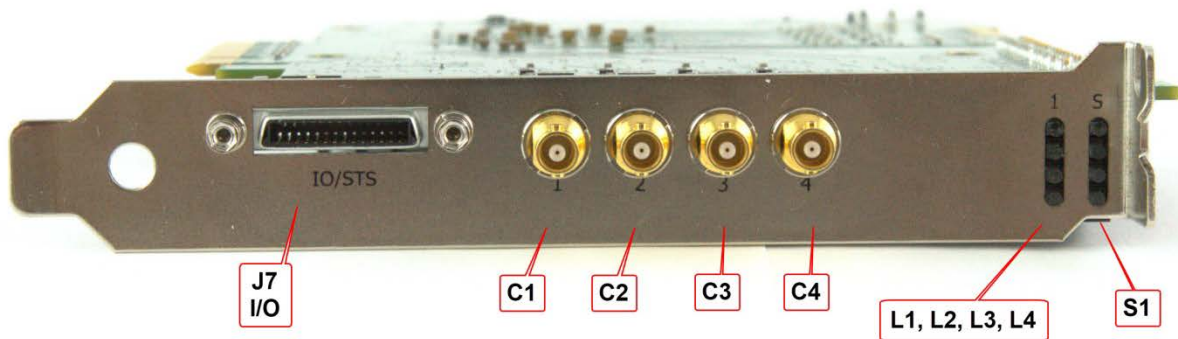


Figure 27: End Bracket Details

The hardware installation process is completed with the connection of a supported camera to the Xtium2-CXP PX8 board using an HDBNC connector (12G models) or DIN 1.0/2.3 connector (6G model). (See the [CoaXPRESS Cables](#) section).

The Xtium2-CXP PX8 board supports up to 4 CoaXPRESS camera outputs.

- **1CH Model**
  - One Camera connection:
    - Connect the camera to the C1 connector.
- **2CH Model**
  - One Camera connection:
    - Connect the camera to the C1 and C2 connectors. The order that the cables are connected to the camera does not matter.
  - Two Camera connection:
    - Connect Camera #1 to C1 and Camera #2 to C2.
- **4CH Model**
  - One Camera connection:
    - Connect the camera to the C1, C2, C3 and C4 connectors. The order that the cables are connected to the camera does not matter.
  - Two Camera connection:
    - Connect Camera #1 to C1/C2 and Camera #2 to C3/C4. The order that the cables are connected to the camera does not matter.
  - Three Camera connection:
    - Connect Camera #1 to C1, Camera #2 to C2 and Camera #3 to C3/C4. The order that the cables are connected to the camera #3 does not matter.
  - Four Camera connection:
    - Connect Camera #1 to C1, Camera #2 to C2, Camera #3 to C3 and Camera #4 to C4.

## Status LEDs Functional Descriptions

LED indicators mounted on the board bracket, provide information on board and connection status as per the tables below.

**S: Boot-up/PCIe Status LED** — Provides general board status information

**L1, L2, L3, L4: CoaXPress status LED** — Indicates status for C1, C2, C3 and C4 respectively.

### S: Boot-up/PCIe Status LED

Table 25: S Boot-up/PCIe Status LED

Color	State	Description
Red	Solid	FPGA firmware not loaded
Green	Solid	Normal FPGA firmware loaded, Gen3 speed, link width x8
Green	Flashing	Normal FPGA firmware loaded, Gen1/Gen2 speed, link width x8
Yellow	Solid	Normal FPGA firmware loaded, Gen3 speed, link width not x8
Yellow	Flashing	Normal FPGA firmware loaded, Gen1/Gen2 speed, link width not x8
Blue	Solid	Safe FPGA firmware loaded, Gen3 speed
Blue	Flashing	Safe FPGA firmware loaded, Gen1/Gen2 speed
Red	Flashing	PCIe Training Issue – Board will not be detected by computer

### L1, L2, L3, L4: CoaXPress Status LED

The Xtium2-CXP PX8 implements the mandatory LED Status indicators as defined by the CoaXPress Specification v1.1.

This LED status table reflects activity on input connectors C1, C2, C3 and C4.

Table 26: Camera CXP Status LED

LED State	Description
Off	No power, driver not started or Backup FPGA running
Slow Pulse Red	Driver running, but nothing connected. Only if PoCXP is disabled
Fast Flashing Green / Orange	Connection detection in progress, PoCXP enabled.
Fast Flashing Orange	Connection detection in progress, PoCXP disabled.
Solid Red	PoCXP over-current
Solid Green	Connected, but no data being transferred
Fast Flashing Green	Connected, data being transferred
Fast Flashing Red	System error: If PoCXP is enabled, 12V is not detected. Make sure PC power is connected to J10.

## J7: External I/O Signals Connector (Female DH60-27P)

Table 27: DH60-27P Connector Signals

Description	Pin #	Pin #	Description
Ground	1	15	External Trigger Input 3/General Input 3 (+)
RS-422 Shaft Encoder Phase A (-)	2	16	External Trigger Input 4/General Input 4 (+)
TTL/RS-422 Shaft Encoder Phase A (+) (see note 3)	3	17	External Trigger Input 4/General Input 4 (-)
Ground	4	18	External Trigger Input 3/General Input 3 (-)
RS-422 Shaft Encoder Phase B (-)	5	19	Power Output 5 Volts, 100 mA max
TTL/RS-422 Shaft Encoder Phase B (+)	6	20	External Trigger Input 2/General Input 2 (-)
External Trigger Input 1/General Input 1 (-)	7	21	Strobe 3 / General Output 3
External Trigger Input 1/General Input 1 (+)	8	22	Strobe 4 / General Output 4
External Trigger Input 2/General Input 2 (+)	9	23	General Output 5
Ground	10	24	General Output 6
Strobe 1 / General Output 1 (See note 2)	11	25	General Output 7
Strobe 2 / General Output 2	12	26	General Output 8
Ground	13	27	NC
Power Output 12 Volts, 350 mA max	14		

## J8: Internal I/O Signals Connector (40-pin TST-120-01-G-D)



**Warning:** J7 and J8 have the same signal assignments. Signals are routed to both connectors directly from their internal circuitry. Therefore, never connect both J7 and J8 to external devices at the same time.

Table 28: 40-pin TST-120-01-G-D Connector Signals

Description	Pin #	Pin #	Description
Power Output 5 Volts, 100mA max	1	21	External Trigger Input 1/General Input 1 (+)
Power Output 12 Volts, 350mA max	2	22	External Trigger Input 1/General Input 1 (-)
Ground	3	23	External Trigger Input 2/General Input 2 (+)
Ground	4	24	External Trigger Input 2/General Input 2 (-)
TTL/RS-422 Shaft Encoder Phase A (+) (see note 3)	5	25	External Trigger Input 3/General Input 3 (+)
RS-422 Shaft Encoder Phase A (-)	6	26	External Trigger Input 3/General Input 3 (-)
TTL/RS-422 Shaft Encoder Phase B (+)	7	27	External Trigger Input 4/General Input 4 (+)
RS-422 Shaft Encoder Phase B (-)	8	28	External Trigger Input 4/General Input 4 (-)
Ground	9	29	Reserved
Ground	10	30	Reserved
Strobe 1 / General Output 1 (See note 2)	11	31	Reserved
Strobe 2 / General Output 2	12	32	Reserved
Strobe 3 / General Output 3	13	33	Reserved
Strobe 4 / General Output 4	14	34	Reserved
General Output 5	15	35	Reserved
General Output 6	16	36	Reserved
General Output 7	17	37	Reserved
General Output 8	18	38	Ground
Ground	19	39	Ground
Ground	20	40	Ground

## Note 1: General Inputs / External Trigger Inputs Specifications

Each of the four General Inputs are opto-coupled and able to connect to differential or single ended source signals. General Inputs can also act as External Trigger Inputs. See “Board Information” user settings. The inputs generate individual interrupts, which are read by the Sopera application. The following figure is typical for each Genera Input.

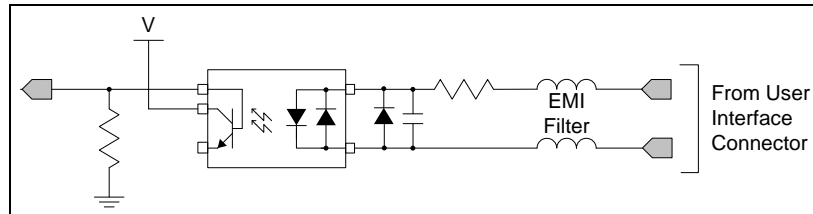


Figure 28: General Inputs Electrical Diagram

### Input Details:

- Maximum input voltage is 26V.
- Maximum input signal frequency is 100 KHz.
- Each input has a 649-ohm series resistor on the opto-coupler input.
- The 0.01uF capacitor provides high frequency noise filtering.
- Minimum current is dependent on input voltage applied:  $I_{optoin(min)} = (V_{optoin} - 0.5)/649\Omega$
- The switch point is software programmable to support differential RS-422 or single ended TTL, 12V or 24V input signals.

### For External Trigger usage:

- Input signal is “debounced” to ensure that no voltage glitch is detected as a valid transition. This debounce circuit time constant can be programmed from 1 $\mu$ s to 255 $\mu$ s. Any pulse smaller than the programmed value is blocked and therefore not seen by the board. If no debounce value is specified (value of 0 $\mu$ s), the minimum value of 1 $\mu$ s will be used.
- Refer to Sopera parameters:  
CORACQ\_PRM\_EXT\_TRIGGER\_SOURCE  
CORACQ\_PRM\_EXT\_TRIGGER\_ENABLE  
CORACQ\_PRM\_EXT\_TRIGGER\_LEVEL  
CORACQ\_PRM\_EXT\_FRAME\_TRIGGER\_LEVEL  
CORACQ\_PRM\_EXT\_TRIGGER\_DETECTION  
CORACQ\_PRM\_EXT\_TRIGGER\_DURATION
- See also \*.cvi file entries:  
External Trigger Level, External Frame Trigger Level, External Trigger Enable and External Trigger Detection.
- External Trigger Input 2 used for two pulse external trigger with variable frame length line scan acquisitions.

## Trigger Signal Total Delay

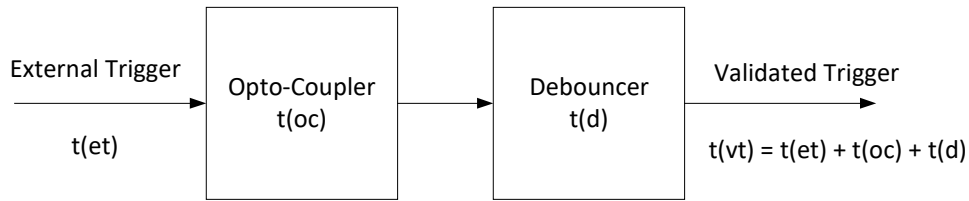


Figure 29: External Trigger Input Validation & Delay

Table 29: External Trigger Timing Specifications

Let	$t(et)$ = time of external trigger in $\mu s$
	$t(oc)$ = time opto-coupler takes to change state (time varies dependent on input voltage)
	$t(d)$ = user set debounce duration from 1 to 255 $\mu s$
	$t(vt)$ = time of validated trigger in $\mu s$



**Note:** Teledyne DALSA recommends using the fastest transition to minimize the time it takes for the opto-coupler to change state.

If the duration of the external trigger is  $> t(oc) + t(d)$ , then a valid acquisition trigger is detected.

It is possible to emulate an external trigger using the software trigger that is generated by a function call from an application.

Table 30: Input Switching Points and Propagation Delay

Trigger Level	Switch Point	Propagation Delay $t(oc)$ (rising edge signal $\uparrow$ )	Propagation Delay $t(oc)$ (falling edge signal $\downarrow$ )
RS-422	1.6V	1.75 $\mu s$	5.5 $\mu s$
TTL	1.6V	1.75 $\mu s$	5.5 $\mu s$
12V	6V	2.6 $\mu s$	2.6 $\mu s$
24V	12V	1.9 $\mu s$	3.1 $\mu s$



# Block Diagram: Connecting External Drivers to General Inputs

Using J7

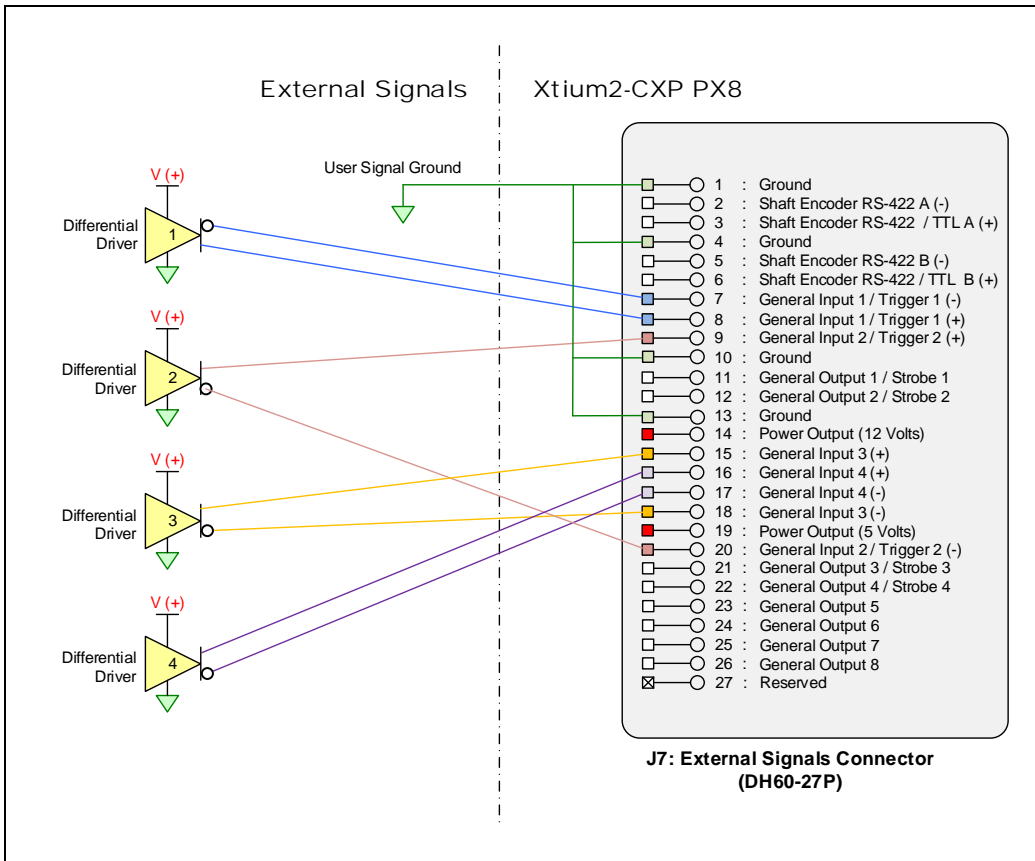


Figure 30: External Signals to J7 Connection Diagram

## Using J8

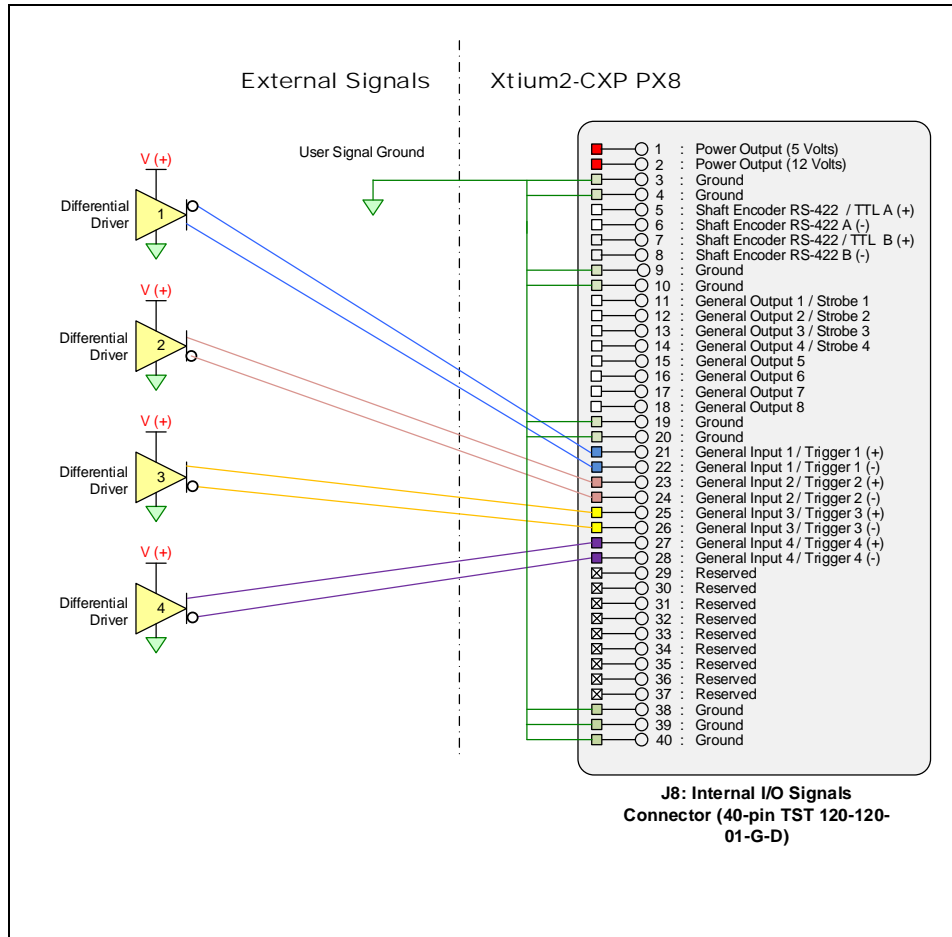


Figure 31: External Signals to J8 Connection Diagram

## External Driver Electrical Requirements

The Xtium2-CXP allows user selected (software programmable) input switching points to support differential (RS-422) input signals and single ended (TTL, 12V or 24V) input signals. The following table defines the external signal voltage requirements from the driver circuits connected to the Xtium external inputs.

Table 31: External Driver Electrical Requirements

Input Level	Description	MIN	MAX
RS-422	Input Voltage High ( $V_{IH}$ )	2.4 V	13.0 V
	Input Voltage Low ( $V_{IL}$ )	-2.4 V	-13.0 V
TTL	Input Voltage High ( $V_{IH}$ )	2.4 V	5.5 V
	Input Voltage Low ( $V_{IL}$ )	0 V	0.8 V
12V	Input Voltage High ( $V_{IH}$ )	9 V	13.2 V
	Input Voltage Low ( $V_{IL}$ )	0 V	3 V
24V	Input Voltage High ( $V_{IH}$ )	18 V	26.4 V
	Input Voltage Low ( $V_{IL}$ )	0 V	6 V

## Note 2: General Outputs /Strobe Output Specifications

Each of the eight General Outputs is TTL (3.3V) compatible. General Outputs 1, 2, 3 and 4 can also function as the Strobe Output controlled by Sopera strobe control functions. See “Board Information” user settings. The following figure is typical for each General Output.

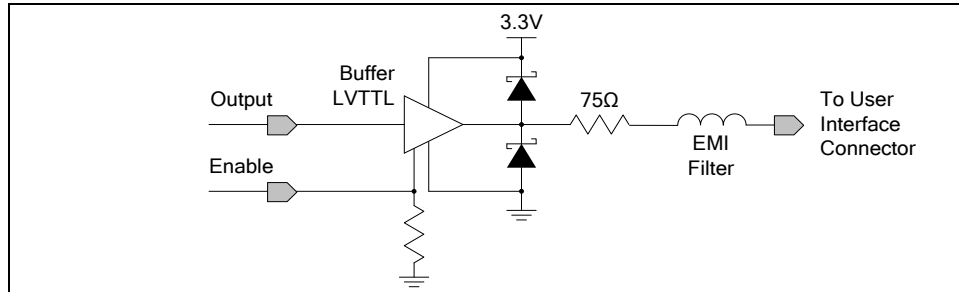


Figure 32: General Outputs Electrical Diagram

### Output Details:

- Each output has a 75-ohm series resistor
- The 2 diodes protect the LVTTL buffer against overvoltage
- Each output is a tristate driver, enabled by software
- Minimum guaranteed output current is +/- 24mA @ 3.3V
- Maximum output current is 50mA
- Maximum short circuit output current is 44mA
- Minimum voltage for output level high is 2.4V, while maximum voltage for output low is 0.55V
- Maximum output switching frequency is limited by driver and register access on the PCIe bus.

### For Strobe Usage:

- Refer to Sopera Strobe Methods parameters:  
CORACQ\_PRM\_STROBE\_ENABLE  
CORACQ\_PRM\_STROBE\_POLARITY  
CORACQ\_PRM\_STROBE\_LEVEL  
CORACQ\_PRM\_STROBE\_METHOD  
CORACQ\_PRM\_STROBE\_DELAY  
CORACQ\_PRM\_STROBE\_DURATION  
CORACQ\_PRM\_STROBE\_DESTINATION
- See also \*.cvi file entries:  
Strobe Enable, Strobe Polarity, Strobe Level, Strobe Method, Strobe Delay, Strobe Duration.

# Block Diagram: Connecting External Receivers to the General Outputs Using J7

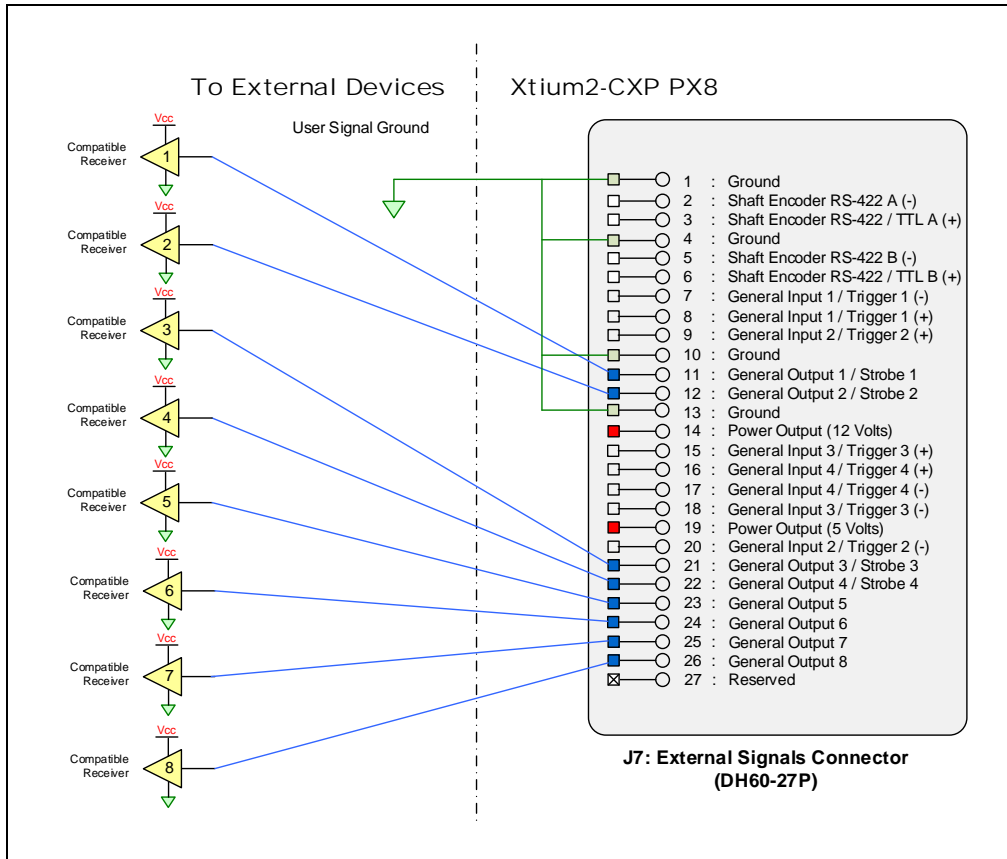


Figure 33: Output Signals to J7 Connection Diagram

## Using J8

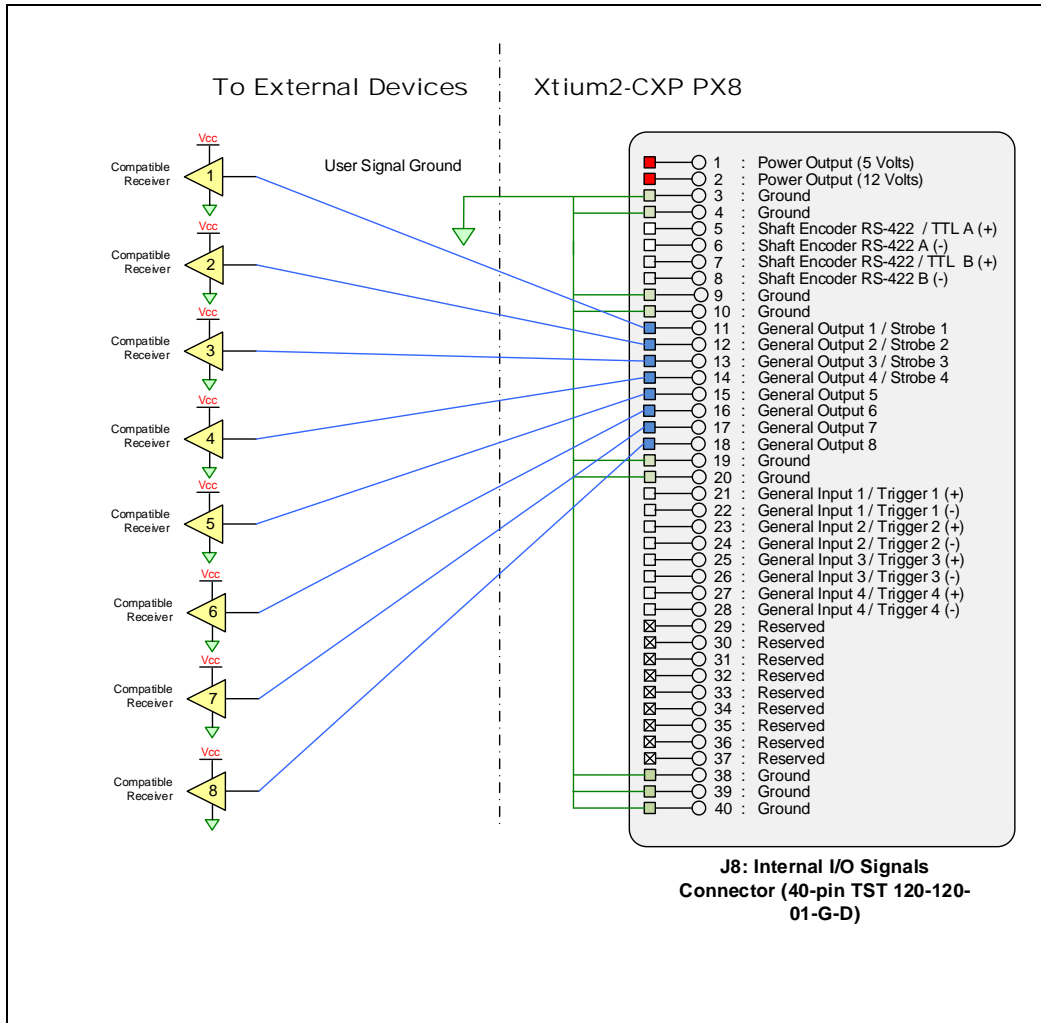


Figure 34: Output Signals to J8 Connection Diagram

### External Receiver Electrical Requirements


- Xtium General Outputs are standard TTL logic levels.
- External receiver circuits must be compatible to TTL signals.

Table 32: External Receiver Electrical Requirements

Xtium2 PX8 Output Level	Description	MIN	MAX
TTL	Output Voltage High ( $V_H$ )	2.0 V	–
	Output Voltage Low ( $V_L$ )	–	0.8 V

### Note 3: RS-422/TTL Shaft Encoder Input Specifications

Dual Quadrature Shaft Encoder Inputs (phase A and phase B) connect to differential signals (RS-422), single ended signals or TTL signals. The figure below shows the simplified representation of these inputs.

	<p><b>WARNING:</b> When using shaft encoders, make sure to connect a common ground between the shaft encoder and frame grabber.</p>
	<p>See <b>RED</b> boxed connections in the diagram below.</p>
	<p>Failure to follow the described instructions could damage the board resulting in the shaft encoder not working properly.</p> <p>Ensure that these grounding measures are followed when migrating from boards with opto-coupled shaft encoders (such as the Xcelera).</p>

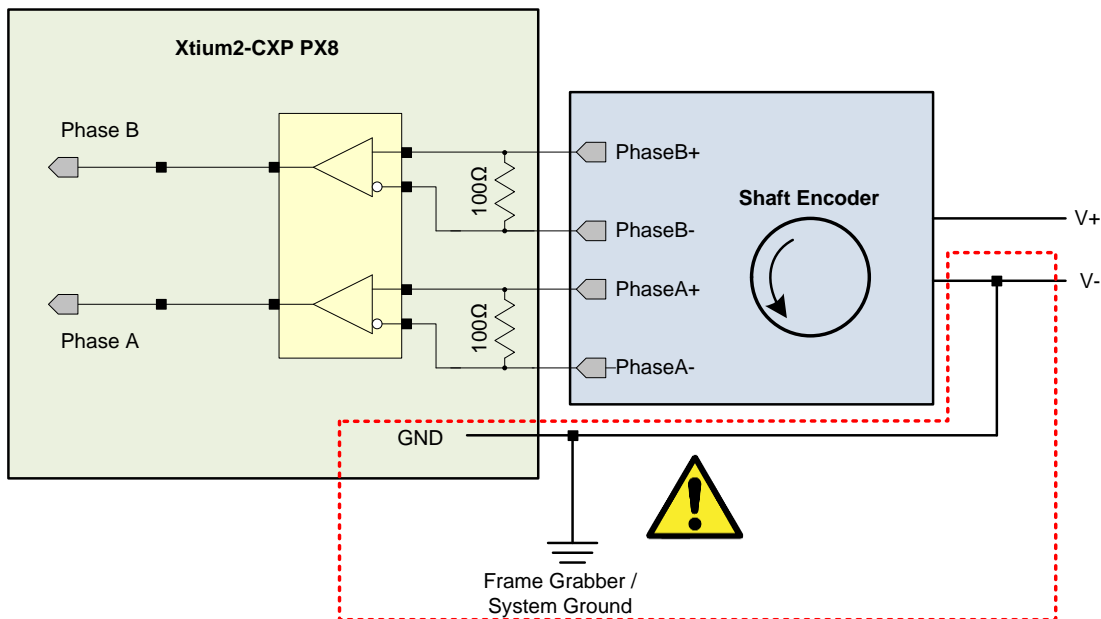


Figure 35: RS-422 Shaft Encoder Input Electrical Diagram

- The shaft encoder ground and the Xtium2-CXP PX8 computer system ground must be connected together.
- RS-422 Input Specifications:
  - Input signals must meet the following
    - Maximum differential input voltage is +/- 7V.
    - Minimum differential voltage level is +/- 200mV.
  - Both inputs have a 100-ohm differential resistor.

- TTL Input Specifications:
  - RS-422 differential line receiver used is am26lv32
  - Input signals must meet the following
    - Input voltage high minimum = 2V
    - Input voltage low maximum = 0.8V
  - Input Current Max = 5mA
- RS-422/TTL differential line receiver used is am26lv32.
- Maximum input signal frequency is 5 MHz.
- The Xtium2-CXP PX8 provides ESD filtering on-board.
- See the [Line Trigger Source Selection for Line scan Applications](#) section for more information.
- Refer to Sopera parameters:
  - [CORACQ\\_PRM\\_SHAFT\\_ENCODER\\_ENABLE](#)
  - [CORACQ\\_PRM\\_SHAFT\\_ENCODER\\_LEVEL](#)
  - [CORACQ\\_PRM\\_SHAFT\\_ENCODER\\_DROP](#)
 or refer to
  - [CORACQ\\_PRM\\_EXT\\_LINE\\_TRIGGER\\_ENABLE](#)
  - [CORACQ\\_PRM\\_EXT\\_LINE\\_TRIGGER\\_DETECTION](#)
  - [CORACQ\\_PRM\\_EXT\\_LINE\\_TRIGGER\\_LEVEL \(RS-422 or TTL\)](#)
  - [CORACQ\\_PRM\\_EXT\\_LINE\\_TRIGGER\\_SOURCE](#)
- See also \*.cvi file entries:
  - Shaft Encoder Enable, Shaft Encoder Pulse Drop,
  - or see External Line Trigger Enable, External Line Trigger Detection, External Line Trigger Level, External Line Trigger Source.
- For TTL signals, connect directly to RS-422/TTL (+) input.
- For single ended signals, connect a bias voltage to the RS-422 (-) input to ensure correct detection of the logic state of the signal connected to the RS-422/TTL (+) input.
- See the following sections for connection methods.

### Note 3.1: Interfacing to an RS-422 Driver Output

Using J7

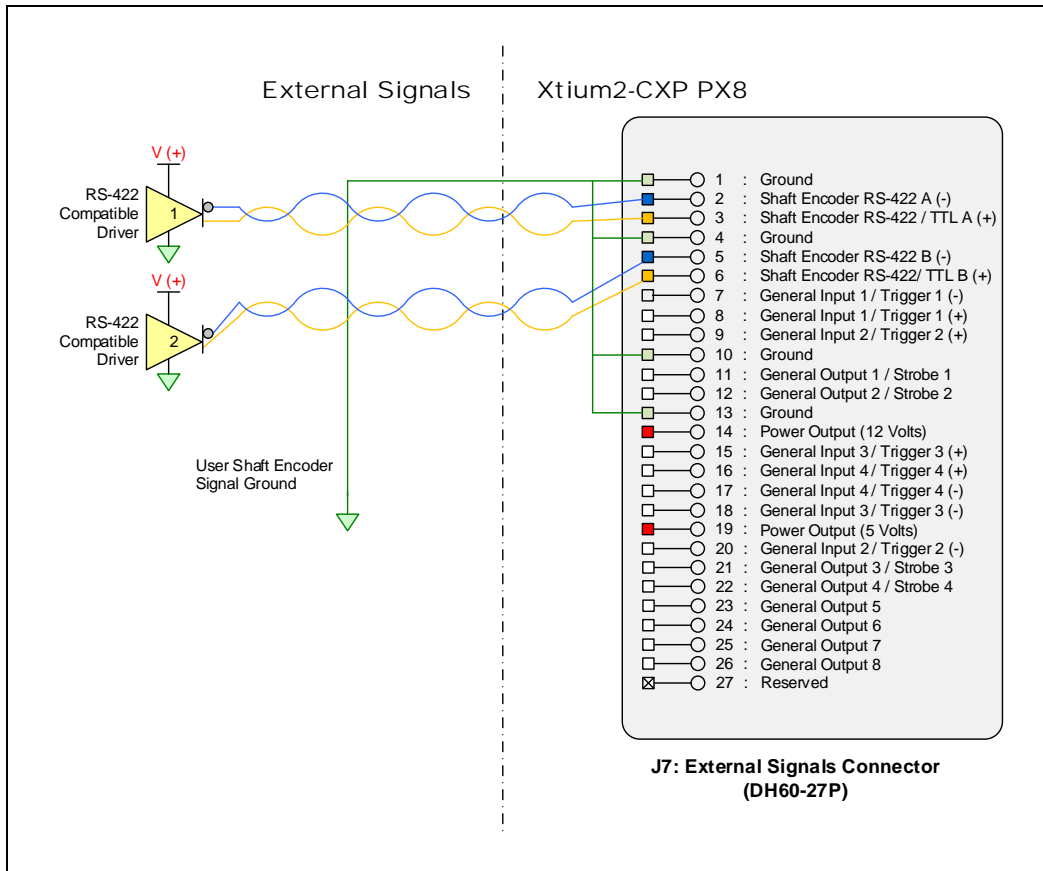


Figure 36: External RS-422 Signals to J7 Connection Diagram



## Using J8

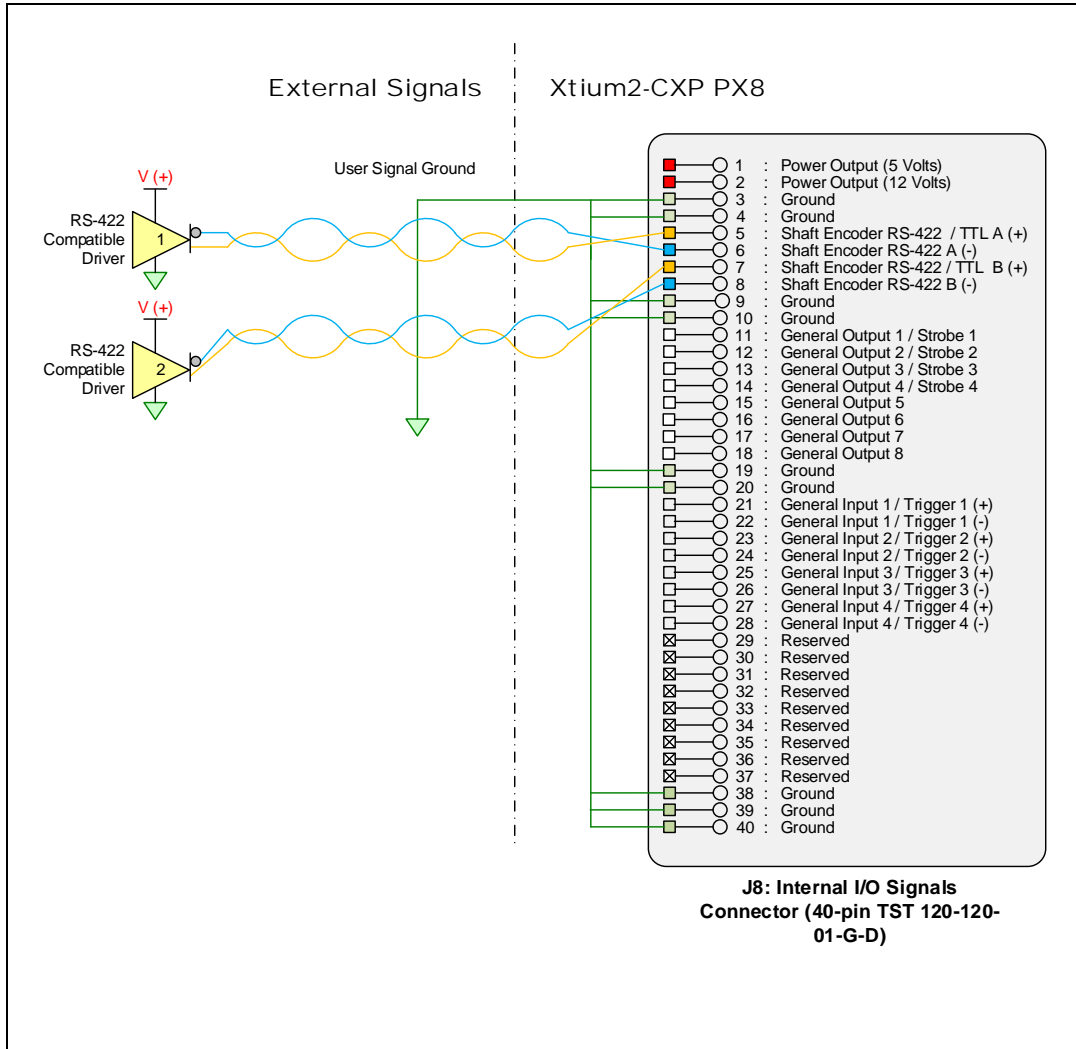


Figure 37: External RS-422 Signals to J8 Connection Diagram

### Note 3.2: Interfacing to a Line Driver (also called Open Emitter) Output

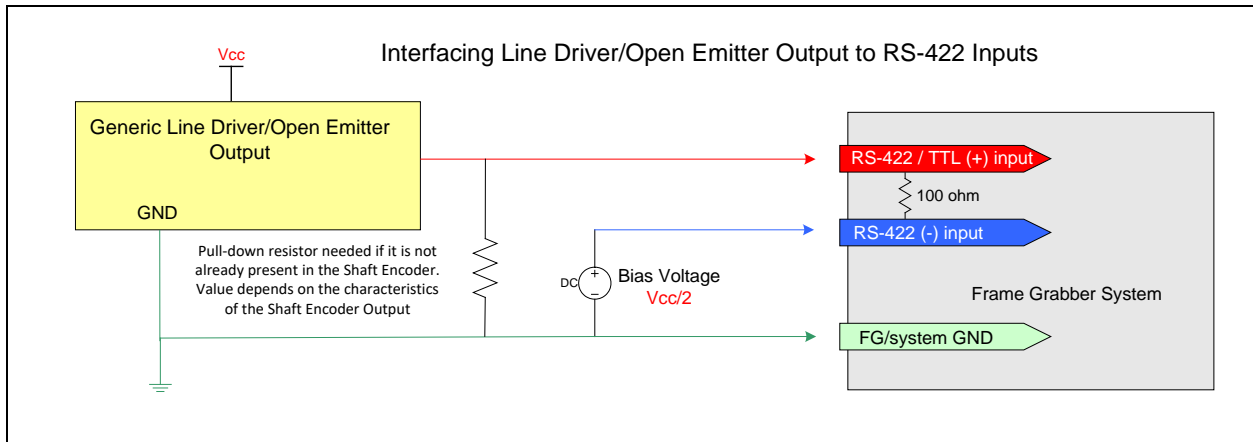


Figure 38: Interfacing to a Line Driver Output

- NOTE: User must select the Shaft Encoder RS-422 level when using this mode (`CORACO_PRM_SHAFT_ENCODER_LEVEL = CORACO_VAL_LEVEL_422 (0x2)`).

### Note 3.3: Interfacing to an Open Collector Output

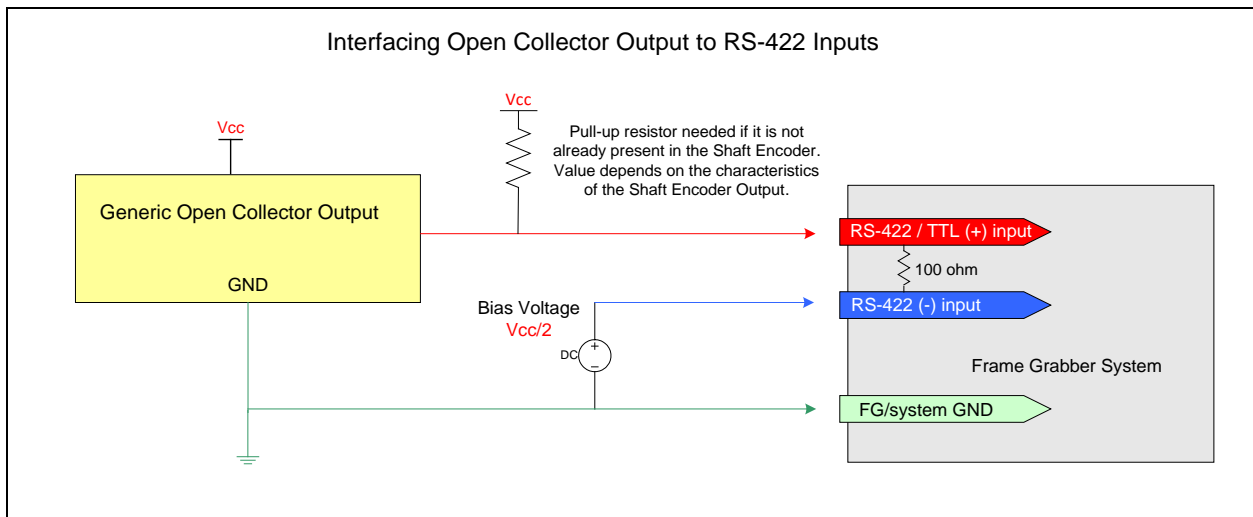


Figure 39: Interfacing to an Open Collector Output

- NOTE: User must select the Shaft Encoder RS-422 level when using this mode (`CORACO_PRM_SHAFT_ENCODER_LEVEL = CORACO_VAL_LEVEL_422 (0x2)`).

### Note 3.4: Interfacing directly to a TTL (also called Push-Pull) Output

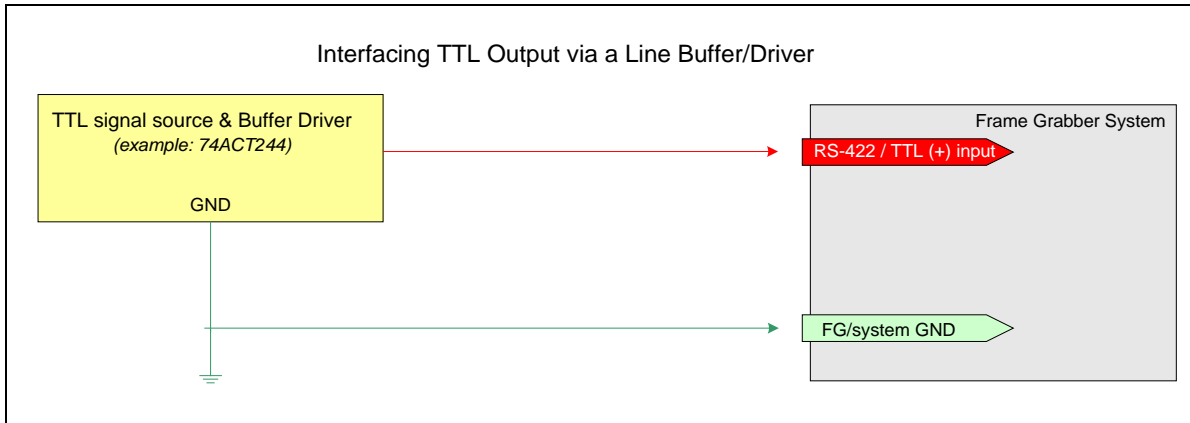


Figure 40: Interfacing TTL to TTL Shaft Encoder Inputs

- NOTE: User must select the Shaft Encoder TTL level when using this mode (`CORACQ_PRM_SHAFT_ENCODER_LEVEL = CORACQ_VAL_LEVEL_TTL (0x1)`).

### Note 3.5: Interfacing to a TTL using a Bias Voltage

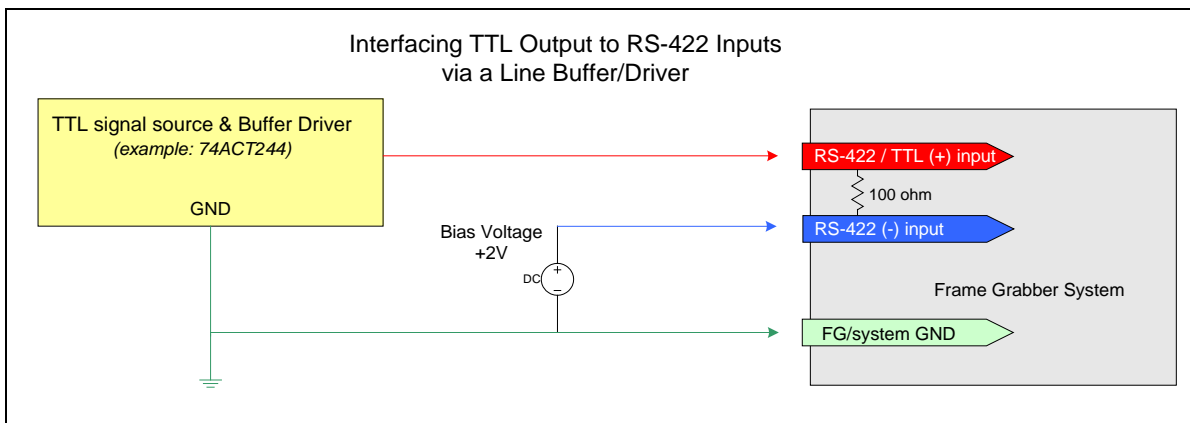


Figure 41: Interfacing TTL to RS-422 Shaft Encoder Inputs using a Bias Voltage

- If necessary, a TTL input can be connected to the RS-422 / TTL input using a bias voltage (however it is recommended to use the Shaft Encoder TTL mode described in [Note 3.4](#). The graphic shows a single-ended driver signal interfaced to the RS-422 input).
- RS-422 (-) input is biased to a DC voltage of +2 volts. This guarantees that the TTL signal connected to the RS-422 / TTL (+) input will be detected as a logic high or low relative to the (-) input.
- The TTL shaft encoder ground, the bias voltage ground, and the Xtium2-CXP PX8 computer system ground must be connected together.
- DC voltage for the RS-422 (-) input can be generated by a resistor voltage divider.
- Use a single battery cell if this is more suitable to your system.
- NOTE: User must select the Shaft Encoder RS-422 level when using this mode (`CORACQ_PRM_SHAFT_ENCODER_LEVEL = CORACQ_VAL_LEVEL_422 (0x2)`).

## C1, C2, C3, C4: CoaXPress Connector



**Note:** The CoaXPress camera connector is defined in the J11A document “CoaXPress Standard” *version 2.0*, ©2019 J11A. Typically, there is no need to be concerned with the physical pinout of the connector or cables that meet the standard.

## J9: Multi-Board Sync / Bi-directional General I/Os

There are 8 bi-directional General I/Os that can be interconnected between multiple boards. These bi-directional I/Os can be read or written by Sapera applications. Bi-directional General I/O no.1 and no.2 also can also act as the multi-board sync I/O.

The multi-board synchronization feature permits interconnecting multiple Xtium boards to synchronize acquisitions to one or two triggers or events. The trigger source origin can be either an external signal or a software control signal. The board sending the trigger(s) is the “Sync Master” board, while the one or more boards receiving the control signal(s) are “Sync Slaves”.

Setup of the boards is done either by setting parameters via a Sapera application or by using CamExpert to configure two camera files (.ccf). For testing purposes, two instances of CamExpert (one for each board) can be run on the system where the frame grabbers are installed.

### Hardware Preparation

- Interconnect two, three, or four Xtium boards via their J9 connector using the OR-YXCC-BSYNC20 cable (for 2 boards) or the OR-YXCC-BSYNC40 cable (see [Board Sync Cable Assembly OR-YXCC-BSYNC40](#) for 3 or 4 boards).



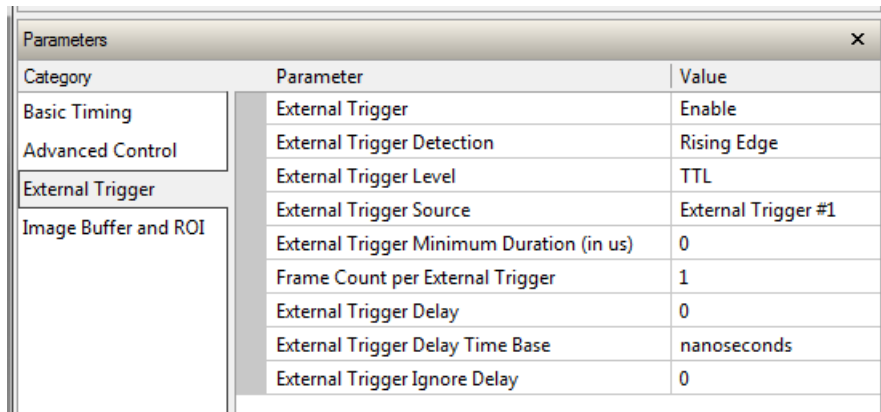
**Warning:** Multi-Board Sync / Bi-directional General I/Os are only for use with Teledyne DALSA frame grabbers within the same PC, otherwise electrical damage to boards can occur.

### Configuration via Sapera Application Programming

- **Sync Master Board** Software Setup: Choose one Xtium as “Sync Master”. The Sapera parameter CORACQ\_PRM\_BOARD\_SYNC\_OUTPUT1\_SOURCE and/or CORACQ\_PRM\_BOARD\_SYNC\_OUTPUT2\_SOURCE select the signal(s) to send to the “Sync Slave” boards.
- Other sync master parameters are set as for any external trigger application, such as External Trigger enable, detection, and level. See Sapera documentation for more details.
- **Sync Slave Board** Software Setup: The Sapera parameter CORACQ\_PRM\_EXT\_TRIGGER\_SOURCE and/or CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_SOURCE are set to Board Sync #1 or #2.

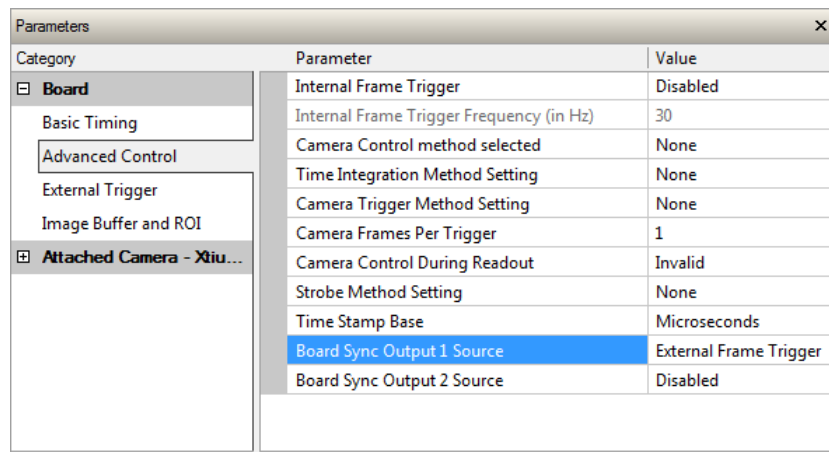
## Configuration via Sopera CamExpert

- Start the first instance of CamExpert and select one installed **Xtium2 board** to be the **sync master**. As shown in the following image, this board is configured to use an external trigger on input #1.



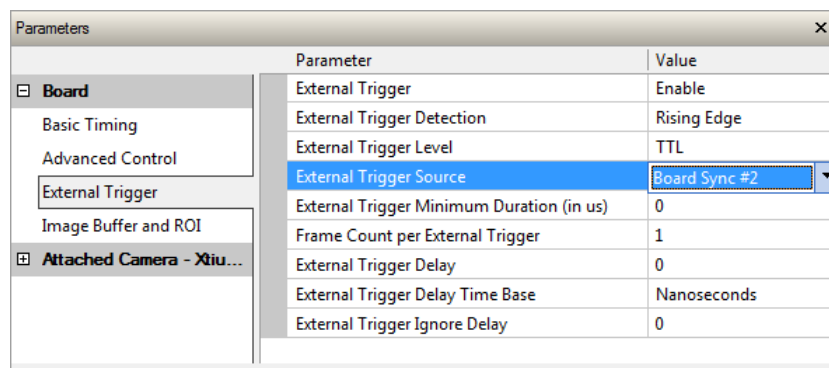
Category	Parameter	Value
Basic Timing	External Trigger	Enable
Advanced Control	External Trigger Detection	Rising Edge
External Trigger	External Trigger Level	TTL
Image Buffer and ROI	External Trigger Source	External Trigger #1
	External Trigger Minimum Duration (in us)	0
	Frame Count per External Trigger	1
	External Trigger Delay	0
	External Trigger Delay Time Base	nanoseconds
	External Trigger Ignore Delay	0

- The **Sync Master Xtium2 board** is also configured to output the external trigger on board sync #1, as shown in the following image.



Category	Parameter	Value
Board	Internal Frame Trigger	Disabled
Basic Timing	Internal Frame Trigger Frequency (in Hz)	30
Advanced Control	Camera Control method selected	None
External Trigger	Time Integration Method Setting	None
Image Buffer and ROI	Camera Trigger Method Setting	None
Attached Camera - Xtium2	Camera Frames Per Trigger	1
	Camera Control During Readout	Invalid
	Strobe Method Setting	None
	Time Stamp Base	Microseconds
	Board Sync Output 1 Source	External Frame Trigger
	Board Sync Output 2 Source	Disabled

- The **Sync Slave Xtium2 board** is configured to receive its trigger on the board sync signal. As an example, the following image shows the Xtium2 board configured for an external sync on board sync #2.



Category	Parameter	Value
Board	External Trigger	Enable
Basic Timing	External Trigger Detection	Rising Edge
Advanced Control	External Trigger Level	TTL
External Trigger	External Trigger Source	Board Sync #2
Image Buffer and ROI	External Trigger Minimum Duration (in us)	0
Attached Camera - Xtium2	Frame Count per External Trigger	1
	External Trigger Delay	0
	External Trigger Delay Time Base	Nanoseconds
	External Trigger Ignore Delay	0

- **Test Setup:** Start the acquisition on all slave boards. The acquisition process is now waiting for the control signal from the master board. Trigger master board acquisition and the acquisition start signal is sent to each slave board.

## J10: Power Connector

### *DC Power Details*



**Warning:** Never remove or install any hardware component with the computer power on. Never connect a power cable to J10 when the computer is powered on.

- Connect a computer 6-pin PCI Express power connector to J10 to supply DC power to the CoaXPress connectors for PoCXP operation. Older computers may need a power cable adapter (see [Power Cable Assembly OR-YXCC-PWRY00](#)).
- The 12 Volt source supplies the 24V (through voltage step-up circuitry) with up to 13W of power for each CXP input as per CoaXPress specifications.

# Cables & Accessories

The following cables and accessories are available for purchase via third party vendors or Teledyne DALSA. Contact sales for information.

## CoaXPress Cables

The Xtium2 CXP frame grabber uses HD-BNC coaxial connectors (camera connectors may vary depending on the camera model). For additional information on cables and their specifications, visit the following web sites:

Table 33: CoaXPress Cable Suppliers

Components Express	<a href="http://www.componentsexpress.com/">http://www.componentsexpress.com/</a>
Samtec	<a href="https://www.samtec.com/">https://www.samtec.com/</a>

## DH40-27S Cable to Blunt End (OR-YXCC-27BE2M1, Rev B1)

Cable assembly consists of a 2000 mm (~6 ft.) blunt end cable to mate to Xtium external connector **J7**. Note: The applicable wiring color-code table is included with the printed Product Notice shipped with the cable package — no other wiring table should be used.

**Important:** The older cable part number OR-YXCC-27BE2M0 (rev.3) is obsolete. Do not use with any Xtium series boards.

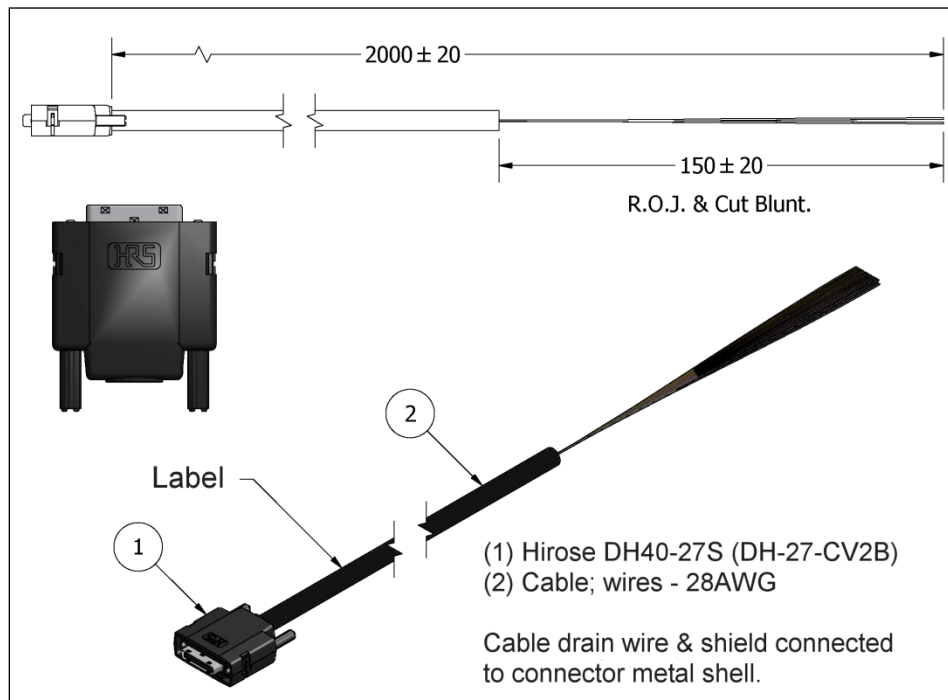


Figure 42: DH60-27P Cable No. OR-YXCC-27BE2M1 Detail



*Figure 43: Photo of cable OR-YXCC-27BE2M1*



## DH40-27S Connector Kit for Custom Wiring

Teledyne DALSA makes available a kit comprised of the DH40-27S connector plus a screw lock housing package, for clients interested in assembling their own custom I/O cable.

Order part number "OR-YXCC-H270000", (package as shown below).

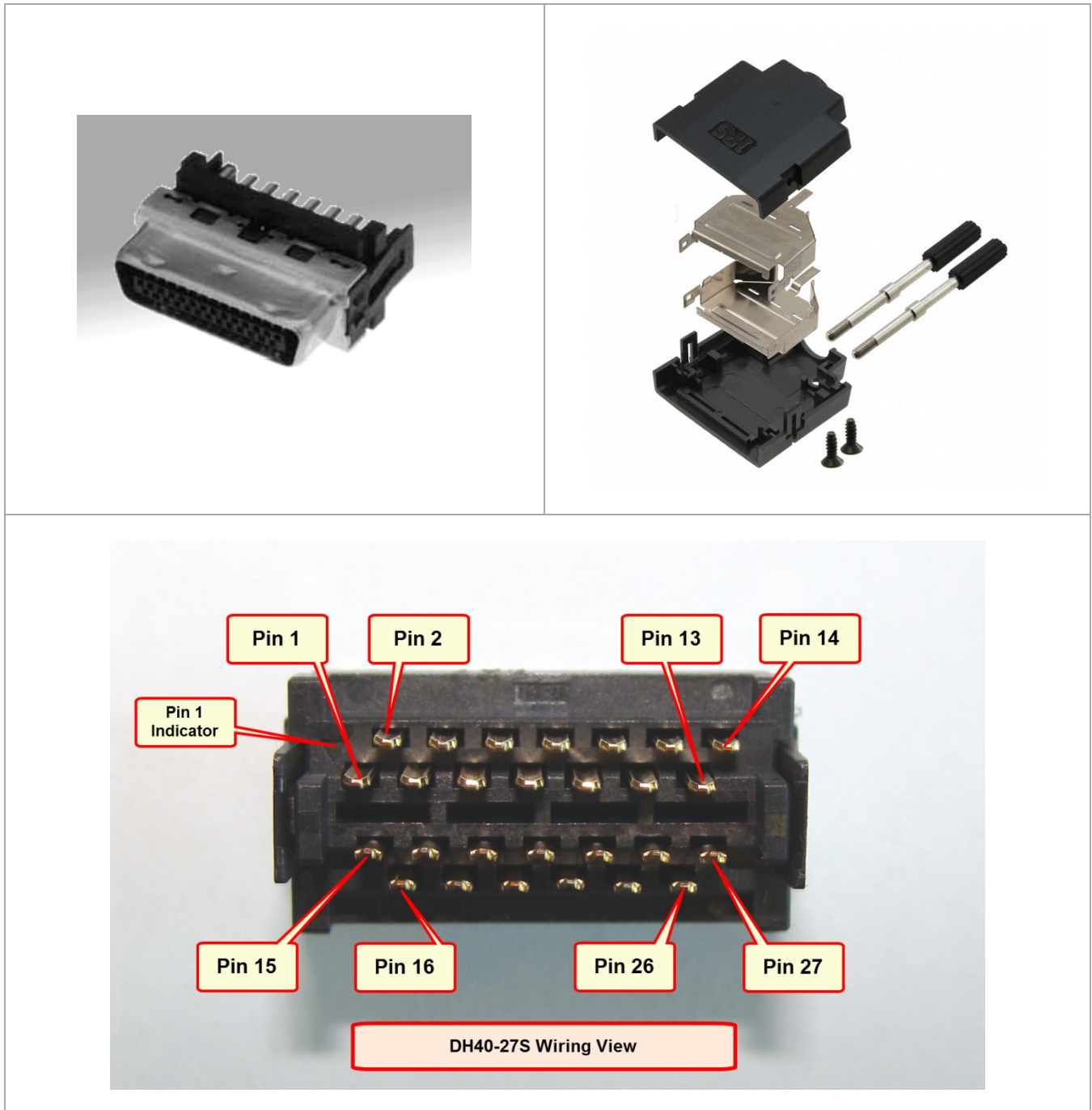


Figure 44: OR-YXCC-H270000 Custom Wiring Kit

## Cable assemblies for I/O connector J8

Flat ribbon cables for connecting J8 to a DB37 bracket can be purchased from Teledyne DALSA or from third party suppliers.

### External Signals Connector Bracket Assembly

The External Signals bracket (OC-X4CC-IOCAB) provides a simple way to bring out the signals from the External Signals Connector **J8 to a bracket mounted DB37**. Install the bracket assembly into an adjacent PC expansion slot and connect the free cable end to the board's J8 header. When connecting the cable make sure that the cable pin 1 goes to J8 pin 1.

### External Signals Connector Bracket Drawing

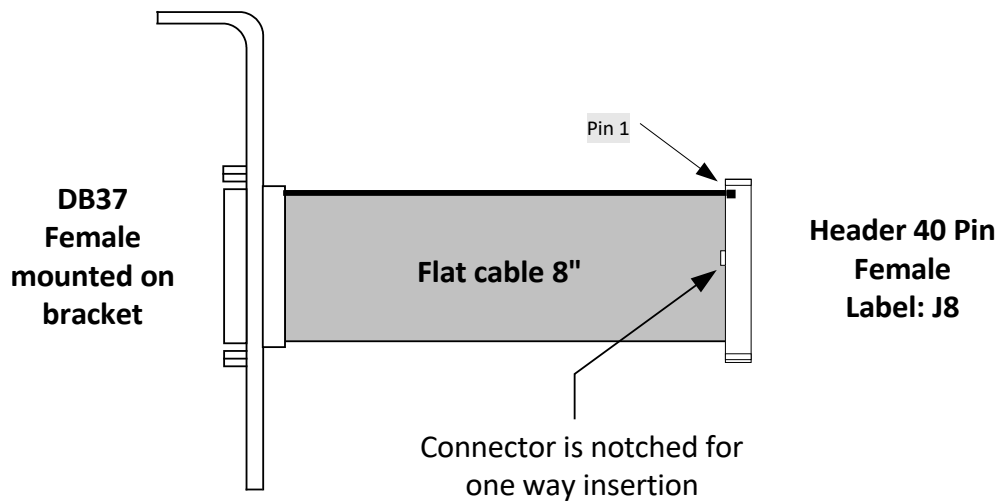


Figure 45: DB37 Output Cable

### External Signals Connector Bracket Pinout

The following table defines the signal pinout on the DB37 connector when connected to J8 of the Xtium2-CXP PX8 board.

Table 34: DB37 Cable Connector Details

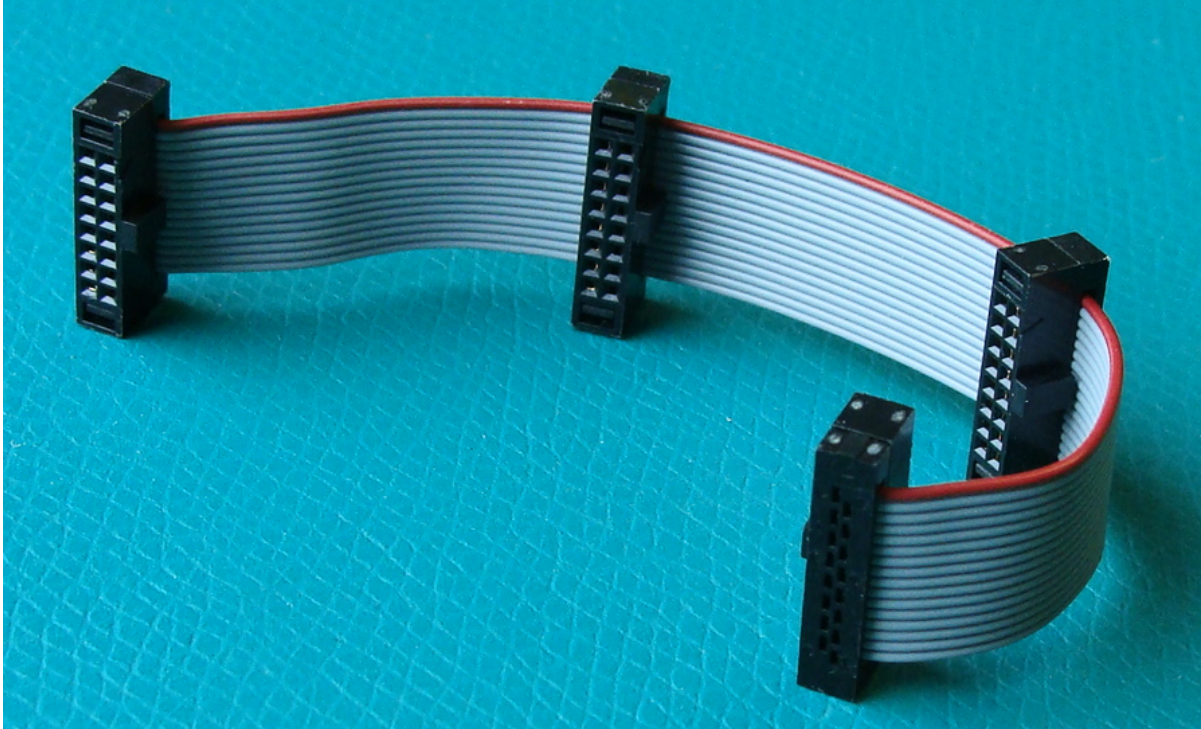
DB37 Pin Number	Signal	J8 Connector Pin Number
1	Power Output 5 Volts, 100mA max	1
20	Power Output 12 Volts, 350mA max	2
2	Ground	3
21	Ground	4
3	TTL/RS-422 Shaft Encoder Phase A (+)	5
22	RS-422 Shaft Encoder Phase A (-)	6
4	TTL/RS-422 Shaft Encoder Phase B (+)	7
23	TTL/RS-422 Shaft Encoder Phase B (-)	8
5	Ground	9
24	Ground	10
6	Strobe 1 / General Output 1	11
25	Strobe 2 / General Output 2	12
7	Strobe 3 / General Output 3	13
26	Strobe 4 / General Output 4	14
8	General Output 5	15
27	General Output 6	16
9	General Output 7	17
28	General Output 8	18
10	Ground	19
29	Ground	20
11	External Trigger Input 1/General Input 1 (+)	21
30	External Trigger Input 1/General Input 1 (-)	22
12	External Trigger Input 2/General Input 2 (+)	23
31	External Trigger Input 2/General Input 2 (-)	24
13	External Trigger Input 3/General Input 3 (+)	25
32	External Trigger Input 3/General Input 3 (-)	26
14	External Trigger Input 4/General Input 4 (+)	27
33	External Trigger Input 4/General Input 4 (-)	28
15	Reserved	29
34	Reserved	30
16	Reserved	31
35	Reserved	32
17	Reserved	33
36	Reserved	34
18	Reserved	35
37	Reserved	36
19	Reserved	37
—	Ground	38
—	Ground	39
—	Ground	40

## Board Sync Cable Assembly OR-YXCC-BSYNC40

This cable connects 3 to 4 Xtium2 boards for the board sync function as described in section [J9: Multi-Board Sync / Bi-directional General I/Os](#).

For a shorter 2-board cable, order cable assembly OR-YXCC-BSYNC20.

For a third part source of cables contact <https://www.samtec.com/> for information.

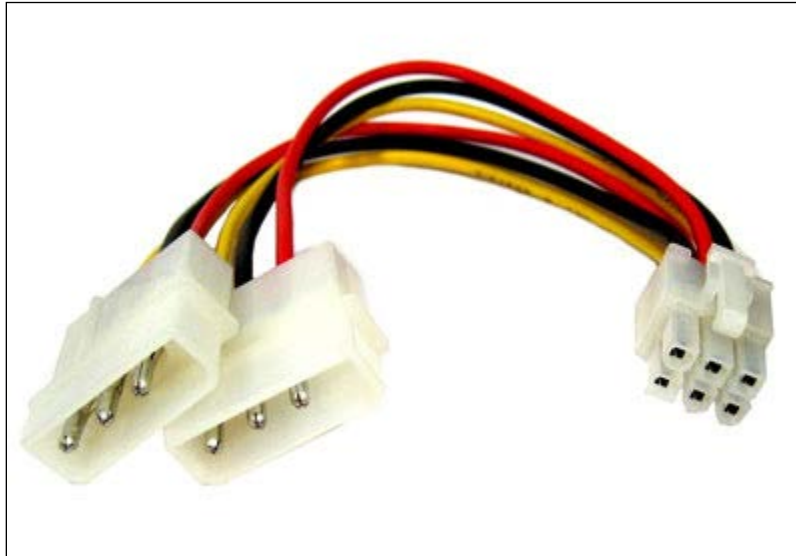


*Figure 46: Photo of cable OR-YXCC-BSYNC40*

## Power Cable Assembly OR-YXCC-PWRY00

When the Xtium2-CXP PX8 supplies power to cameras via PoCXP, the PC power must be connected to the Xtium2 external power source connector (J10).

Recent computer power supplies provide multiple 6-pin power source connectors for PCI Express video cards, where one is connected to J10 on the Xtium2-CXP. However, if the computer is an older model, this power supply adapter converts two standard 4-pin large power connectors to a 6-pin power connector.



*Figure 47: Photo of cable assembly OR-YXCC-PWRY00*

This is an industry standard adapter cable, which can be purchased from Teledyne DALSA.

# CoaXPress Interface

---

## CoaXPress Overview



**Note:** The following text is extracted from the CoaXPress website; refer to their site [www.coaxpress.com](http://www.coaxpress.com) for additional information.

CoaXPress (CXP) is an asymmetric high-speed point-to-point-serial communication standard for the transmission of video and still images, scalable over single or multiple coaxial cables.

It has a high-speed downlink of up to 12.5 Gbps (HDBNC connector) / 6.25 Gbps (DIN connector) per cable for video, images and data, plus a lower speed, up to 41.6 Mbps (HDBNC connector) / 20.83 Mbps (DIN connector) uplink for communications and control.

Power is also available over the cable (“Power-over-Coax”) and cable lengths of greater than 100 m may be achieved.

- High-speed data rates: up to 12.5 Gbps over a single coax cable and scalable for multiple cables (for example, 4 cables give 50 Gbps, 8 cables give 100 Gbps, and so forth)
- Long Cable Lengths: In excess of 100 m at 3.125 Gbps, 40 m at 6.25 Gbps and 30 m at 12.5 Gbps
- Real time behavior with fixed, low latency transmission
- Precise triggering capability
- Flexible and reliable through use of standard coax – for example, RG59 and RG6
- Ease of integration: image data, communication, control and power over a single coax cable
- Cost-effective cabling solutions
- Hot pluggable
- Royalty-free solution

# Appendix A: Silent Installation

Both Sapera LT and the Xtium2-CXP PX8 driver installations share the same installer technology. When the installations of Teledyne DALSA products are embedded within a third party's product installation, the mode can either have user interaction or be completely silent. The following installation mode descriptions apply to both Sapera and the hardware driver.



You must restart the computer after the installation of Sapera LT. However, to streamline the installation process, Sapera LT can be installed without restarting before installing the board hardware device drivers. The installations then complete with a single final system reboot.

Perform Teledyne DALSA embedded installations in either of these two ways:

- **Normal Mode**  
The default mode is interactive. This is identical to running the setup.exe program manually from Windows (either run from Windows Explorer or the Windows command line).
- **Silent Mode**  
This mode requires no user interaction. A preconfigured response file provides the user input. The installer displays nothing.

---

## Silent Mode Installation

A Silent Mode installation is recommended when integrating Teledyne DALSA products into your software installation. The silent installation mode allows the device driver installation to proceed without any user interaction.

Preparing a Silent Mode Installation requires two steps:

- Prepare the response file, which emulates a user.
- Invoke the device driver installer with command options to use the prepared response file.

### Creating a Response File

Create the installer response file by performing a device driver installation with a `-r` command line switch. The response file is automatically named `setup.iss` and is saved in the `\windows` folder. If a specific directory is desired, use also the `-f1` switch.

As an example, to save a response file in the same directory as the installation executable of the Xtium2-CXP PX8<sup>1</sup>, the command line would be:

```
Xtium2-CXP_PX8_1.00.00.0000 -r -f1" .\setup.iss"
```

---

<sup>1</sup> Note that the name of the installer executable will reflect the version to be installed, instead of all the zeros indicated here.

## Running a Silent Mode Installation

A device driver silent installation, whether done alone or within a larger software installation requires the device driver executable and the generated response file.

Execute the device driver installer with the following command line:

```
Xtium2-CXP_PX8_1.00.00.0000 -s -f1" .\setup.iss"
```

Where the `-s` switch specifies the silent mode and the `-f1` switch specifies the location of the response file. In this example, the switch `-f1" .\setup.iss"` specifies that the `setup.iss` file be in the same folder as the device driver installer.



On Windows 10, the Windows Security dialog box will appear unless one has already notified Windows to *Always trust software from "Teledyne DALSA Inc."* during a previous installation of a driver.

---

## Silent Mode Uninstall

A response file must be prepared prior to silently removing the device driver.

### Creating a Response File

The installer response file is created by performing a device driver un-installation with a `-r` command line switch. The response file is automatically named `setup.iss` which is saved in the `\windows` folder. If a specific directory is desired, the `-f1` switch is used.

For instance, to save a response file in the same directory as the installation executable of the Xtium2-CXP PX8, the command line would be:

```
Xtium2-CXP_PX8_1.00.00.0000 -r -f1" .\setup_uninstall.iss"
```

### Running a Silent Mode Uninstall

To uninstall silently, the device driver requires the device driver executable and the generated response file.

Execute the device driver installer with the following command line:

```
Xtium2-CXP_PX8_1.00.00.0000 -s -f1" .\setup_uninstall.iss"
```

Where the `-s` switch specifies the silent mode and the `-f1` switch specifies the location of the response file. In this example, the switch `-f1" .\setup_uninstall.iss"` specifies that the `setup_uninstall.iss` file be in the same folder as the device driver installer.



---

## Silent Mode Installation Return Code

A silent mode installation creates a corinstall.ini file in the Windows directory. A section called [SetupResult] contains the status of the installation.

- A value of **1** indicates that the installation has started.
- A value of **2** indicates that the installation has terminated.

A silent mode installation also creates a setup.log log file, which by default is created in the same directory and with the same name (except for the extension) as the response file. The -f2 switch enables you to specify an alternative log file location and file name, as in:

```
Setup.exe -s -f2"C:\Setup.log"
```

The setup.log file contains three sections. The first section, [InstallShield Silent], identifies the version of InstallShield used in the silent installation. It also identifies the file as a log file. The second section, [Application], identifies the installed application name, version, and the company name. The third section, [ResponseResult], contains the ResultCode indicating whether the silent installation succeeded. A value of **0** means the installation was successful.

---

## Installation Setup with CorAppLauncher.exe

The installation setup can be run with the CorAppLauncher.exe tool provided with the driver.

- Install the board driver and get CorAppLauncher.exe from the \bin directory of the installation.
- When running the installation, CorAppLauncher.exe will return only when the installation is finished.
- When run from within a batch file, obtain the installation exit code from the ERRORLEVEL value.
- The arguments to CorAppLauncher.exe are:
  - -l: Launch application
  - -f: full path of the application to launch.

### As an example:

```
CorAppLauncher -l -f"c:\driver_install\Xtium2-CXP_PX8_1.00.00.0000.exe"  
IF %ERRORLEVEL% NEQ 0 goto launch error
```

**Note:** There is a 32-bit and 64-bit version of CorAppLauncher.exe. When installing the driver, only the version related to the OS is installed. However, the 32-bit version is usable on either 32-bit or 64-bit Windows.

# Custom Driver Installation using install.ini

Customize the driver installation using parameters defined in the file install.ini. By using this file, the user can:

- Select the user default configuration.
- Select different configurations for systems with multiple boards.
- Assign a standard Serial COM port to board.

## Creating the install.ini File

- Install the driver in the target computer. All Xtium2-CXP PX8 boards required in the system must be installed.
- Configure each board's acquisition firmware using the Teledyne DALSA Device Manager tool (see [Device Manager – Board Viewer](#)).
- When each board setup is complete, using the Teledyne DALSA Device Manager tool, click **Save Config File**. This will create the install.ini file.

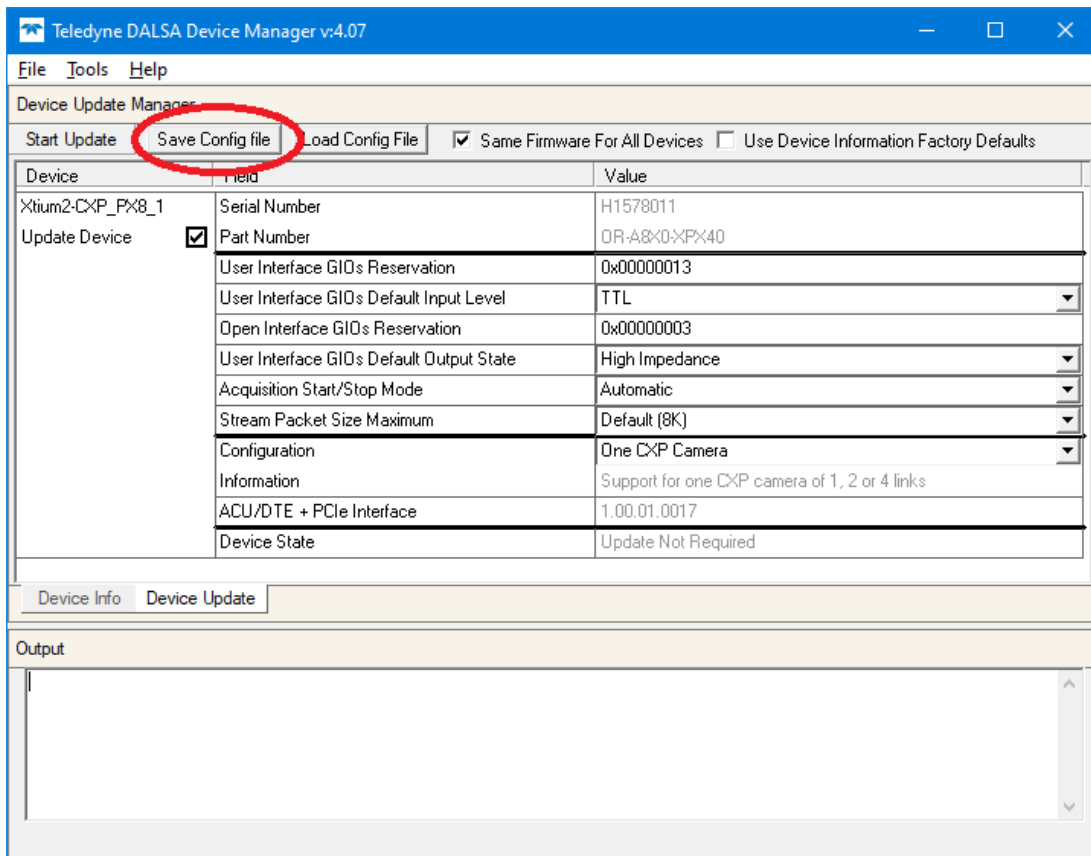


Figure 48: Create an install.ini File

## Run the Installation using install.ini

Copy the install.ini file into the same directory as the setup installation file. Run the setup installation as normal. The installation will automatically check for an install.ini file and if found, use the configuration defined in it.

# Appendix B: Troubleshooting Problems

---

## Overview

The Xtium2-CXP PX8 (and the Xtium family of products) is tested by Teledyne DALSA in a variety of computers. Although unlikely, installation problems may occur due to the constant changing nature of computer equipment and operating systems. This section describes what the user can verify to determine the problem or the checks to make before contacting Teledyne DALSA Technical Support.

If you require help and need to contact Teledyne DALSA Technical Support, make detailed notes on your installation and/or test results for our technical support to review. See [Technical Support](#) for contact information.

---

## Problem Type Summary

Xtium2-CXP PX8 problems are either installation types where the board hardware is not recognized on the PCIe bus (i.e. trained), or function errors due to camera connections or bandwidth issues. The following links jump to various topics in this troubleshooting section.

### First Step: Check the Status LED

Status LED 'S' should be **BLUE** or flashing **BLUE** just after power up. If it remains flashing **RED**, the board firmware did not load correctly. Once the Windows driver is started, the status LED should be **GREEN** or flashing **GREEN**. If it remains **BLUE** or flashing **BLUE**, the board is still running from the safe mode load. This could indicate that the normal operating load from the flash memory is corrupted or not present.

CXP Link status is indicated by LEDs (L1, L2, L3 and L4). The status colors displayed follow industry specifications for CoaXPress.

The complete status LED descriptions are available in the technical reference section, (see [Status LEDs Functional Descriptions](#)).

### Possible Installation Problems

- **Hardware PCI bus conflict:** When a new installation produces PCI bus error messages or the board driver does not install, it is important to verify that there are no conflicts with other PCI or system devices already installed. Use the Teledyne DALSA PCI Diagnostic tool as described in [Checking for PCI Bus Conflicts](#). Also, verify the installation via the [Windows Device Manager](#).
- **BSOD (blue screen) following a board reset:** After programming the board with different firmware, the computer displays the BSOD when the board is reset (see [BSOD \(blue screen\) Following a Board Reset](#)).
- **Verify Sopera and Board drivers:** If there are errors when running applications, confirm that all Sopera and board drivers are running. See [Sopera and Hardware Windows Drivers](#) for details. In addition, Teledyne DALSA technical support will ask for the log file of messages by Teledyne DALSA drivers. Follow the instructions describe in [Sopera Log Viewer](#).

- **Firmware update error:** There was an error during the Xtium2-CXP PX8 firmware update procedure. The user usually can easily correct this. Follow the instructions [Recovering from a Firmware Update Error](#).
- Installation went well but the board does not work or stopped working. Review these steps described in [Symptoms: CamExpert Detects no Boards](#).
- **Using Windows 10/11 Fast Startup option:** When adding, removing, or moving boards while the PC is shutdown with the Windows Fast Startup option activated, it is possible that the boards are not mapped properly on the next reboot of the computer. The driver will detect such a situation and the Device Manager launched at startup will display a message indicating that a normal reboot is required.

Define power buttons and turn on password protection

Choose the power settings that you want for your computer. The changes you make to the settings on this page apply to all of your power plans.

[Change settings that are currently unavailable](#)

Power and sleep buttons and lid settings

	On battery	Plugged in
When I press the power button:	Hibernate	Hibernate
When I press the sleep button:	Sleep	Sleep
When I close the lid:	Sleep	Do nothing

Shutdown settings

Turn on fast startup (recommended)  
 This helps start your PC faster after shutdown. Restart isn't affected. [Learn More](#)

- Sleep  
Show in Power menu.
- Hibernate  
Show in Power menu.
- Lock  
Show in account picture menu.

## Possible Functional Problems

- **Driver Information:** Use the Teledyne DALSA device manager program to view information about the installed Xtium2-CXP PX8 board and driver. See [Driver Information via the Device Manager Program](#).
- **On-Board Image Memory Requirements:** The Xtium2-CXP PX8 on-board memory can provide two frame buffers large enough for most imaging situations. See [On-board Image Memory Requirements for Acquisitions](#) for details on the on board memory and possible limitations.

Sometimes the problem symptoms are not the result of an installation issue but due to other system issues. Review the sections described below for solutions to various Xtium2-CXP PX8 functional problems.

- [Symptoms: Xtium2-CXP PX8 Does Not Grab](#)
- [Symptoms: Card grabs black](#)
- [Symptoms: Card acquisition bandwidth is less than expected](#)

# Troubleshooting Procedures

The following sections provide information and solutions to possible Xtium2-CXP PX8 installation and functional problems. The previous section of this manual summarizes these topics.

## Diagnostic Tool Overview

The Xtium2-CXP PX8 Board Diagnostic Tool provides a quick method to see board status and health. It additionally provides live monitoring of FPGA temperature and voltages, which may help in identifying problems.

A shortcut to this tool is in the Windows **Start** menu under the **Teledyne DALSA/Xtium2-CXP PX8** folder. Do not have any other Sopera application running that connects to the Xtium2 such as CamExpert, else the diagnostic window will indicate an error for the PCIe Bandwidth, as shown in the screen capture below.

	Bus Bit Transfer Rate	Gen 3		
	Bus Payload Size (bytes)	256		
	Bus Request Size (bytes)	512		
PCIe Bandwidth (MB/s)	Achieved Bandwidth	Resource in use	Resource in use	Resource in use
	Maximum Theoretical	Resource in use		
FPGA Temperature (°C)	Measured	70.256	70.256	70.256

Figure 49: Diagnostic Tool "Resource in use"

## Diagnostic Tool Main Window

The main window provides a comprehensive view of the installed Xtium2 board. Toolbar buttons execute the board self-test function and open a FPGA live status window.

Important parameters include the PCI Express bus transfer supported by the host computer and the internal Xtium2 FPGA temperature. The bus transfer defines the maximum data rate possible in the computer, while an excessive FPGA temperature may explain erratic acquisitions due to poor computer ventilation.



**Note:** The Lane Stats for each camera are aggregated into the lane # detected as master. However 8b/10b error statistics are compiled for each lane independently.

The screenshot shows the Diagnostic Tool Main Window with the following callouts and data sections:

- Generate Report**: Callout pointing to the File menu icon.
- Save Report**: Callout pointing to the Save icon.
- Execute Self-Test**: Callout pointing to the Refresh/Reload icon.
- Live FPGA Monitor**: Callout pointing to the TEST button.
- Camera Input Monitor**: Callout pointing to the camera icon.
- Computer Slot**: Callout pointing to the PCI Info section of the Frame Grabber Information table.
- FPGA Monitor**: Callout pointing to the FPGA Temperature section of the Frame Grabber Information table.
- Sapera & System Monitor**: Callout pointing to the System Resource and Sapera Memory sections.
- PCI Slot Type**: Callout pointing to the Gen 3 value in the PCI Info section.
- Data Transfer Performance**: Callout pointing to the PCIe Bandwidth section of the Frame Grabber Information table.
- Right click to Reset Lane Statistics**: Callout pointing to the Lane 3 row in the Lanes Stats table.

**Frame Grabber Information Table:**

Field/Value	Value	Min	Max	Alarm
Driver Version	1.00.01.0011			
Serial Number	H1578003			
PCI Info				
Bus #	4			
Slot #	0			
Function #	0			
Bus Total Lanes	8			
Bus Bit Transfer Rate	Gen 3			
Bus Payload Size (bytes)	256			
Bus Request Size (bytes)	512			
PCIe Bandwidth (MB/s)				
Achieved Bandwidth	6719	6701	6727	
Maximum Theoretical	7000			
FPGA Temperature (°C)				
Measured	94.641	94.151	95.008	Off
Operating Range		0.000	100.000	
Alarm Range		0.000	100.0	
Voltage Aux (V)				
Measured	1.767	1.765	1.768	Off
Operating Range		1.746	1.854	
Alarm Range		1.746	1.854	
Voltage Int (V)				
Measured	0.955	0.953	0.955	Off
Operating Range		0.922	0.979	
Alarm Range		0.922	0.979	

**Lanes Stats Table:**

	CRC Error	Video MSG	Packet Buffer Overflow	Packet Size Error	8b/10b Error
Lane 1	0	0	0	0	0
Lane 2	0	0	0	0	1615
Lane 3	0	0	0	0	1589
Lane 4	0	0	0	0	0

**System Resource Table:**

	Total	Free	Handles	Process	Thread
Physical Memory	8114 MB	4606 MB			
Page File	9394 MB	3922 MB			
Total			89368	189	2410

**Sapera Memory Table:**

	Free	Used	Free Blocks	Largest Free Block	Used Blocks	Largest Used Block
Message Memory	3072 KB	0 B	1	3072 KB	0	0 B
Buffer Memory (32-bit)	3072 KB	0 B	1	3072 KB	0	0 B
Buffer Memory (64-bit)	0 B	0 B	0	0 B	0	0 B

Figure 50: Diagnostic Tool Main Window

## Diagnostic Tool Self-Test Window

Click the Start button to initiate the board memory self-test sequence. A healthy board will pass all memory test patterns.

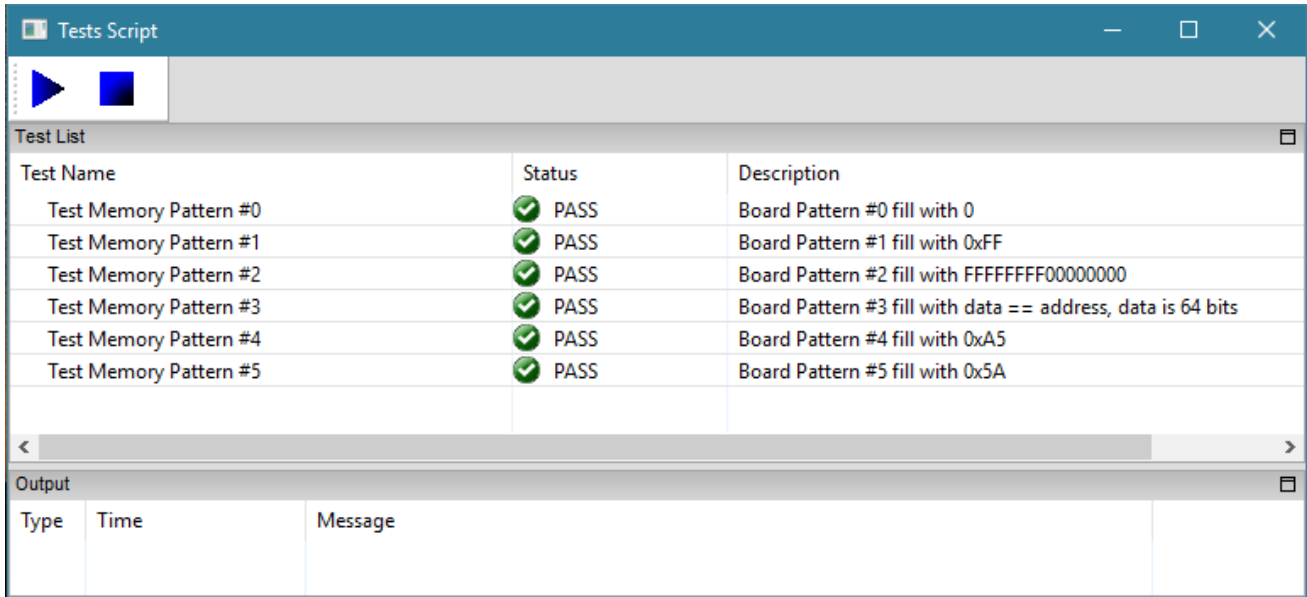


Figure 51: Diagnostic Tool Main Window

## Camera Input Eye Diagram Monitor

Eye Diagrams allow the user to evaluate visibly the signal integrity between camera data lanes or between different cable sets. This tool does not provide specific measurements but will help to identify signal noise or jitter associated with bad cables or overly long cables.

The screen capture below shows a camera with four data lanes, where each digital signal is repetitively sampled and overlaid over itself, showing relative low-high transitions of the differential signal. The blue center area (eye surface) seems similar between each lane, typical for a good cable set.

The closure (collapse or horizontal shortening) of the eye surface would indicate problems such as poor signal to noise, high cable capacitance, multipath interference, among many possible digital transmission faults.

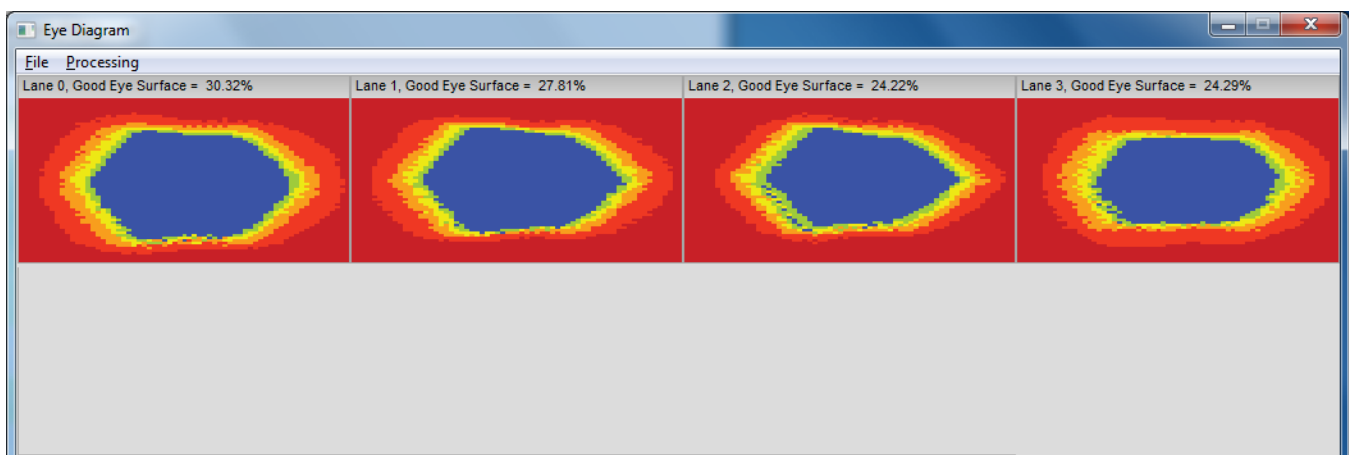


Figure 52: Eye Diagram

## Diagnostic Tool Live Monitoring Window

The three FPGA parameters listed on the main window can also be monitored in real time. Choosing a parameter puts that graph at the top where the user can select the time unit and time range. Clicking the Output button will open a window displaying any error messages associated with that parameter.



Figure 53: Diagnostic Tool Live Monitoring Window

## Checking for PCI Bus Conflicts

One of the first items to check when there is a problem with any PCI board is to examine the system PCI configuration and ensure that there are no conflicts with other PCI or system devices. The *PCI Diagnostic* program (**cpcdiag.exe**) allows examination of the PCI configuration registers and can save this information to a text file. Run the program from the **Start** menu under **Teledyne DALSA Sapera LT > Sapera PCi Diagnostics**.

As shown in the following screen image, use the first drop menu to select the PCI device to examine. Select the device from Teledyne DALSA. Note the bus and slot number of the installed board (this will be unique for each system unless systems are setup identically). Click on the **Diagnostic** button to view an analysis of the system PCI configuration space.



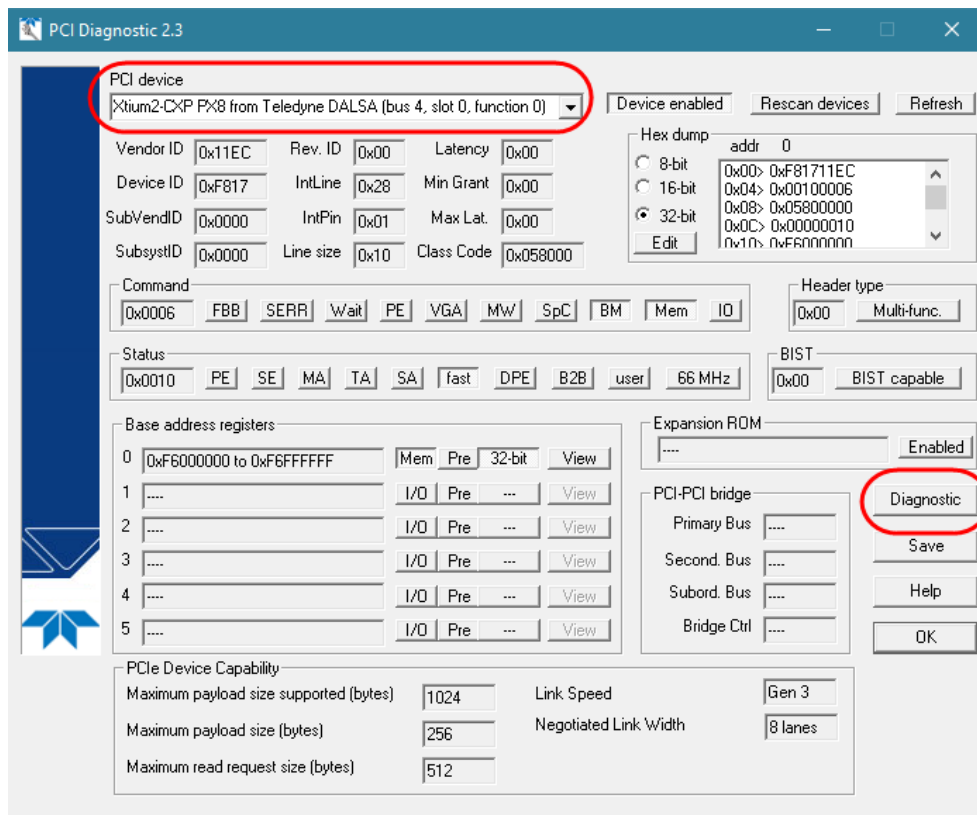


Figure 54: PCI Diagnostic Program

Clicking on the **Diagnostic** button opens a new window with the diagnostic report. From the PCI Bus Number drop menu, select the bus number that the Xtium2-CXP PX8 is installed in—in this example, the slot is bus 4.

The window now shows the I/O and memory ranges used by each device on the selected PCI bus. The information display box will detail any PCI conflicts. If there is a problem, click on the **Save** button. A file named '**pcidiag.txt**' is created (in the Sapera\bin directory) with a dump of the PCI configuration registers. Email this file when requested by the Teledyne DALSA Technical Support group along with a full description of your computer.

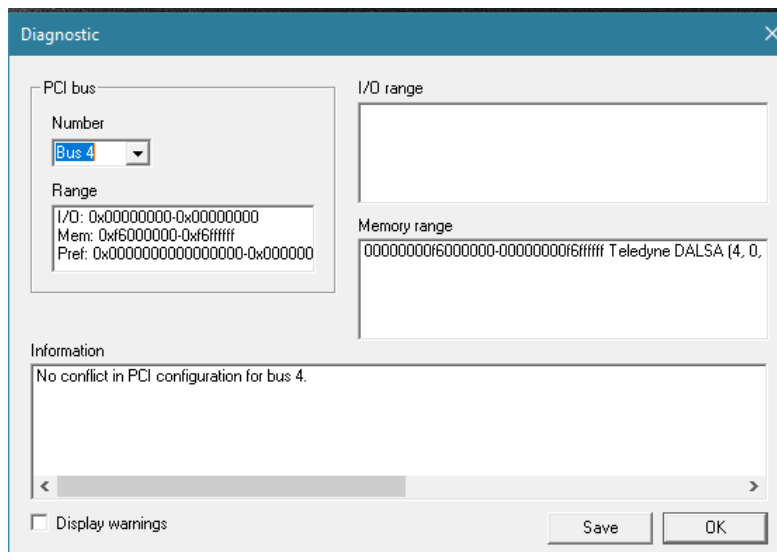


Figure 55: PCI Diagnostic Program – PCI bus info

## Windows Device Manager

An alternative method to confirm the installation of the Xtium2-CXP PX8 board and driver is to use the Windows Device manager tool.

1. Use the taskbar search box to open Device Manager.
2. Expand the **Imaging devices** node.
3. Select a Xtium2-CXP PX8 Board.
4. On the shortcut menu, select **Properties**. The **Device status** should indicate “This device is working properly.”
5. In the properties window, click the **Resources** tab. Make sure that the device has an interrupt assigned to it and that there are no conflicts.

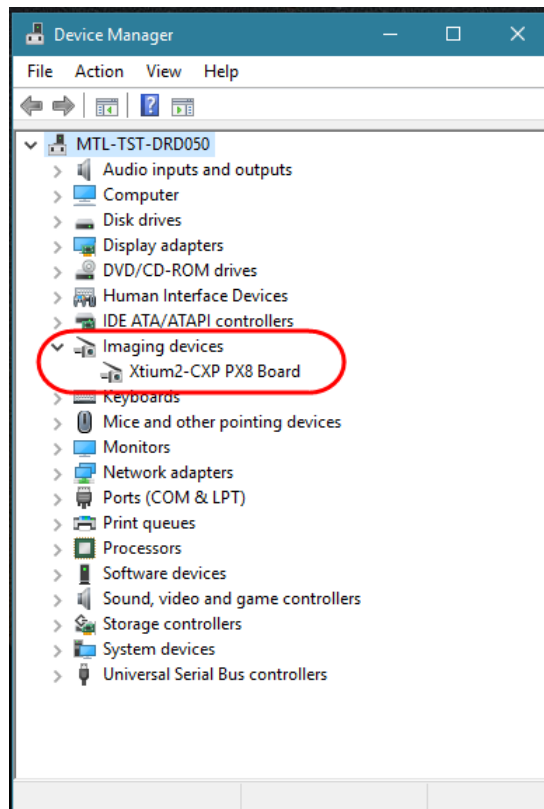


Figure 56: Using Windows Device Manager

## BSOD (blue screen) Following a Board Reset

There are cases where a PC will falsely report a hardware malfunction when the Xtium2-CXP PX8 board is reset. Ensure that you are using Sapera LT 7.50 or later.

## Sapera and Hardware Windows Drivers

Any problem seen after installation, such as an error message running CamExpert, first make certain the appropriate Teledyne DALSA drivers have started successfully during the boot sequence.

### To check driver status in System Information

1. Use the taskbar search box to open System Information.
2. Expand **Software Environment**.
3. Select **System Drivers**.

Make certain the following drivers have started for the **Xtium2-CXP PX8**.

Table 35: Xtium2-CXP PX8 Device Drivers

Device	Description	Type	Started
CorXtium2CXPPX8	Xtium2-CXP PX8 messaging	Kernel Driver	Yes
CorLog	Sapera Log viewer	Kernel Driver	Yes
CorMem	Sapera Memory manager	Kernel Driver	Yes
CorPci	Sapera PCI configuration	Kernel Driver	Yes
CorSerial	Sapera Serial Port manager	Kernel Driver	Yes

Teledyne DALSA Technical Support may request that you check the status of these drivers as part of the troubleshooting process.

## Recovering from a Firmware Update Error

This procedure is required if any failure occurred while updating the Xtium2-CXP PX8 firmware on installation or during a manual firmware upgrade. If on the case the board has corrupted firmware, any Sapera application such as CamExpert or the grab demo program will not find an installed board to control.

Possible reasons for firmware loading errors or corruption are:

- Power failure or deep brown-out.
- PCI bus or checksum errors.
- PCI bus timeout conditions due to other devices.
- User forcing a partial firmware upload using an invalid firmware source file.

When the Xtium2-CXP PX8 firmware is corrupted, the board will automatically run from the Safe load after a PC reset.

### To recover from a firmware update error

- Update the board using the standard method described in section [Firmware Update: Automatic Mode](#).

## Driver Information via the Device Manager Program

The Device Manager program provides a convenient method of collecting information about the installed Xtium2-CXP PX8. System information such as operating system, computer CPU, system memory, PCI configuration space, plus Xtium2-CXP PX8 firmware information is displayed or written to a text file (default file name – BoardInfo.txt). Note that this program also manually uploads firmware to the Xtium2-CXP PX8 (described elsewhere in this manual).



## Sapera Log Viewer

The third step in the verification process is to save the information collected by the Sapera Log Viewer program. The Log Viewer lists information about the installed Teledyne DALSA drivers.

### To save information from the Sapera Log Viewer program

1. On the **Start** menu, select **Teledyne DALSA Sapera LT > Sapera Log Viewer**.
2. On the **File** menu, select **Save All Messages**.

Email this text file to Teledyne DALSA Technical Support when requested or as part of your initial contact email.

## On-board Image Memory Requirements for Acquisitions

The Xtium2-CXP PX8 by default will allocate the maximum number of buffers that can fit in on-board memory based on the size of the acquired image before cropping, to a maximum of 65 535 buffers.



**Note:** Applications can change the default number of on-board frame buffers using the Sapera LT API.

Usually, two buffers will ensure that the acquired video frame is complete and not corrupted in cases where the image transfer to host system memory may be interrupted and delayed by other host system processes. That is, there is no interruption to the image acquisition of one buffer by any delays in transfer of the other buffer (which contains the previously acquired video frame) to system memory.

If allocation for the requested number of buffers fails, the driver will reduce the number of on-board frame buffers requested until they can all fit. If there is not enough memory for 2 on-board buffers, the driver will reduce the size such that it allocates two partial buffers. This mode is dependent on reading out the image data to the host computer faster than the incoming acquisition.

The maximum number of buffers that can fit in on-board memory can be calculated as follows: (Total On-Board memory / (Buffer Size in Bytes + 256 Bytes used to store the DMA)).



**Note:** When using multi-camera configurations, the total on-board memory is divided evenly between the different inputs.

For example, assuming 1 GB of on-board memory and acquiring 1024 x 1024 x 8 bit images, the number of on-board buffers would be:

1024 MB / [(1024 x 1024) + 256] = 1023.75 => 1023 on-board buffers.

## Symptoms: CamExpert Detects no Boards

When starting CamExpert with no Teledyne DALSA board detected, CamExpert will start in offline mode. There is no error message and CamExpert is functional for creating or modifying a camera configuration file. If CamExpert should have detected an installed board frame grabber, troubleshoot the installation problem as described below.

### *Troubleshooting Procedure*

When CamExpert detects no installed Teledyne DALSA board, there could be a hardware problem, a system bus problem, a kernel driver problem, or a software installation problem.

- Make certain that the card is properly seated in PCIe slot.
- Perform all installation checks described in this section before contacting Technical Support.
- Try the board in a different PCIe slot if available.

## Symptoms: Xtium2-CXP PX8 Does Not Grab

Sapera CamExpert does start but you do not see an image and the frame rate displayed is 0.

- Verify the camera has power.
- Verify the Camera CXP cable(s) is(are) connected to the camera.
- Verify the camera and timing parameters with the camera in free run mode.
- Verify you can grab with the camera in free run mode.
- Make certain that you provide an external trigger if the camera configuration file requires one. Use the software trigger feature of CamExpert if you do not have a trigger source.
- Make certain that the camera configuration is the required mode. This must match the camera configuration file. Refer to your camera datasheet.
- Try to snap one frame instead of continuous grab.
- Perform all installation checks described in this section before contacting Technical Support.

## Symptoms: Card grabs black

You are able to use Sapera CamExpert, the displayed frame rate is as expected, but the display is always black.

- Set your camera to manual exposure mode and set the exposure to a longer period, plus open the lens iris.
- Try to snap one frame instead of continuous grab.
- Make certain that the input LUT is not programmed to output all 0s.
- A PCIe transfer issue sometimes causes this problem. No PCIe transfer takes place, so the frame rate is above 0 but nevertheless no image is displayed in CamExpert.
- Make certain that BUS MASTER bit in the PCIe configuration space is activated. Look in PCI Diagnostics for the **Command** group, and make sure that the **BM** button is activated (see Figure 57).
- Perform all installation checks described in this section before contacting Technical Support.

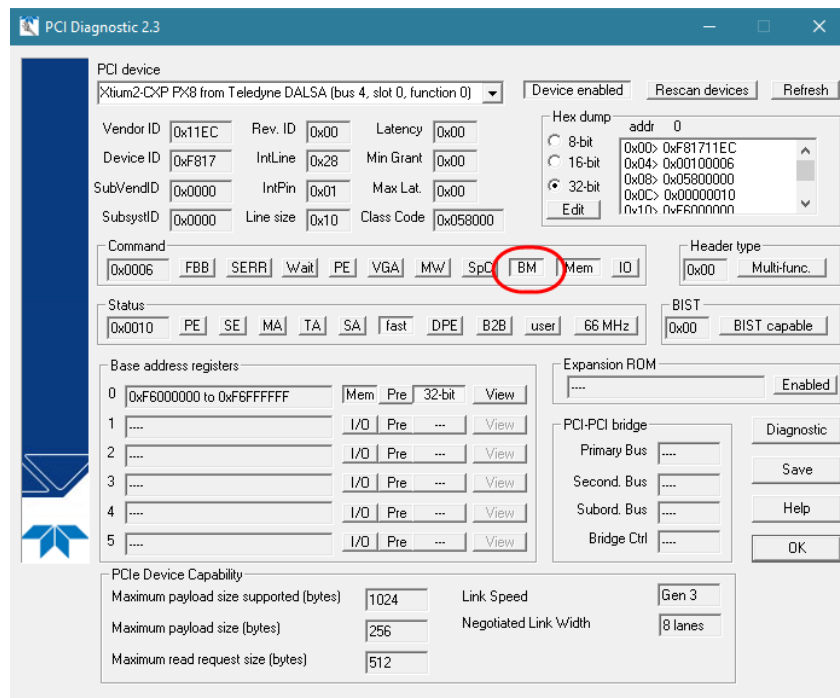


Figure 58: PCI Diagnostic Tool

## Symptoms: Card acquisition bandwidth is less than expected

The Xtium2-CXP PX8 acquisition bandwidth is less than expected.

- Review the system for problems or conflicts with other expansion boards or drivers.
- Remove other PCI Express, PCI-32 or PCI-64 boards and check acquisition bandwidth again. Engineering has seen this case where other PCI boards in some systems cause limitations in transfers. Each system, with its combination of system motherboard and PCI boards, will be unique and must be tested for bandwidth limitations affecting the imaging application.
- Is the Xtium2-CXP PX8 installed in a PCI Express x16 slot?  
Note that some computer's x16 slot may only support non x16 boards at x1 or not at all. Check the computer documentation or test an Xtium2-CXP PX8 installation. The speed at which the board is running can be viewed using the Diagnostic Tool provided with the driver.
- Is the Xtium2-CXP PX8 installed in a PCI Express Gen1 slot?  
Some older computers only have PCIe Gen1 slots. The Generation at which the board is running can be viewed using the [Diagnostic Tool](#) provided with the driver.
- Is the PCI maximum payload size smaller than 256 bytes?  
On some computers, this parameter can be changed in the PC's BIOS.

## Symptoms: PoCXP does not power the camera

If the Xtium2-CXP PX8 does not power the camera, do the following:

- Ensure that a spare power supply connector from the PC power supply is connected to J10.
- If the camera is powered by means of multiple connectors, make sure all the necessary connections are made between the camera and the frame grabber.
- Ensure that Power-over-CXP (PoCXP) is enabled. CamExpert can be used to verify that the PoCXP parameter, available in the Basic Timing category, is set to Enable.

Category	Parameter	Value
Basic Timing	Camera Type	Areascan
	Color Type	Monochrome
	Pixel Depth	8
	Data Lanes	4
	Horizontal Active ...	4096
	Vertical Active (in ...	3072
	Bit Transfer Rate	1.250 Gb/s
	PoCXP	Enable
	PoCXP Status	Disabled
		Enable

Figure 59: CamExpert PoCXP Parameter

- If PoCXP is enabled in CamExpert, check that the Video status PoCXP of the respective connection is green.



Figure 60: CamExpert Video Status Bar

## Over-current protection circuit is tripped

To identify this condition:

- Ensure a CXP camera is connected to the Xtium2-CXP board.
- Use CamExpert and verify that the PoCXP is enabled.

Verify the Video status PoCXP of the respective connection that requires power; a red status indicates a tripped state of the over-current protection circuit.

To confirm the tripped state, start Sopera Log Viewer and search for a message similar to the following:

```
"ERR 2017/12/15 11:10:32:307 CorXtium2CXPPX8.SYS: smPoCXP[brd=0, poCxp=0]: 24V TRIP."
```

where:

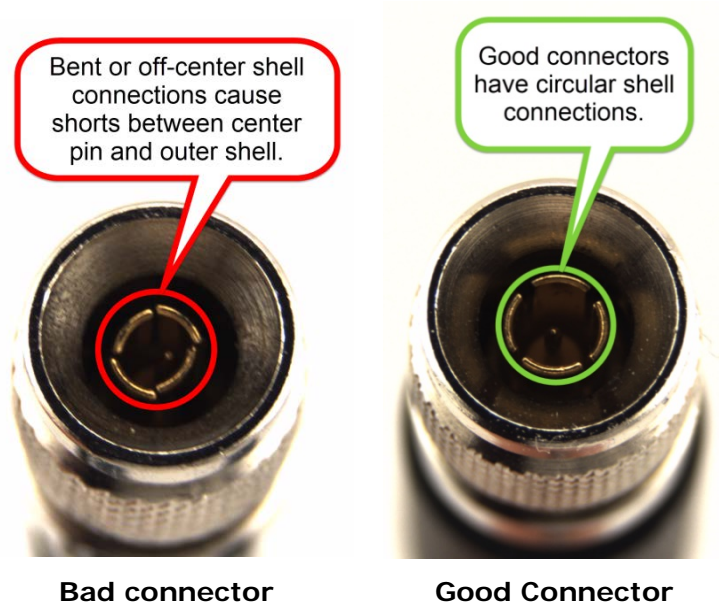
brd: indicates the index of the CXP PX8 board in the system

poCxp: indicates the index of the CXP connector - 1

### To clear the TRIP condition of the Xtium2-CXP PX8 over-current circuit

1. Open the Sopera Log Viewer and clear its contents.
2. Start CamExpert and set PoCXP to *Disabled*, then change the setting to *Enable*. This resets the over-current protection circuit for the current acquisition module. If necessary, perform this procedure for any other cameras in this condition connected to the board.
3. If over-current condition occurs, the PoCXP Video status remains red and the Log Viewer displays a message similar to the one above; verify that the CXP connectors attached to the cables are in good condition. Use the following pictures as a guide.





*Figure 61: Bad vs. Good CXP Connectors*

# Revision History

Revision	Date	Major Changes
1.00	2 October 2020	Initial release.
1.01	15 March 2023	New board and related parameters.

# Contact Information

## Sales Information

<b>Visit our web site:</b>	<a href="http://www.teledynedalsa.com/en/products/imaging/">www.teledynedalsa.com/en/products/imaging/</a>
<b>Email:</b>	<a href="mailto:info@teledynedalsa.com">mailto:info@teledynedalsa.com</a>
<b>Canadian Sales</b>	<b>Canadian Sales</b>
<p>Teledyne DALSA — Head office 605 McMurray Road Waterloo, Ontario N2V 2E9 Canada</p> <p>Tel: +1 519-886-6000 Fax: +1 519-886-8023</p>	<p>Teledyne DALSA — Montreal office 880 Rue McCaffrey Saint-Laurent, Quebec H4T 2C7 Canada</p> <p>Tel: +1 514-333-1301 Fax: +1 514-333-1388</p>
<b>USA Sales</b>	<b>European Sales</b>
<p>Teledyne DALSA — Billerica office 700 Technology Park Drive Billerica, MA 01821 USA</p> <p>Tel: +1 978-670-2000 Fax: +1 978-670-2010</p> <p><a href="mailto:sales.americas@teledynedalsa.com">sales.americas@teledynedalsa.com</a></p>	<p>Teledyne DALSA GMBH Lise-Meitner-Str. 7 82152 Krailling (Munich) Germany</p> <p>Tel: +49 89-89545730 Fax: +49 89-895457346</p> <p><a href="mailto:sales.europe@teledynedalsa.com">sales.europe@teledynedalsa.com</a></p>
<b>Asia Pacific Sales</b>	<b>Asia Pacific Sales</b>
<p>Teledyne DALSA Asia Pacific Ikebukuro East 6F 3-4-3 Higashi Ikebukuro, Toshima-ku Tokyo, 170-0013 Japan</p> <p>Tel: +81 3-5960-6353 Fax: +81 3-5960-6354</p> <p><a href="mailto:sales.asia@teledynedalsa.com">sales.asia@teledynedalsa.com</a></p>	<p>Teledyne DALSA Asia Pacific Room 904, Block C, Poly West Bund Center 275 Rui Ping Road Shanghai 200032 China</p> <p>Tel: +86 21-60131571</p> <p><a href="mailto:sales.asia@teledynedalsa.com">sales.asia@teledynedalsa.com</a></p>

## Technical Support

Submit any support question or request via our web site:

<p><b>Technical support form via our web page:</b></p> <p>Support requests for imaging product installations, Support requests for imaging applications</p> <p>Camera support information</p> <p>Product literature and driver updates</p>	<p><a href="http://www.teledynedalsa.com/en/support/options/">www.teledynedalsa.com/en/support/options/</a></p>
--	---