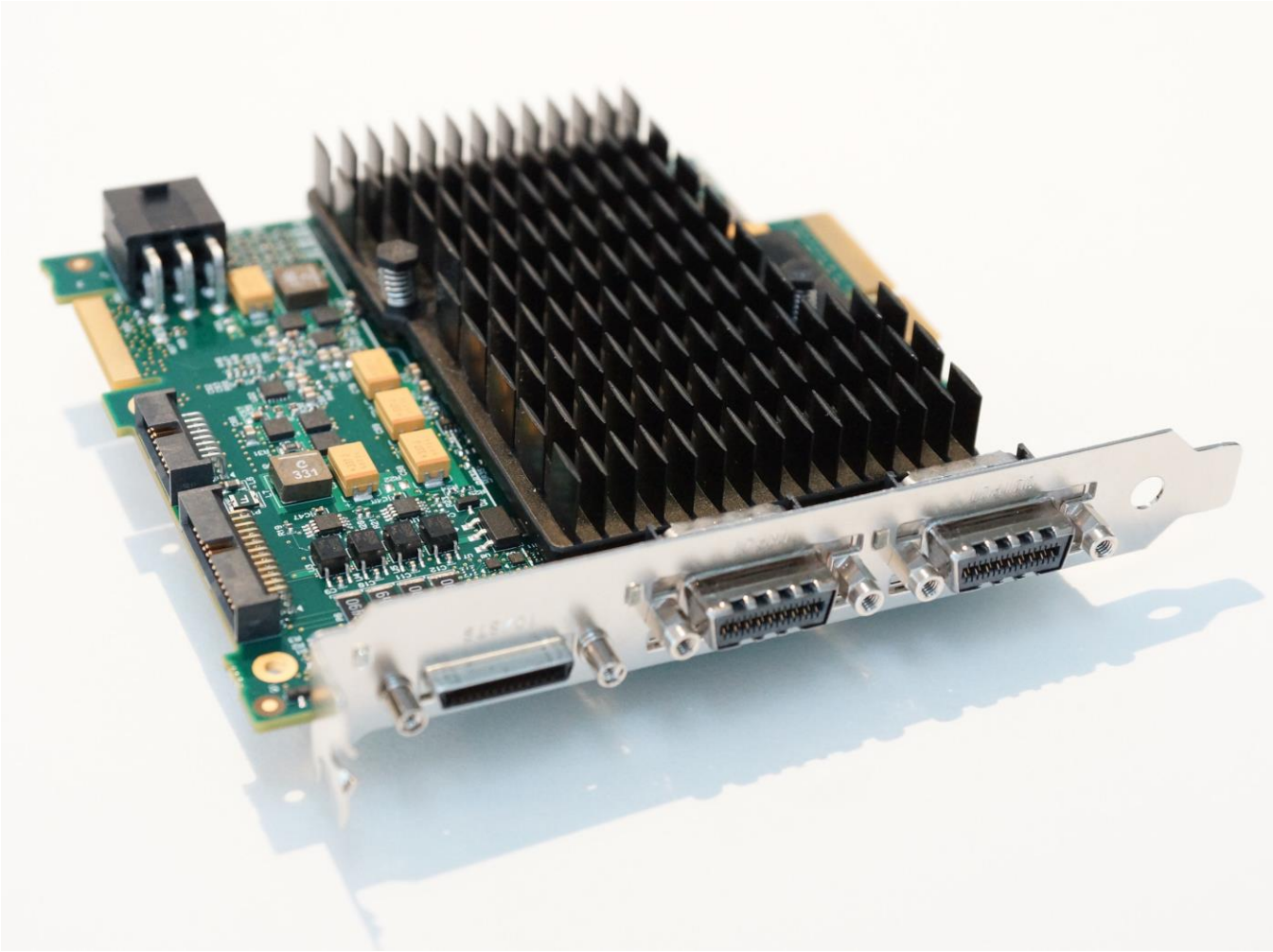
Xtium-CLHS PX4™

User's Manual

Edition 1.30

sensors | cameras | **frame grabbers** | processors | software | vision solutions



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NOTICE

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About Teledyne DALSA
Teledyne DALSA, a business unit of Teledyne Digitial Imaging Inc., is an international high performance semiconductor and Electronics Company that designs, develops, manufactures, and markets digital imaging products and solutions, in addition to providing wafer foundry services.

Teledyne Digital Imaging offers the widest range of machine vision components in the world. From industry-leading image sensors through powerful and sophisticated cameras, frame grabbers, vision processors and software to easy-to-use vision appliances and custom vision modules.

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Overview

Product Part Numbers

Xtium-CLHS PX4 Board

Item	Product Number
Xtium-CLHS PX4	OR-Y4S0-XPX70
For OEM clients, this manual in printed form, is available on request	OC-Y4HM-PUSR0

Xtium-CLHS PX4 Software

Item	Product Number
Sapera LT version 8.10 or later for full feature support (required but sold separately) 1. Sapera LT: Provides everything needed to build imaging application 2. Current Sapera compliant board hardware drivers 3. Sapera documentation: (compiled HTML help, Adobe Acrobat® (PDF)	OC-SL00-0000000
(optional) Sapera Processing Imaging Development Library includes over 600 optimized image-processing routines.	Contact Sales at Teledyne DALSA

Optional Xtium-CLHS PX4 Cables & Accessories

Item	Product Number
DH40-27S cable assembly to blunt end: 6 ft cable I/O 27 pin Hirose connector to blunt end. This cable assembly connects to J1.	OR-YXCC-27BE2M1, Rev B1
Cable set to connect to J4 Internal I/O Signals connector (J4: 26-pin SHF-113-01-L-D-RA)	see suggested cables
DH40-27S Connector Kit for Custom Wiring: Comprised of a DH40-27S connector plus screw lock housing kit	OR-YXCC-H270000
Cable assembly to connect to J5 (Board Sync) Connecting 2 boards Connection 3 or 4 boards	 OR-YXCC-BSYNC20 OR-YXCC-BSYNC40
Power interface cable required when supplying power to J1	OR-YXCC-PWRY00
CX4 Cable:	Contact Sales at Teledyne DALSA

About the Xtium-CLHS PX4 Frame Grabber

Series Key Features

- Compliant with Camera Link HS (CLHS) specification version 1.0 (M-Protocol) (visit http://www.visiononline.org/vision-standards.cfm for details on industry standards)
- Supports up to 7 lanes of 3.125 Gbps
- The specification defines a device discovery methodology that can be automated and which provides plug and play capability
- Camera Link HS cameras implement GenICam and associated GenCP, thus resulting in ease of use for Teledyne DALSA or third party cameras
- Uses a PCIe x4 Gen2 slot to maximize transfers to host computer buffers
- Acquire from Monochrome CLHS cameras, both area scan and linescan
- Output lookup tables (contact sales at Teledyne DALSA for availability)
- Vertical and Horizontal Flip supported on board
- External Input Triggers and Shaft Encoder inputs, along with Strobe outputs
- Supports Data Forwarding Mode, where camera image data is automatically transferred to one or more Xtium-CLHS boards (each installed in a separate computer), allowing distributed processing of the acquisition.
- Supports Multi-board Sync for trigger events, to simultaneously acquire from multiple cameras.
- Supports a number of acquisition events in compliance with "Teledyne DALSA's Trigger to Image Reliability"
- RoHS compliant

See Technical Specifications for detailed information.

User Programmable Configurations

Use the Xtium-CLHS PX4 firmware loader function in the Teledyne DALSA Device manager utility to select firmware for one of the supported modes. Firmware selection is made either during driver installation or manually later on (see Firmware Update: Manual Mode). Currently there is only one firmware version available:

- **Camera Link HS camera** (*installation default*):
  Support for 1 Camera Link HS camera, 8/10/12/14/16 bits per pixel, monochrome.

ACUPlus: Acquisition Control Unit

ACUPlus consists of a grab controller, one pixel packer, and one time base generator.

ACUPlus acquires variable frame sizes up to 64KB per horizontal line and up to 16 million lines per frame. ACUPlus can also capture an infinite number of lines from a line scan camera without losing a single line of data.

DTE: Intelligent Data Transfer Engine

The Xtium-CLHS PX4 intelligent Data Transfer Engine ensures fast image data transfers between the board and the host computer with zero CPU usage. The DTE provides a high degree of data integrity during continuous image acquisition in a non-real time operating system like Windows. DTE consists of intelligent DMA units with auto-loading Scatter-Gather tables.

PCI Express x4 Gen2 Interface

The Xtium-CLHS PX4 is a universal PCI Express x4 Gen2 board, compliant with the PCI Express 2.0 specification. The Xtium-CLHS PX4 board achieves transfer rates up to 1.8Gbytes/sec. to host memory. Note that performance can be lower depending on PC and/or programmed configuration.

The Xtium-CLHS PX4 board occupies one PCI Express x4 Gen2 expansion slot and one chassis opening.

Important:

- To obtain the maximum transfer rate to host memory, make sure the Xtium-CLHS PX4 is in a computer with a Gen2 slot. The board will work in a Gen1 slot, but only with half the possible transfer performance.
- The system motherboard BIOS should allow setting the PCIe maximum payload size to 256 or higher. Systems with fixed settings of 128 will limit performance for transfers to host memory.
- If the computer only has a PCI Express x16 slot, test directly or review the computer documentation to know if the Xtium-CLHS PX4 is supported. Computer motherboards may only support x16 graphic video board products in x16 slots.

Advanced Controls Overview

Visual Indicators

Xtium-CLHS PX4 features 2 LED indicators to facilitate system installation and setup (see Status LEDs). These indicators provide visual feedback on the board status and camera status.

External Event Synchronization

Trigger inputs and strobe signals precisely synchronize image captures with external events.

Camera Link HS Communication Port

A single Sapera LT Acquisition Device provides access to the Camera Link HS camera configuration via the board device driver. The communication port presents a seamless interface to access GenICam camera features.

Quadrature Shaft Encoder

An important feature for web scanning applications, the Quadrature Shaft Encoder inputs allow synchronized line captures from external web encoders (see J1- I/O Connector). The Xtium-CLHS PX4 provides a RS-422 or TTL (board revision B only, and mutually exclusive) input that supports a tick rate of up to 5MHz.

Development Software Overview

Sapera++ LT Library

Sapera++ LT is a powerful development library for image acquisition and control. Sapera++ LT provides a single API across all current and future Teledyne DALSA hardware. Sapera++ LT delivers a comprehensive feature set including program portability, versatile camera controls, flexible display functionality and management, plus easy to use application development wizards. Applications are developed using either C++ or .NET frameworks.

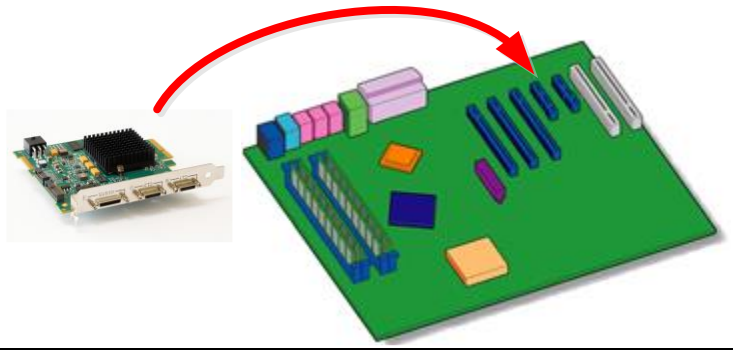
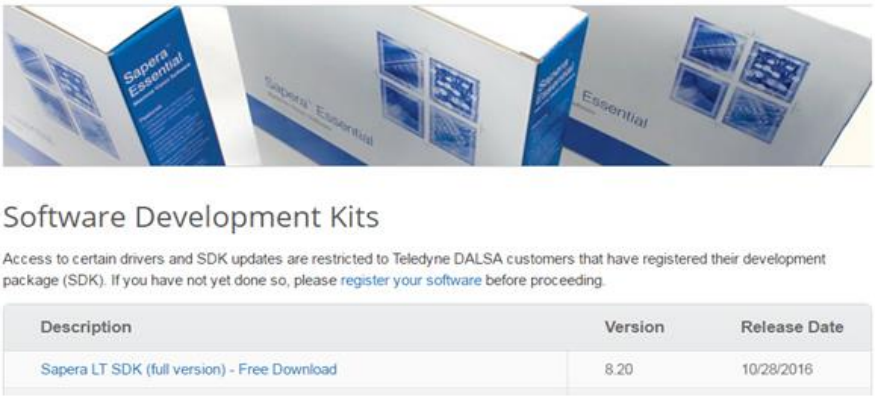
Sapera++ LT comes bundled with CamExpert, an easy to use camera configuration utility to create new, or modify existing camera configuration files.

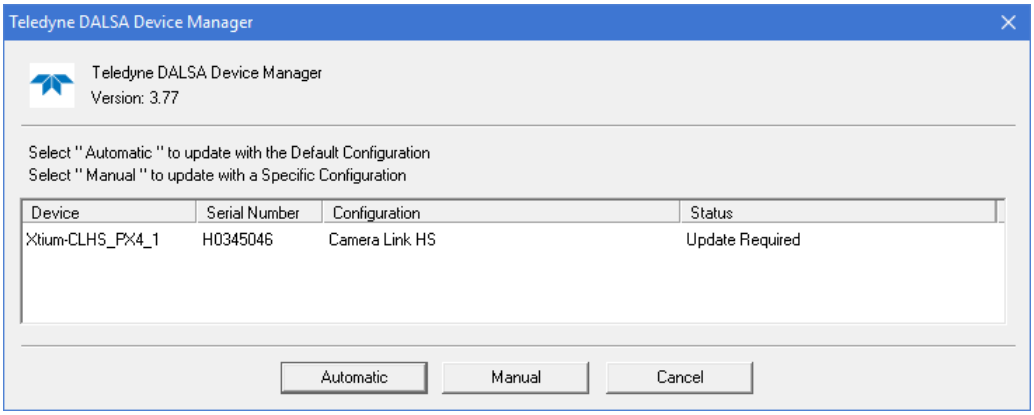
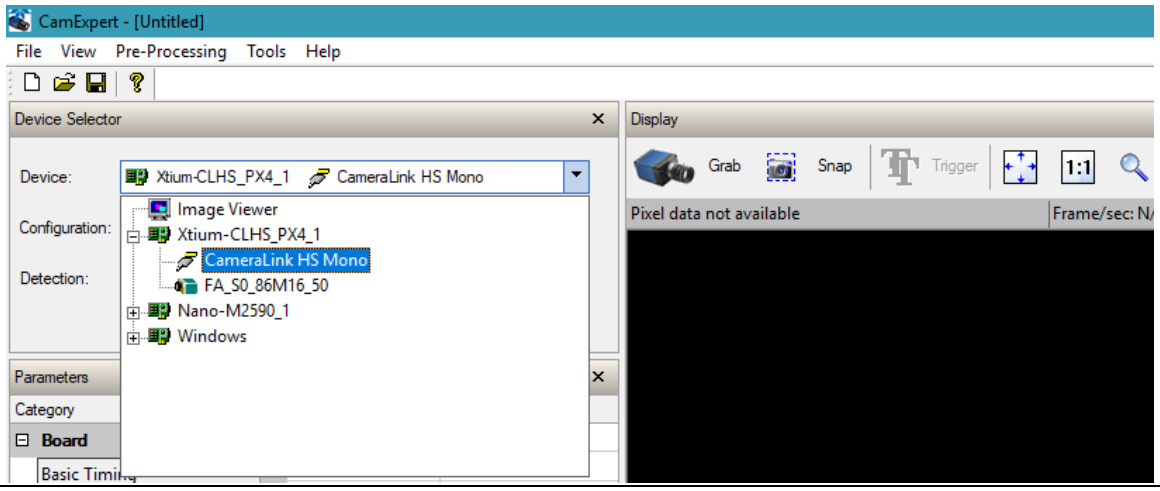
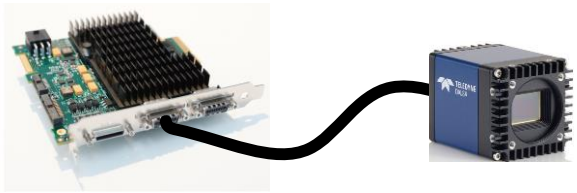
Sapera Processing Library

Sapera Processing is a comprehensive set of C++ classes or .NET classes for image processing and analysis. Sapera Processing offers highly optimized tools for image processing, blob analysis, search (pattern recognition), OCR and barcode decoding.

Quick Start Setup & Installation

The following procedure outlines the basic steps required to install the Teledyne DALSA Xtium-CLHS PX4. For complete installation details and information, see Installing Xtium-CLHS PX4.

1	Install the Xtium-CLHS PX4 in an available PCIe x4 slot on the host computer. 
2	Download and install the Sapera LT SDK software from the Teledyne DALSA website. http://teledynedalsa.com/imaging/support/downloads/sdks/ 
3	Download and install the Xtium-CLHS PX4 device driver from the Teledyne DALSA website. https://www.teledynedalsa.com/imaging/support/downloads/drivers/ 

4	To complete the installation, update the Xtium-CLHS PX4 firmware when prompted; select Automatic to update the firmware (only one firmware option is available, support for one Camera Link HS camera).  Reboot when all software and board drivers are installed.
5	Launch Sapera LT CamExpert to verify the installation; the board should be present in the list of available devices. 
6	Connect camera to the board Camera Link HS input connector. Ensure camera is properly powered. 

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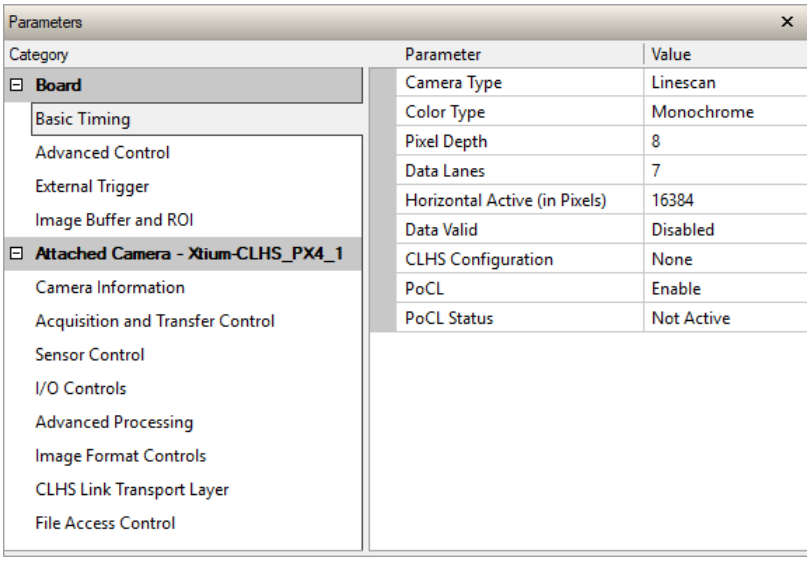
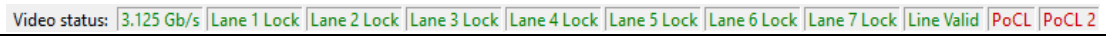
When CamExpert detects a camera (as per the CLHS device discovery protocol), camera parameters are displayed along with the board parameters.

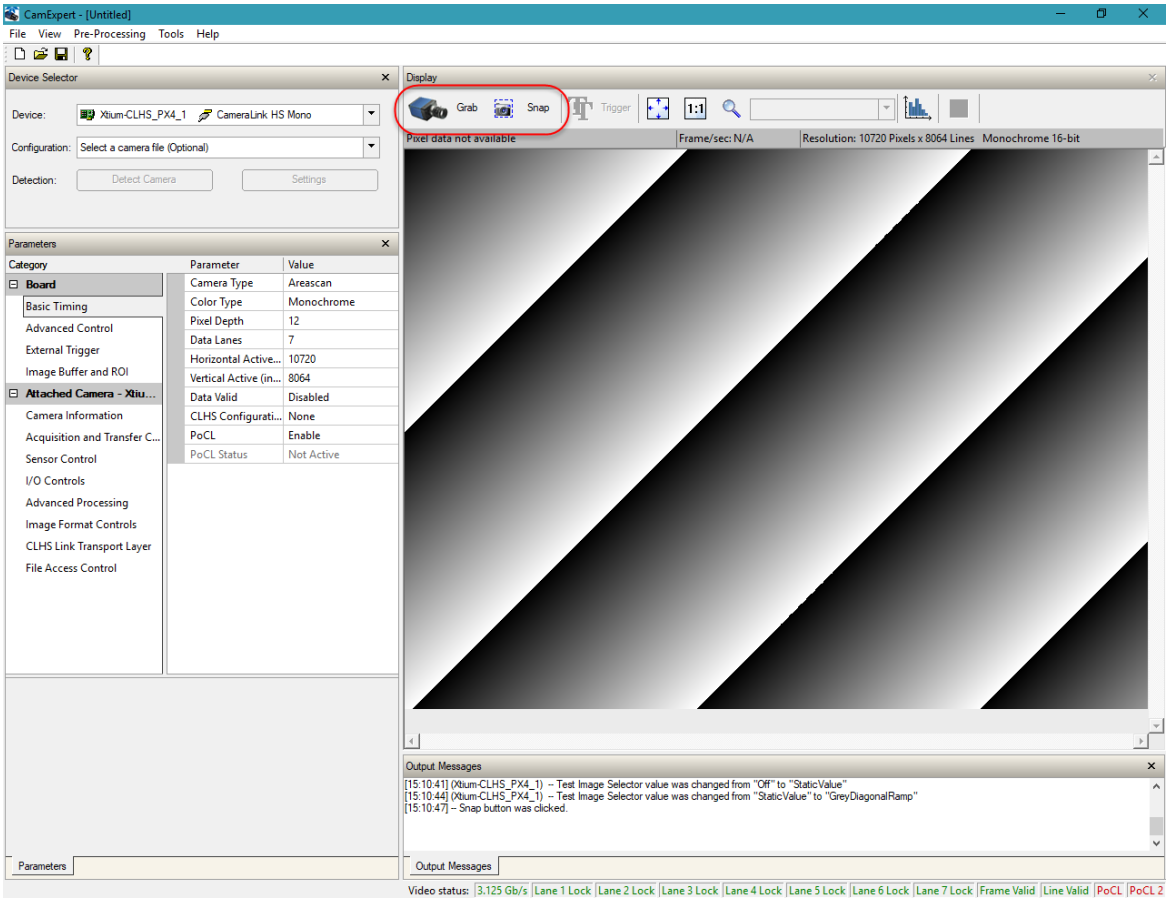


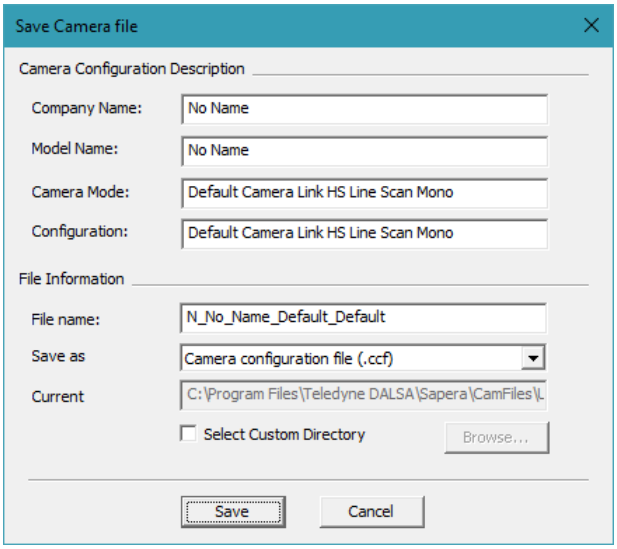
When properly connected, the video status bar displays camera signals in green.



8

Click Grab or Snap to acquire a test image to validate the setup.



9	Modify the board and camera parameters as necessary. When completed, save the camera configuration file.  The Xtium-CLHS PX4 can be configured using the the parameter settings in this file when using the Sapera LT API in your application to acquire images

Installing Xtium-CLHS PX4

Warning! (Grounding Instructions)

Static electricity can damage electronic components. Please discharge any static electrical charge by touching a grounded surface, such as the metal computer chassis, before performing any hardware installation. If you do not feel comfortable performing the installation, please consult a qualified computer technician.

Important: Never remove or install any hardware component with the computer power on. Disconnect the power cord from the computer to disable the power standby mode. This prevents the case where some computers unexpectedly power up when a board is installed.

Installation

The installation sequence is as follows:

- Install the board hardware into an available PCI Express x4 Gen2 slot.
- Turn on the computer.
- Install the Sapera LT Development Library or only its 'runtime library'.
- Install the Xtium-CLHS PX4 Sapera board driver.
- Update the board firmware if required.
- Reboot the computer.
- Connect a CLHS camera and test.

For information on performing a silent installation, refer to Appendix A: Silent Installation.
For troubleshooting installation problems, refer to Appendix B: Troubleshooting Problems.

Hardware Installation

- Turn the computer off, disconnect the power cord (disables power standby mode), and open the computer chassis to allow access to the expansion slot area.
- Install the Xtium-CLHS PX4 into a free PCI Express x4 Gen2 expansion slot (or an available x8 slot). Note that some computer's x16 slot may support boards such as the Xtium-CLHS PX4, not just display adapters.
- Connect a spare power supply connector to J7 when DC power is required on the external signals connector J1/J4. See Power Cable Assembly OR-YXCC-PWRY00 for information about an adapter for older computers.
- Close the computer chassis and turn the computer on.
- Logon to the computer as administrator or with an account that has administrator privileges.
- Connect a CLHS camera to J3 after installing Sapera as described below. Test with CamExpert.

Multi-board Data Forwarding Hardware Setup

- For distributed processing applications, see Data Forwarding Setup for information about data forwarding cabling with one to six Xtium-CLHS boards.

Multi-board Sync & I/O Setup

For multi-board sync applications, see J5: Multi-Board Sync / Bi-Directional General I/Os for information on using two to four Xtium-CLHS boards in one computer.

Sapera LT Library & Xtium-CLHS PX4 Driver Installation

Sapera LT SDK (full version), the image acquisition and control SDK for Teledyne DALSA cameras and frame grabbers is available for download from the Teledyne DALSA website:

http://teledynedalsa.com/imaging/support/downloads/sdks/

Run-time versions are also available for download at this location.

Software Development Kits

Access to certain drivers and SDK updates are restricted to Teledyne DALSA customers that have registered their development package (SDK). If you have not yet done so, please register your software before proceeding.

Description	Version	Release Date
Sapera LT SDK (full version) - Free Download	8.30	05/19/2017

	The Sapera LT SDK installation includes compiled demo and example programs, along with project source code, in both C++ and .NET languages, for most Microsoft Visual Studio development platforms. The Sapera LT ++ and Sapera LT .NET demo source code are found in the Sapera\Demos directory.

Refer to *Sapera LT User's Manual* for additional details about Sapera LT.

Teledyne DALSA Device Drivers

All Teledyne DALSA device drivers are available for download from the Teledyne DALSA website:

https://www.teledynedalsa.com/imaging/support/downloads/drivers/

Installation Procedure

- Sapera LT is installed before Teledyne DALSA board drivers.
- Download the Sapera LT SDK from the Teledyne DALSA website and run the executable file; the installation menu is presented.
- The installation program may prompt to reboot the computer. It is not necessary to reboot the computer between the installation of Sapera LT and the board driver.
- Download the Xtium-CLHS PX4 device driver from the Teledyne DALSA website and run the executable file; the installation menu is presented.
- During the late stages of the installation, the Xtium-CLHS PX4 firmware loader application starts.
- Reboot when all software and board drivers are installed.

	If Windows displays any unexpected message concerning the board, power off the system and verify the Xtium-CLHS PX4 is installed in the slot properly. You should also note the board's status LED color and compare it to the defined LED states as described in D1: Boot-up/PCIe Status LED.

Xtium-CLHS PX4 Firmware Loader

The Device Manager-Firmware Loader program automatically executes at the end of the driver installation and on every subsequent reboot of the computer. It will determine if the Xtium-CLHS PX4 requires a firmware update. If firmware is required, a dialog displays. This dialog also allows the user to load alternative firmware if available for the Xtium-CLHS PX4.

***Important*:** In the rare case of firmware loader errors please see Recovering from a Firmware Update Error.

Firmware Update: Automatic Mode

Click **Automatic** to update the Xtium-CLHS PX4 firmware. The **Xtium-CLHS PX4** currently supports one firmware configuration.

See User Programmable Configurations for details on all supported modes, selected via a manual update of alternative firmware.

With multiple Xtium-CLHS PX4 boards in the system, all are updated with new firmware. If any installed Xtium-CLHS PX4 board installed in a system already has the correct firmware version, an update is not required. In the following screen shot a single Xtium-CLHS PX4 board is installed and ready for a firmware upgrade.

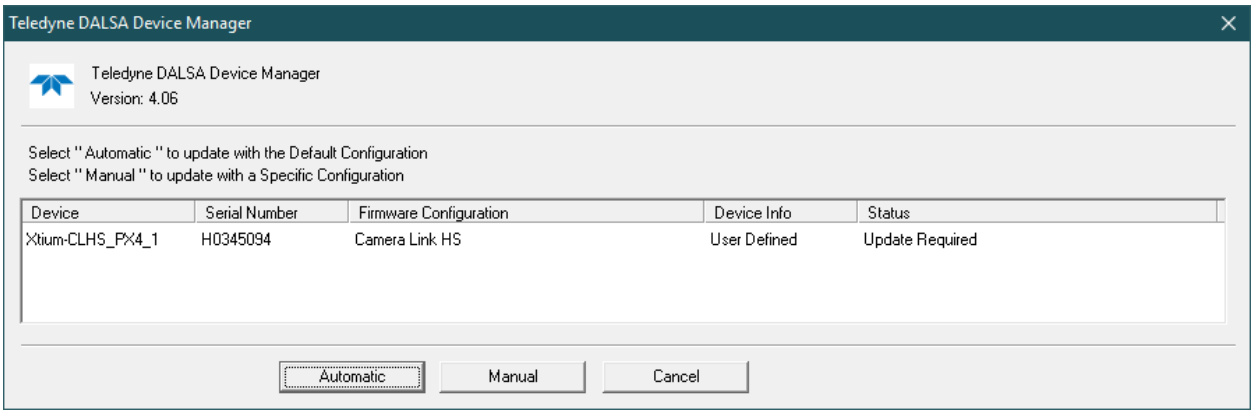


Figure 1: Automatic Firmware Update

Firmware Update: Manual Mode

Select **Manual** mode to load firmware other than the default version or when, in the case of multiple Xtium-CLHS PX4 boards in the same system, if each requires different firmware.

The following figure shows the Device Manager manual firmware screen. Displayed is information on all installed Xtium-CLHS PX4 boards, their serial numbers, and their firmware components.

Do a manual firmware update as follows:

- Select the Xtium-CLHS PX4 to update via the board selection box (if there are multiple boards in the system).
- Click on the Start Update button.
- Observe the firmware update progress in the message output window.
- Close the Device manager program when the device reset complete message is shown.

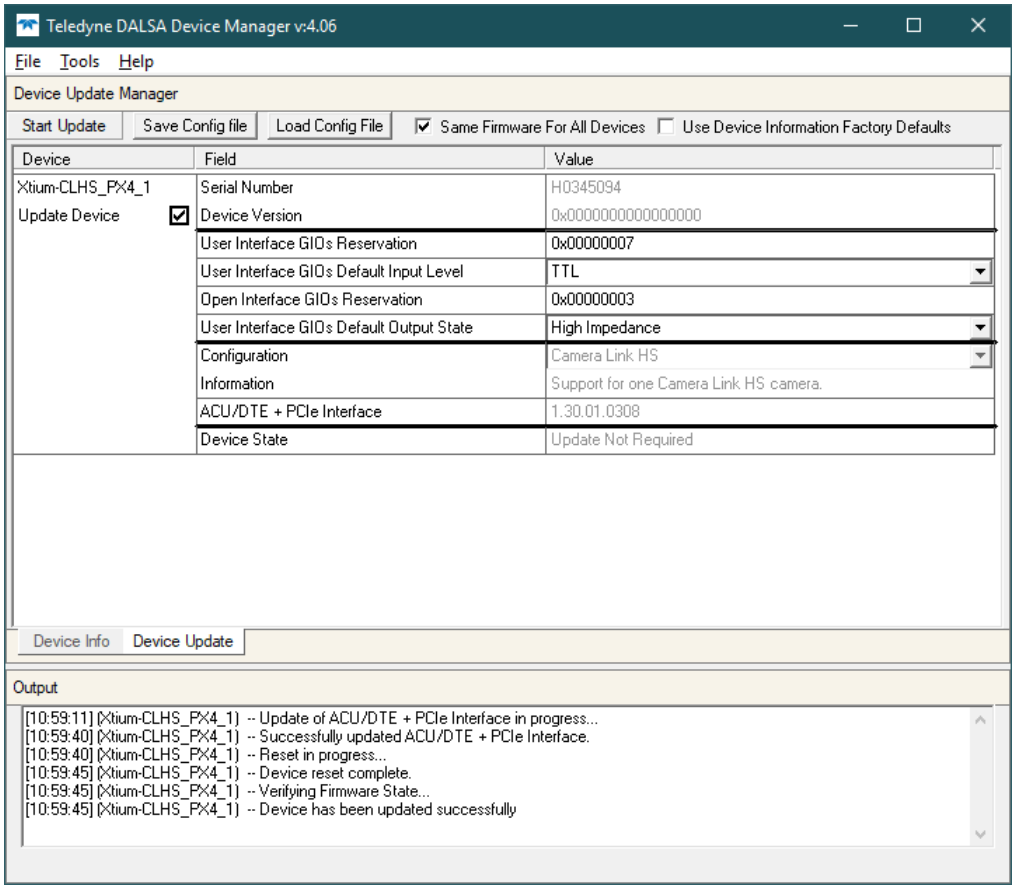


Figure 2: Manual Firmware Update

Executing the Firmware Loader from the Start Menu

If required, the Xtium-CLHS PX4 Firmware Loader program is executed via the Windows Start Menu shortcut **Start ● Programs ● Teledyne DALSA ● Xtium-CLHS PX4 Driver ● Firmware Update**.

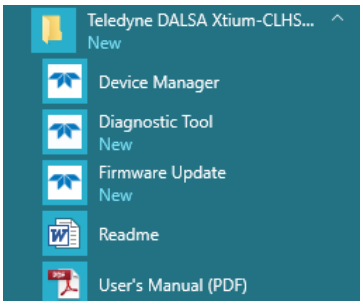


Figure 3: Start Menu Firmware Update Shortcut

A firmware change after installation is required to select a different configuration mode, if available; see User Programmable Configurations.

Upgrading Sapera or Board Driver

When installing a new version of Sapera or a Teledyne DALSA acquisition board driver in a computer with a previous installation, the current version **must** be un-installed first. Described below are two upgrade situations. Note that if the board is installed in a different slot, the new hardware wizard opens. Answer as instructed in section Installation.

Board Driver Upgrade Only

Minor upgrades to acquisition board drivers are distributed as ZIP files available in the Teledyne DALSA web site http://www.teledynedalsa.com/en/support/options/.

Often minor board driver upgrades do not require a new revision of Sapera. To confirm that the current Sapera version will work with the new board driver:

- Check the new board driver ReadMe file before installing, for information on the minimum Sapera version required.
- If the ReadMe file does not specify the Sapera version required, contact Teledyne DALSA Technical Support (see Technical Support).

To upgrade the board driver only:

- Logon the computer as an administrator or with an account that has administrator privileges.
- In **Windows 7**, from the start menu select **Start ● Settings ● Control Panel ● Programs and Features**. Double-Click the Teledyne DALSA Xcelera board driver and click **Remove**.
- In **Windows 8 & Windows 10**, just type Control Panel while in the start screen, or click the arrow in the lower left side to bring up the all applications window. Select Programs and Features, then double-click the Teledyne DALSA Xtium CLHS PX4 board driver and click **Remove**.
- Install the new board driver. Run **Setup.exe** if installing manually from a downloaded driver file.

Important: You cannot install a Teledyne DALSA board driver without Sapera LT installed on the computer.

Upgrading both Sapera and Board Driver

When upgrading both Sapera and the acquisition board driver, follow the procedure described below.

- Logon the computer as an administrator or with an account that has administrator privileges.
- In **Windows 7**, from the start menu select **Start ● Settings ● Control Panel ● Programs and Features**. Double-click the Teledyne DALSA Xcelera board driver and click **Remove**. Follow by also removing the older version of Sapera LT.
- In **Windows 8 & Windows 10**, just type Control Panel while in the start screen, or click the arrow in the lower left side to bring up the all applications window. Select Programs and Features, then double-click the Teledyne DALSA Xtium CLHS PX4 board driver and click **Remove**. Follow by also removing the older version of Sapera LT.
- Reboot the computer and logon the computer as an administrator again.
- Install the new versions of Sapera and the board driver as if this was a first time installation. See Sapera LT Library & Xtium-CLHS PX4 Driver Installation for installation procedures.

Preserving Board Parameters During Driver Upgrade

User defined parameter settings for previously installed boards can be preserved when upgrading a device driver by using an *install.ini* file as described in the Custom Driver Installation Using install.ini section. Clicking **Automatic** on the Device Manager start-up dialog will apply the settings specified in the *install.ini* file.

To verify the settings specified in the *install.ini* file, click **Manual**; differences between the current device settings are shown in green in both the Device Info and Device Update tabs.

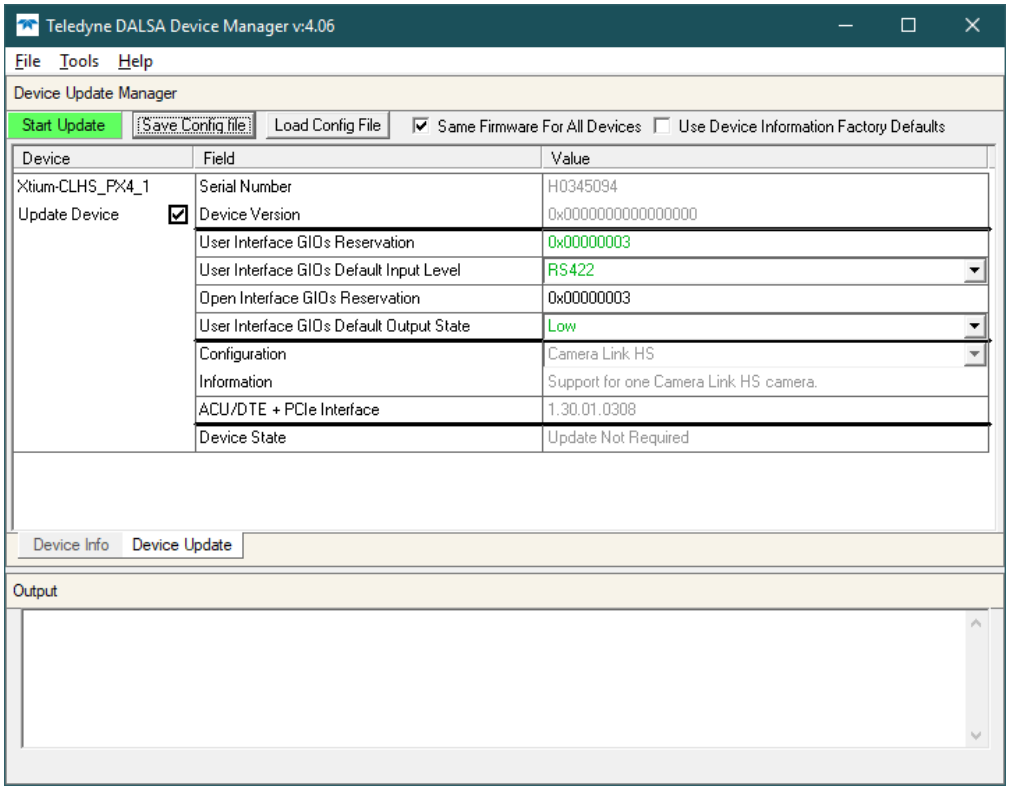


Figure 4: Device Manager Parameter Setting Differences

Upgrading without an *install.ini* file requires selecting **Manual** update on the Device Manager start-up dialog and setting the required parameters manually.

	**Note:** Without an *install.ini, c*onfiguration information is not preserved and is always set to factory default.

Preserving Board Parameters during Board Replacement or System Cloning

When replacing a board in a system or cloning a system configuration using a harddrive image, if the previous device parameter settings differ from the factory default driver settings it is indicated as "User Defined" or "Manual Configuration" in the Teledyne DALSA Device Manager start-up dialog under the Device Info column. User-defined settings are specific to the PCI Express slot on the system.

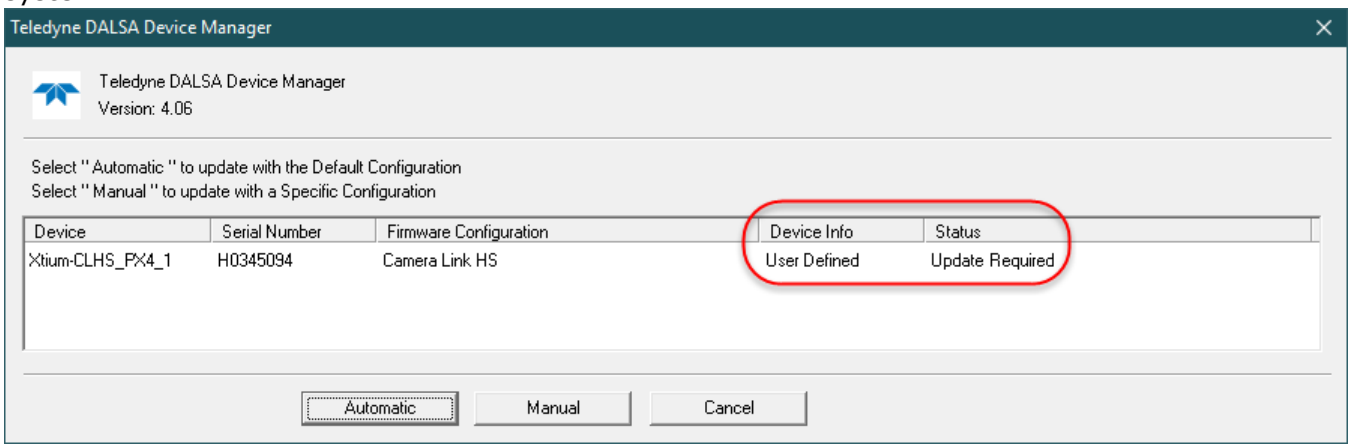


Figure 5: Firmware Update Status

To preserve the user defined parameter settings, select "Manual" and proceed with the update; differences between the current settings are shown in green in both the Device Info and Device Update tabs.

For systems with mulitple boards, if boards use different firmware configurations, disable the **Same Firmware For All Devices** option (otherwise the configuration specified for the first board according to slot position is applied to all boards in the system).

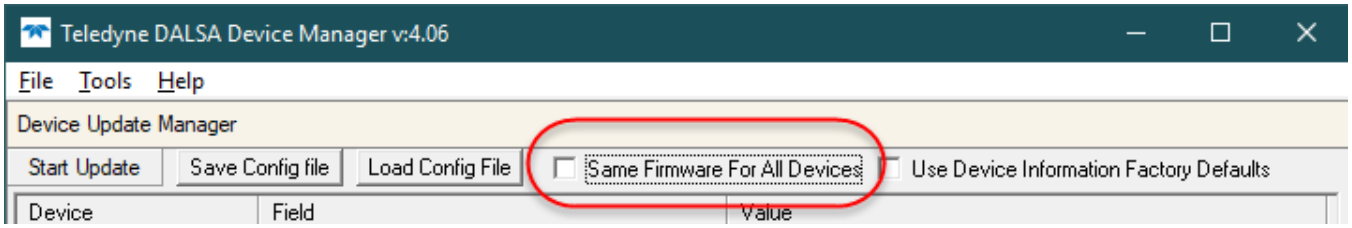


Figure 6: Same Firmware For All Devices Checkbox

Displaying Xtium-CLHS PX4 Board Information

The Device Manager program also displays information about the Xtium-CLHS PX4 boards installed in the system. To view board information run the program via the Windows Start Menu shortcut **Start ● Programs ● Teledyne DALSA ● Xtium-CLHS PX4 Device Driver ● Device Manager**.

Device Manager – Board Viewer

The following screen image shows the Device Manager program with the Information/Firmware tab active. The left window displays all Teledyne DALSA boards in the system and their individual device components. The right window displays the information stored in the selected board device. This example screen shows the Xtium-CLHS PX4 board information.

Generate the Xtium-CLHS PX4 device manager report file (BoardInfo.txt) by clicking **File ● Save Device Info**. Teledyne DALSA Technical Support may request this report to aid in troubleshooting installation or operational problems.

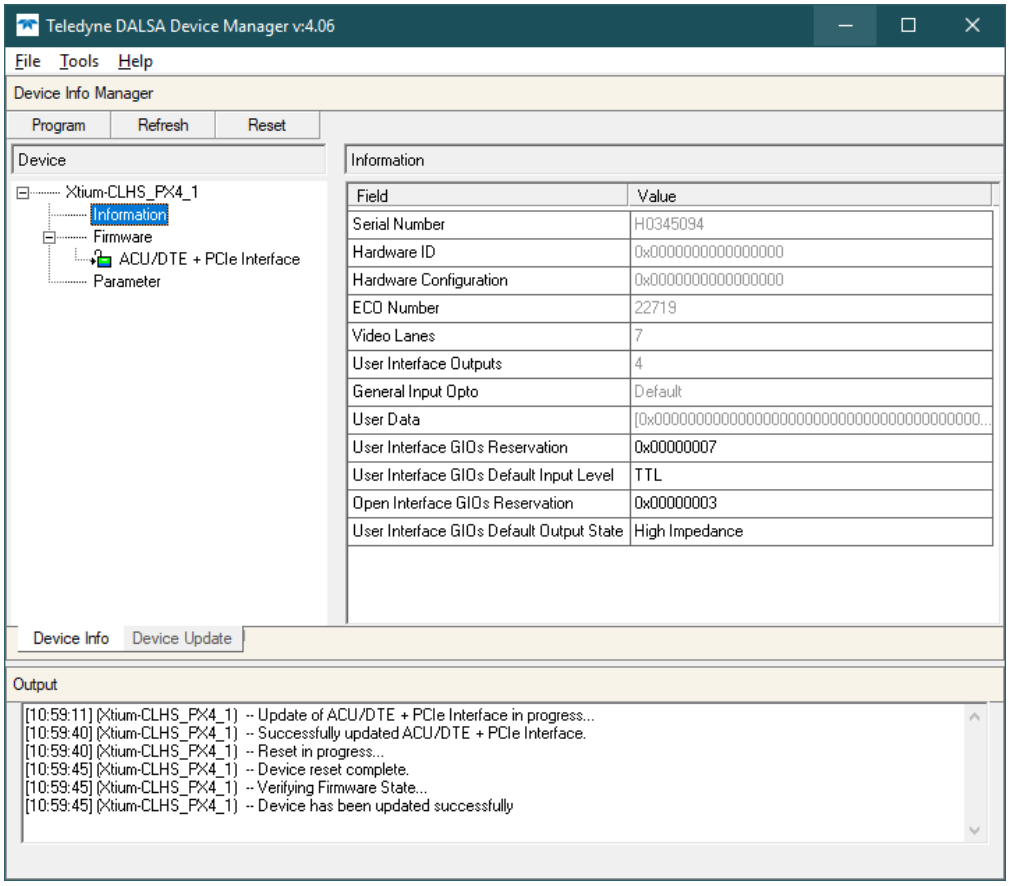
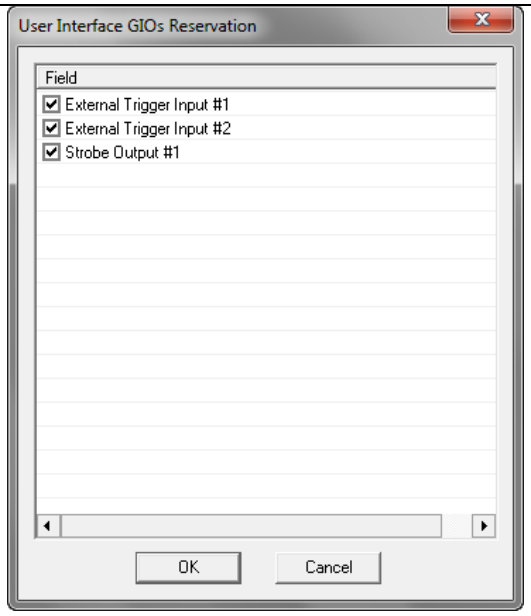
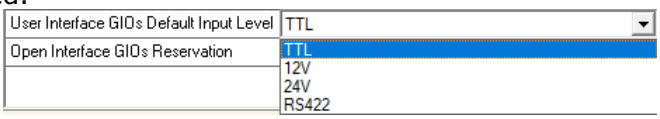
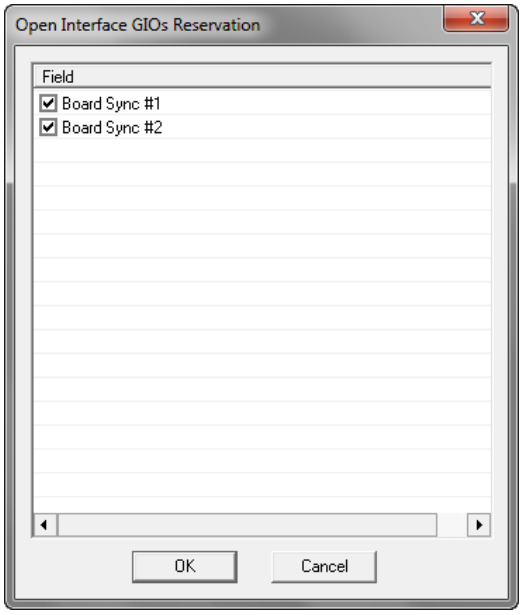
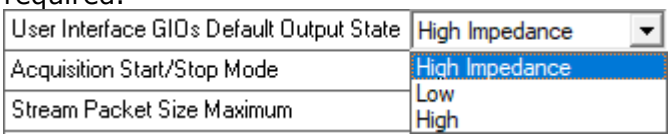


Figure 7: Board Information via Device Manager

Information Field Description

Field	Description
Serial Number	[Read-Only]: Serial Number of the board
Hardware ID	[Read-Only]: This field identifies hardware changes that affect the operation of the board. Possible values are: • **0x0000000000000000**: Rev A3 • **0x0000000000110001**: Rev B1
Hardware Configuration	[Read-Only]: This field will state the presence or absence of optional components. Possible values are: • **0x0000000000000100**: Rev A3 • **0x0000000000000101:** Rev B1 **Bit 0:** Both Shaft Encoder RS-422 and TTL input is supported. **Bit 8:** Backup FPGA supports stripping CRC from PCIe packet
ECO Number	[Read-Only]: Indicates the last Engineering Change Order applied to the board. **Note**: For boards shipped with driver 1.10 and below, this entry will show 0.
Video Lanes	[Read-Only]: Indicates the maximum number of video lanes supported by the board. For this board, the value is 7. **Note**: For boards shipped with driver 1.00, this entry will show 0.
User Interface Outputs	[Read-Only]: Number of available user interface outputs on the board. Possible values are: • **4**: Rev A3 • **8**: Rev B. **Note**: For boards Rev A3 shipped with driver 1.10 and earlier, this entry will show 0.
General Input Opto	[Read-Only]: Type of opto-coupler on the board. Possible values are: • TLP130 (Default) • **Note**: Boards shipped with driver 1.11 or earlier; 1.30 and later will show Default.
User Data	[Read/Write]: This is a 64 byte general purpose user storage area. For information on how to read/write this field at the application level, contact Teledyne DALSA Technical Support.
User Interface GIOs Reservation	[Read/Write]: Use this field to reserve User Interface GIOs for use by the acquisition module. By default, boards are shipped with User Interface General Inputs 1 & 2 reserved for External Triggers and User Interface General Output 1 reserved for Strobe Output. Click on the 'Value' field to open the dialog box show below. Disable any GIO reservations that are not required. Click the OK button to update the value field.

	 By default, boards are shipped with User Interface General Inputs 1 & 2 reserved for External Triggers and User Interface General Output 1 reserved for Strobe Outputs.
User Interface GIOs Default Input Level	[Read/Write]: Use this field to select the default input level of the User Interface GIOs. Click on the 'Value' field to select the input signal level detection required.  By default, boards are shipped with User Interface General Inputs set to 24V. Note that the input level can also be modified at the application level.

Open Interface GIOs Reservation	[Read/Write]: Use this field to reserve Open Interface GIOs for use by the acquisition module. To specify the open interface GIO reservations, click on the 'Value' field. Disable any GIO reservations that are not required. Click OK to update the value field.  By default, boards are shipped with Open Interface GIOs 1 & 2 reserved for Board Sync 1 &
User Interface GIOs Default Output State	[Read/Write]: Use this field to select the default Output State of the User Interface GIOs. Click on the 'Value' field to select the input signal level detection required.  By default, boards are shipped with User Interface General Outputs set to High Impedance. Note that the output state can also be modified at the application level.

Device Information Report

Teledyne DALSA Technical Support may request device information report to aid in troubleshooting installation or operational problems. Generate the Xtium-CLHS PX4 device manager report file (BoardInfo.txt) by clicking **File ● Save Device Info**.

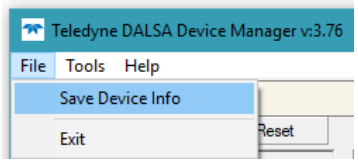


Figure 8: Device Manager File Menu Save Device Info Command

Configuring Sapera

Viewing Installed Sapera Servers

The Sapera configuration program (**Start • Programs • Teledyne DALSA • Sapera LT • Sapera Configuration**) allows the user to see all available Sapera servers for the installed Sapera-compatible boards. The **System** entry represents the system server. It corresponds to the host machine (your computer) and is the only server that should always be present.

Increasing Contiguous Memory for Sapera Resources

The **Contiguous Memory** section lets the user specify the total amount of contiguous memory (a block of physical memory, occupying consecutive addresses) reserved for the resources needed for **Sapera buffers** allocation and **Sapera messaging**. For both items, the **Requested** value dialog box shows the 'CorMem' driver default memory setting while the **Allocated** value displays the amount of contiguous memory allocated successfully. The default values will generally satisfy the needs of most applications.

The **Sapera buffers** value determines the total amount of contiguous memory reserved at boot time for the allocation of dynamic resources used for frame buffer management such as scatter-gather list, DMA descriptor tables plus other kernel needs. Adjust this value higher if your application generates any out-of-memory error while allocating host frame buffers or when connecting the buffers via a transfer object. You can approximate the worst-case scenario amount of contiguous memory required as follows:

- Calculate the total amount of host memory used for one frame buffer [number of pixels per line • number of lines • (2 - *if buffer is 10/12/14 or 16 bits*)].
- Provide 200 bytes per frame buffer for Sapera buffer resources.
- Provide 64 bytes per frame buffer for metadata. Memory for this data is reserved in chunks of 64kB blocks.
- Provide 48 bytes per frame buffer for buffer management. Memory for this data is reserved in chunks of 64kB blocks.
- For each frame buffer DMA table, allocate 24 bytes + 8 bytes for each 4kB of buffer. For example, for a 120x50x8 image: 120x50 = 6000 = 1.46 4kB blocks -> roundup to 2 4kB blocks. Therefore 24 bytes + (2 * 8 bytes) = 40 bytes for DMA tables per frame buffer. Memory for this data is reserved in chunks of 64kB blocks. If vertical flipping is enabled, one must add 16 bytes per line per buffer. For example, for an image 4080x3072 image: 16 bytes * 3072 = 49152 bytes.
- Note that Sapera LT reserves the 1st 5MB for its own resources, which includes the 200 bytes per frame buffer mentioned above.
- Test for any memory error when allocating host buffers. Simply use the Buffer menu of the Sapera Grab demo program (see Grab Demo Overview) to allocate the number of host buffers required for your acquisition source. Feel free to test the maximum limit of host buffers possible on your host system – the Sapera Grab demo will not crash when the requested number of host frame buffers is not allocated.
- The following calculation is an example of the amount of contiguous memory to reserve beyond 5MB with 80,000 buffers of 2048x1024x8:
  a) (80000 * 64 bytes)
  b) (80000 * 48 bytes)
  c) (80000 * (24 + (((2048*1024)/4kB) * 8))) = 323MB
  d) Total = a (rounded up to nearest 64kB) + b (rounded up to nearest 64kB) + c (rounded up to nearest 64kB).

Host Computer Frame Buffer Memory Limitations

When planning a Sapera application and its host frame buffers used, plus other Sapera memory resources, do not forget the Windows operating system memory needs.

A Sapera application using the preferred *scatter gather buffers* could consume most of the remaining system memory, with a large allocation of frame buffers. If using frame buffers allocated as a *single contiguous memory block*, Windows will limit the allocation dependent on the installed system memory. Use the Buffer menu of the Sapera Grab demo program to allocate host buffer memory until an error message signals the limit allowed by the operating system used.

Contiguous Memory for Sapera Messaging

The current value for **Sapera messaging** determines the total amount of contiguous memory reserved at boot time for messages allocation. This memory space stores arguments when a Sapera function is called. Increase this value if you are using functions with large arguments, such as arrays and experience any memory errors.

CamExpert Quick Start

Interfacing CLHS Cameras with CamExpert

CamExpert is the camera-interfacing tool for Teledyne DALSA frame grabber boards supported by the Sapera library. CamExpert is the primary tool to configure, test and calibrate your camera and imaging setup. Display tools include, image pixel value readout, image zoom, and histogram.

An important component of CamExpert is its live acquisition display window which allows immediate verification of timing or control parameters without the need to run a separate acquisition program.

After CamExpert identifies the camera (as per the Camera Link device discovery protocol), timing parameters are displayed and the user can test image acquisition by clicking on *Grab*.

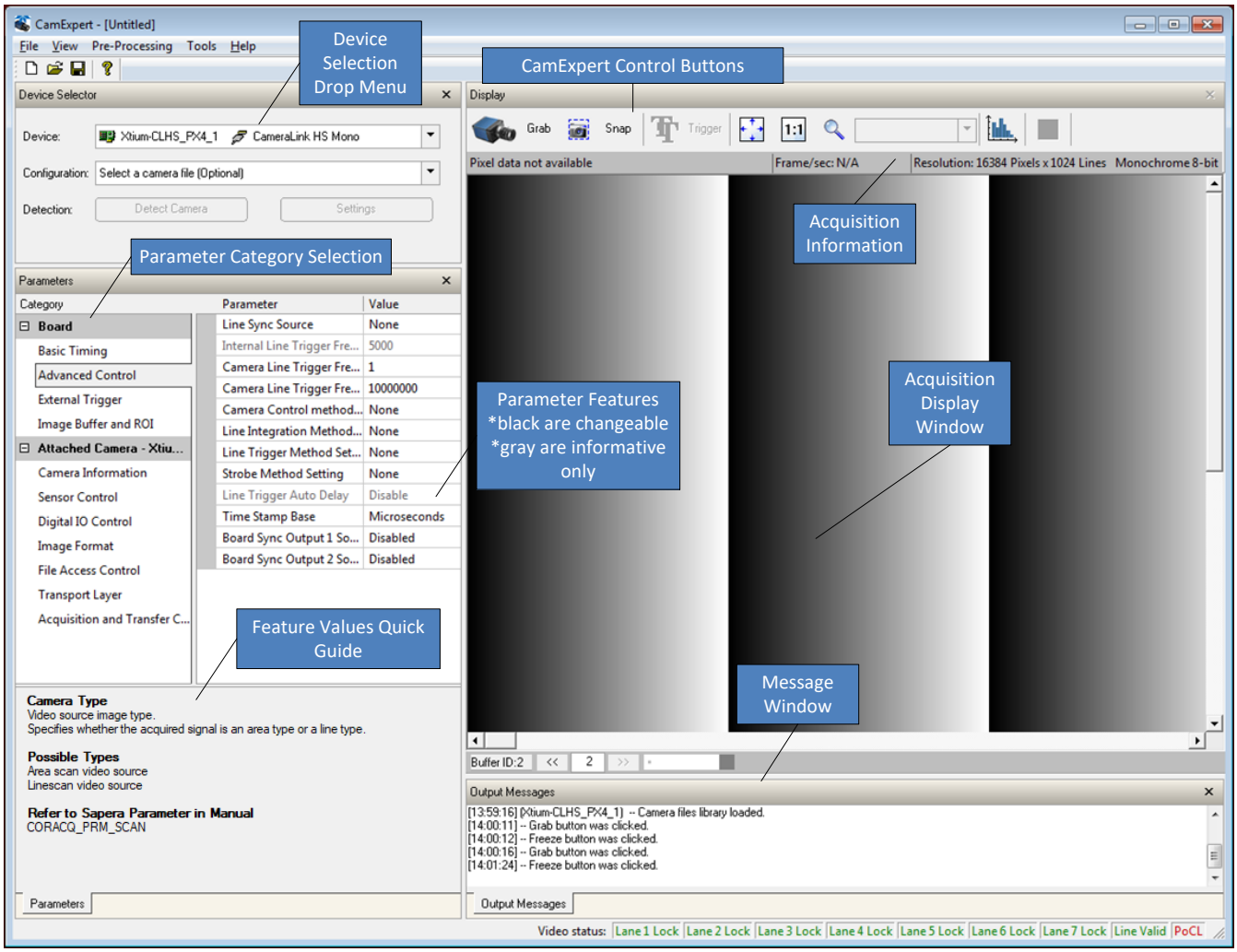
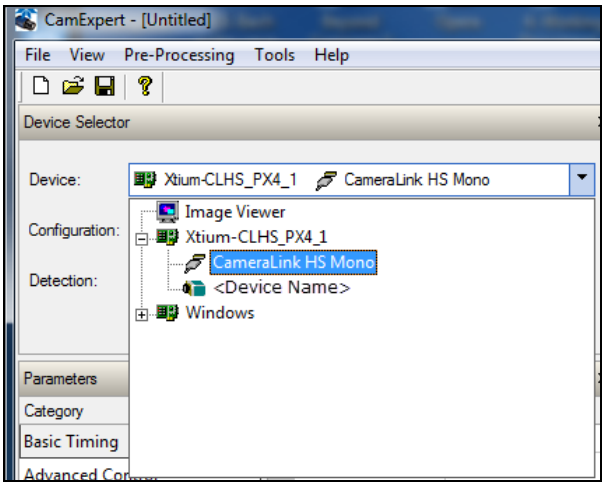


Figure 9: CamExpert Program

CamExpert groups camera features into functional categories. The features shown depend on the frame grabber used and what camera is connected. The values are either the camera defaults or the last stored value when the camera was used. The general descriptions below are not specific to a particular camera.

- **Device Selector:** Two drop menus allow selection of which device and which saved configuration to use.
  - **Device:** Select which acquisition device to control and configure a camera file. Required in cases where there are multiple boards in a system and when one board supports multiple acquisition types. Note in this example, the installed Xtium-CLHS PX4 has firmware to support a monochrome Camera Link HS camera.



  - **Configuration:** Select the timing for a specific camera model included with the Sapera installation or a standard video standard. The *User's* subsection is where user created camera files are stored.

- **Parameter Groups:** Select a function category and change parameter values as required. Descriptions for the camera parameters change dependent on the camera.
  - **Basic Timing:** Provides or change static camera parameters.
  - **Advanced Controls:** Advanced parameters used to select various integration methods, frame trigger type, Camera Link HS controls, etc.
  - **External Trigger:** Parameters to configure the external trigger characteristics.
  - **Image Buffer and ROI:** Allows control of the host buffer dimension and format.

- **Display:** An important component of CamExpert is its live acquisition display window, which allows immediate verification of timing or control parameters without the need to run a separate acquisition program. **Grab** starts continuous acquisition (button then toggles to **Freeze** to stop). **Snap** is a single frame grab. **Trigger** is a software trigger to emulate an external source.
- **Output Messages and Video Status Bar:** Events and errors are logged for review. Camera connection status is displayed where green indicates connected signals present.

The CamExpert tool is described more fully in the Sapera Getting started and Sapera Introduction manuals.

Sapera Camera Configuration Files

CamExpert generates the Sapera camera configuration file (*yourcamera.ccf*) based on timing and control parameters entered. When using the Sapera LT API in your imaging application, the frame grabber parameter settings can be loaded from this file. For backward compatibility with previous versions of Sapera, CamExpert also reads and writes the *.cca and *.cvi camera parameter files.

Every Sapera demo program starts with a dialog window to select a camera configuration file (for details on the included demos, see the Sapera Demo Applications section). Even when using the Xtium-CLHS PX4 with common video signals, a camera file is required. Therefore, CamExpert is typically the first Sapera application run after an installation. Existing .ccf files can be copied to any new board installations when similar cameras are used.

Camera Types & Files

The Xtium-CLHS PX4 supports digital area scan or line scan cameras using the Camera Link HS interface standard. Browse our web site [http://www.teledynedalsa.com/imaging/] for the latest information on Teledyne DALSA Camera Link HS cameras.

Camera Files Distributed with Sapera

The Sapera distribution includes camera files for a selection of Xtium-CLHS PX4 supported cameras. Using the Sapera CamExpert program, you may use the camera files (CCA) provided to generate a camera configuration file (CCF) that describes the desired camera and frame grabber configuration..

Teledyne DALSA continually updates a camera application library composed of application information and prepared camera files. Camera files are ASCII text, readable with Windows Notepad on any computer without having Sapera installed.

Overview of Sapera Acquisition Parameter Files (*.ccf or *.cca/*.cvi)

Concepts and Differences between the Parameter Files

There are two components to the legacy Sapera acquisition parameter file set: CCA files (also called cam-files) and CVI files (also called VIC files, i.e. video input conditioning). The files store video-signal parameters (CCA) and video conditioning parameters (CVI), which in turn simplifies programming the frame-grabber acquisition hardware for the camera in use. **Sapera LT 5.0** introduces a new camera configuration file (**CCF**) that combines the CCA and CVI files into one file.

Typically, a camera application will use a CCF file per camera operating mode (or one CCA file in conjunction with several CVI files, where each CVI file defines a specific camera-operating mode). An application can also have multiple CCA/CCF files to support different image format modes supported by the camera or sensor (such as image binning or variable ROI).

CCF File Details

A file using the ".CCF" extension, (Camera Configuration files), is the camera (CCA) and frame grabber (CVI) parameters grouped into one file for easier configuration file management. This is the default Camera Configuration file used with Sapera LT 5.0 and the CamExpert utility.

CCA File Details

Teledyne DALSA distributes camera files using the legacy ".CCA" extension, (CAMERA files), which contain all parameters describing the camera video signal characteristics and operation modes (what the camera outputs). The Sapera parameter groups within the file are:

- Video format and pixel definition
- Video resolution (pixel rate, pixels per line, lines per frame)
- Synchronization source and timing
- Channels/Taps configuration
- Supported camera modes and related parameters
- External signal assignment

CVI File Details

Legacy files using the ".CVI" extension contain all operating parameters related to the frame grabber board - what the frame grabber can actually do with camera controls or incoming video. The Sapera parameter groups within the file are:

- Activate and set any supported camera control mode or control variable.
- Define the integration mode and duration.
- Define the strobe output control.
- Allocate the frame grabber transfer ROI, the host video buffer size and buffer type (RGB888, RGB101010, MONO8, and MONO16).
- Configuration of line/frame trigger parameters such as source (internal via the frame grabber /external via some outside event), electrical format (TTL, RS-422, OPTO-isolated), and signal active edge or level characterization.

Saving a Camera File

Use CamExpert to save a camera file (*.ccf) usable with any Sapera demo program or user application. An example would be a camera file, which sets up parameters for a free running camera (i.e. internal trigger) with exposure settings for a good image with common lighting conditions.

When CamExpert is setup as required, click on **File•Save As** to save the new .ccf file. The dialog that opens allows adding details such as camera information, mode of operation, and a file name for the .ccf file.

Camera Interfacing Check List

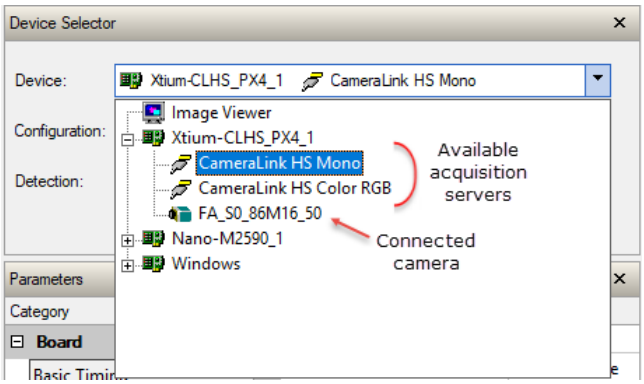
Before interfacing a camera from scratch with CamExpert:

- Confirm that Teledyne DALSA has not already published an application note with camera files [www.teledynedalsa.com].
- Confirm that the correct version or board revision of Xtium-CLHS PX4 is used. Confirm that the required firmware is loaded into the Xtium-CLHS PX4.
- Confirm that Sapera does not already have a .cca file for your camera installed on your hard disk. If there is a .cca file supplied with Sapera, then use CamExpert to generate the .ccf file with default parameter values matching the frame grabber capabilities.
- Check if the Sapera installation has a similar type of camera file. A similar .cca file can be loaded into CamExpert and modified to match timing and operating parameters for your camera, and lastly save them as Camera Configuration file (.ccf).
- Finally, if there is no file for your camera, run CamExpert after installing Sapera and the acquisition board driver, select the board acquisition server, and manually enter the camera parameters.

Using CamExpert with Xtium-CLHS PX4

The Sapera CamExpert tool is the interfacing tool for Xtium-CLHS PX4 frame grabbers and connected cameras; it is supported by the Sapera library and hardware. CamExpert allows a user to test frame grabber and camera functions. Additionally CamExpert saves the frame grabber settings configuration as individual camera parameter files on the host system (*.ccf).

When an acquisition server is selected, CamExpert only presents parameters supported by the selected device.



The Xtium-CLHS PX4 firmware supports one Camera Link HS camera and provides the following acquisition server:

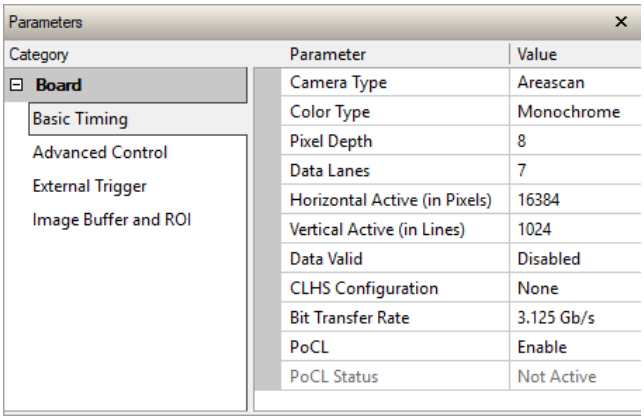
Firmware	Acquisition Servers
Camera Link HS (default configuration)	Xtium-CLHS_PX4_1 CameraLink HS Mono

Depending on the selected server, different parameters may be displayed.

For more information, see the Sapera Servers and Resources section.

Basic Timing Category

The Basic Timing category groups parameters such as camera type, the active image size, and other settings related to basic timing.



Parameter Descriptions

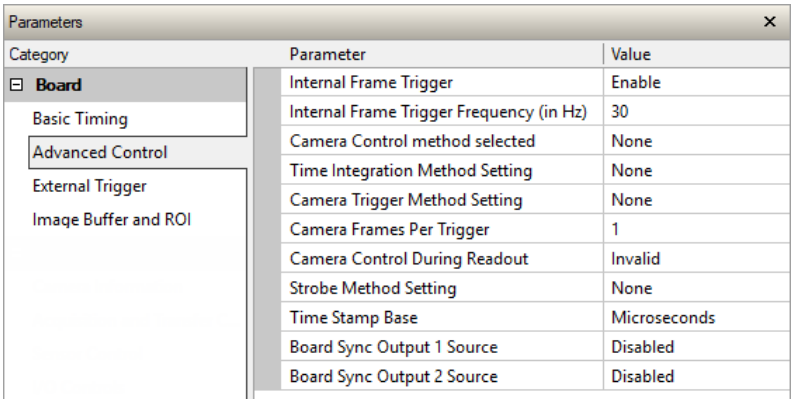
The following table describes the CamExpert Basic Timing category of Sapera LT parameters. Acquisition server notes, if applicable, indicate if parameter availablility or supported values are dependent on the selected frame grabber acquisition server and acquisition device.

Display Name	Parameter	Description	Notes
Camera Type	CORACQ_PRM_SCAN	Video source image type. Possible values are areascan or line scan.	Not shown for Bayer servers (areascan only).
Color Type	CORACQ_PRM_VIDEO	Sets the color format of the input source.	Not shown for RGB servers. Monochrome servers support: Monochrome Bayer mosaic
Pixel Depth	CORACQ_PRM_PIXEL_DEPTH	Pixel depth (bits per pixel) of the input source.	Not shown for RGB servers. Monchrome servers support: 8, 10, 12, 14 or 16 bit
Data Lanes	CORACQ_PRM_DATA_LANES	Number of data lanes output by the camera.	
Horizontal Active (in Pixels)	CORACQ_PRM_HACTIVE	Sets the horizontal camera resolution in pixels. This corresponds to the visible part of the image from the camera. Valid range is: min = 32 pixel max = 16384 pixel step = 32 pixel Note: minimum is per lane	
Vertical Active (in Lines)	CORACQ_PRM_VACTIVE	Sets the vertical camera resolution in lines per frame. This corresponds to the visible part of the image from the camera. Valid range is 1-16777215.	Not shown for linescan cameras.
Data Valid	CORACQ_PRM_DATA_VALID_ENABLE	Specifies if the acquisition board uses the camera data valid signal. Boolean parameter (TRUE or FALSE).	
CLHS Configuration	CORACQ_PRM_CLHS_CONFIGURATION	Sets the board's CLHS configuration. Possible values are: None Camera Port Slave Manual Acquisition Start/Stop	

Bit Transfer Rate	CORACQ_PRM_BIT_TRANSFER_RATE	Specifiies the bit transfer rate. Possible values are: 3.125 Gb/s 5.0 Gb/s	
PoCL	CORACQ_PRM_POCL_ENABLE	Enables/disables sending power through the Camera Link CLHS cable for Active Optical Cable (AOC). Boolean parameter (TRUE or FALSE).	
PoCL Status	CORACQ_PRM_SIGNAL_STATUS	Status of power signals connected to the acquisition device. Possible values are Active or Not Active.	

Advanced Control Category

The Advanced Control category groups parameters for configuring camera control signals, board sync outputs and other advanced settings.



Parameter Descriptions

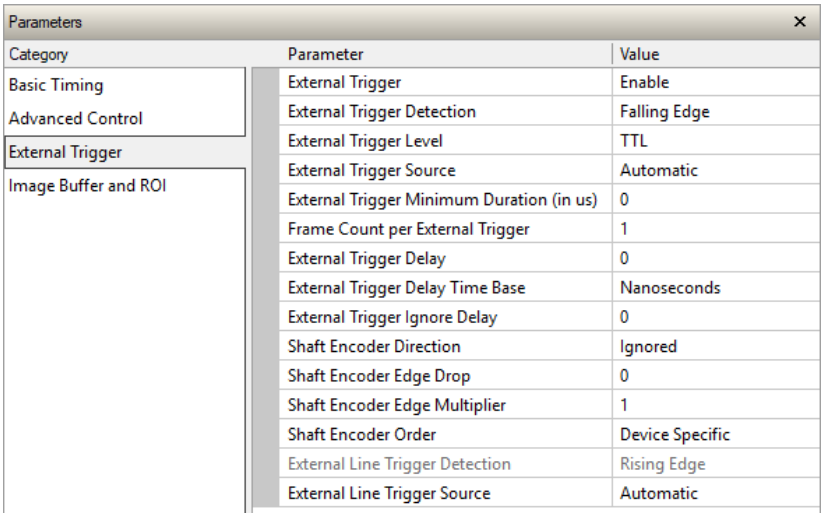
The following table describes the CamExpert Advanced Control category of Sapera LT parameters. Acquisition server notes, if applicable, indicate if parameter availablility or supported values are dependent on the selected frame grabber acquisition server and acquisition device.

Display Name	Parameter	Description	Notes
Internal Frame Trigger	CORACQ_PRM_INT_FRAME_TRIGGER_ENABLE	Enables/disables the acquisition device's internal frame trigger. Boolean parameter (TRUE or FALSE).	Applies to areascan cameras only.
Internal Frame Trigger Frequency (in Hz)	CORACQ_PRM_INT_FRAME_TRIGGER_FREQ	Internal frame trigger frequency in Hz. Set to the required frame rate when using internal frame trigger to control camera acquisition. Valid range is 0.001-10000Hz.	
Line Sync Source	CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE CORACQ_PRM_INT_LINE_TRIGGER_ENABLE CORACQ_PRM_SHAFT_ENCODER_ENABLE	Selects the line trigger source for linescan cameras, unless free-running.	Applies to linescan cameras only.
Interal Line Trigger Frequency (in Hz)	CORACQ_PRM_INT_LINE_TRIGGER_FREQ	Sets the internal line trigger frequency, in Hz. Applies only when the Line Sync Source is set to Internal Line Trigger.	Applies to linescan cameras only.
Camera Line Trigger Frequency Min (in Hz)	CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MIN	Sets the camera's minimum line trigger frequency. Minimum value is 1Hz.	Applies to linescan cameras only.
Camera Line Trigger Frequency Max (in Hz)	CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MAX	Sets the camera's maximum line trigger frequency. Maximum value is 10000000 Hz.	Applies to linescan cameras only.
Camera Control method selected	CORACQ_PRM_TIME_INTEGRATE_ENABLE CORACQ_PRM_CAM_TRIGGER_ENABLE CORACQ_PRM_LINE_TRIGGER_ENABLE	Enables or disables an available camera control method. Each supported control method has one or more operating modes to choose from; refer to the parameters: Camera Trigger Method Setting Time Integration Method Setting.	
Time Integration Method Setting	CORACQ_PRM_TIME_INTEGRATE_METHOD CORACQ_PRM_TIME_INTEGRATE_DELAY	When the Camera Control method is Time Integration, select and configure the control method required. Click on the parameter field to open the configuration dialog.	
Camera Trigger Method Setting	CORACQ_PRM_CAM_TRIGGER_METHOD	When an asynchronous trigger pulse to a camera is required, select and configure the required method.	
Line Integration Method Setting	CORACQ_PRM_LINE_INTEGRATE_METHOD	Sets the method for controlling the camera's line integration.	Applies to linescan cameras only

Line Trigger Method Setting	CORACQ_PRM_LINE_TRIGGER_METHOD	Sets the method for line trigger pulse output.	Applies to linescan cameras only
Camera Frames Per Trigger	CORACQ_PRM_CAM_FRAMES_PER_TRIGGER	Specifies the number of frames output by the camera per trigger; currently not available.	Applies to area scan cameras only.
Camera Control During Readout	CORACQ_PRM_CAM_CONTROL_DURING_READOUT	Specifies if the camera control signals can be sent during the readout of a frame. Possible values are: • Valid • Invalid • Ignore	
Strobe Method Setting	CORACQ_PRM_STROBE_METHOD CORACQ_PRM_STROBE_ENABLE CORACQ_PRM_STROBE_DELAY CORACQ_PRM_STROBE_DURATION CORACQ_PRM_STROBE_LEVEL CORACQ_PRM_STROBE_POLARITY	When a strobe output signal from the acquisition board is required, select and configure the control method required. Note, method 1 is only available for areascan camera type; method 3 for line scan only.	
Line Trigger Auto Delay	CORACQ_PRM_LINE_TRIGGER_AUTO_DELAY	Enables delaying line triggers to a camera based on the selected method. Used to avoid over-triggering a camera.	Applies to linescan cameras only
Time Stamp Base	CORACQ_PRM_TIME_STAMP_BASE	Sets the counter stamp time base. Possible values are: • Microseconds • Line Counts • External line trigger or shaft encoder • Shaft Encoder • 100 Nanoseconds	
Board Sync Output 1 Source	CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE	Specifies the signal to output on board sync output 1. This parameter permits the synchronization of two acquisition devices using a signal from one acquisition device and synching the second acquisition device with it.	
Board Sync Output 2 Source	CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE	Specifies the signal to output on board sync output 2. This parameter permits the synchronization of two acquisition devices using a signal from one acquisition device and synching the second acquisition device with it.	

External Trigger Category

The External category groups parameters for configuring an external trigger for controlling image acquisition.



Parameter Descriptions

The following table describes the CamExpert External Trigger category of Sapera LT parameters. Acquisition server notes, if applicable, indicate if parameter availablility or supported values are dependent on the selected frame grabber acquisition server and acquisition device.

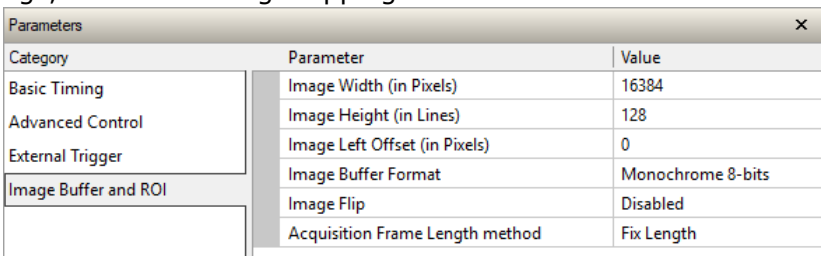
Display Name	Parameter	Description	Notes
External Trigger	CORACQ_PRM_EXT_TRIGGER_ENABLE	Enables/disables external trigger on the acquisition board. When enabled, the acquisition board acquires an image frame from the camera after receiving the trigger. Boolean parameter (TRUE or FALSE). Note: Applies to area scan cameras only.	
External Trigger Detection	CORACQ_PRM_EXT_TRIGGER_DETECTION	Defines the signal detected that generates an external trigger event to the acquisition device. Two types of trigger are available: *Level Trigger: Active Low / High* Logic level (Low/High) on the trigger input enables continuous image capture until the trigger input is set to opposite logic . *Edge Trigger: Rising / Falling edge* Edge transition of a trigger pulse captures one image frame.	
External Trigger Level	CORACQ_PRM_EXT_TRIGGER_LEVEL	Specifies the electrical level of the external trigger connected to the acquisition board. Possible values: TTL single-ended logic signal RS-422 balanced logic signal 12V single-ended logic signal 24V single-ended logic signal	

External Trigger Source	CORACQ_PRM_EXT_TRIGGER_SOURCE	Specifies the physical input source the external frame trigger is connected to or which trigger input is used on the acquisition device. Note: to assign the external trigger source to a GPIO it must be reserved; By default, boards are shipped with User Interface General Inputs 1 & 2 reserved for External Triggers and User Interface General Outputs 1 & 2 reserved for Strobe Outputs. Refer to User Interface GIOs Reservation for more information on using the Teledyne DALSA Device Manager tool to reserve GPIOs.	
External Trigger Minumum Duration (in µs)	CORACQ_PRM_EXT_TRIGGER_DURATION	Minimum external trigger pulse duration (in µs), needed for the pulse to be acknowledged by the acquisition device. If the duration of the pulse is shorter, the pulse is ignored. This feature is useful for trigger pulse debouncing. If the value is '0', no validation is performed	
Frame Count per External Trigger	CORACQ_PRM_EXT_TRIGGER_FRAME_COUNT	Number of images to acquire upon receiving an external trigger. Valid range is 1-262142. Note, infinite frame count (-1) is not supported.	
External Trigger Delay	CORACQ_PRM_EXT_TRIGGER_DELAY	Sets the delay between the reception of the trigger signal and the start of the image acquisition. Units are specified by the External Trigger Delay Time Base parameter.	
External Trigger Delay Time Base	CORACQ_PRM_EXT_TRIGGER_DELAY_TIME_BASE	Sets the external trigger delay time base. Possible values: • Line Counts • Nanoseconds • External Line Trigger or Shaft Encoder • Shaft Encoder	
External Trigger Ignore Delay	CORACQ_PRM_EXT_TRIGGER_IGNORE_DELAY	Sets the time delay, in µsec, where if another external trigger occurs, it is ignored. Valid range is 0-42949672. The start of the delay (time '0') is the end of the next vertical sync for analog cameras, or the beginning of the next frame valid for digital cameras, following a valid external trigger.	
Shaft Encoder Direction	CORACQ_PRM_SHAFT_ENCODER_DIRECTION	Selects the direction of the shaft encoder that increments/decrements the acquisition device encoder counter. Support of dual phase encoders might require that the direction of motion be considered. This is the case where system vibrations and/or conveyor backlash can cause the encoder to momentarily travel backwards. The acquisition device must in those cases count the reverse steps and subtract the forward steps such that only pulses after the reverse count reaches zero are considered valid.	Applies to linescan cameras only.
Shaft Encoder Edge Drop	CORACQ_PRM_SHAFT_ENCODER_DROP	Number of shaft encoder signal edges dropped between active shaft encoder triggers. Use the pulse drop feature to reduce the acquisition rate without reducing the shaft encoder trigger rate. Typical values are 0-255.	Applies to linescan cameras only.
Shaft Encoder Edge Multiplier	CORACQ_PRM_SHAFT_ENCODER_MULTIPLY	Number of signal edges generated internally on the acquisition board for each external shaft encoder signal edge. Use when video acquisitions are controlled by an external shaft encoder trigger but multiple acquisitions are needed from each trigger.	Applies to linescan cameras only.
Shaft Encoder Order	CORACQ_PRM_SHAFT_ENCODER_ORDER	Specifies the order in which to apply drop and multiply operations. For automatic mode the oder is multiply/drop.	Applies to linescan cameras only.
External Line Trigger Detection	CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION	Select the signal detected (rising edge/falling edge) that generates an external line trigger to the acquisition device.	Applies to linescan cameras only.

External Line Trigger Source	CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE	Specifies the physical input source the external line trigger is connected to on the acquisition device, in the case where the acquisition device has more than one input. Line scan cameras typically use the shaft encoder signals as the acquisition board line trigger. The 'Automatic' choice selects the trigger normally used with the acquisition module, in the case of multiple modules – multiple trigger inputs.	Applies to linescan cameras only.

Image Buffer and ROI Category

The Image Buffer and ROI category groups parameters for the configuring the image buffer format, size and offset settings, as well as image flipping.



Parameter Descriptions

The following table describes the CamExpert Image Buffer and ROI category of Sapera LT parameters. Acquisition server notes, if applicable, indicate if parameter availablility or supported values are dependent on the selected frame grabber acquisition server and acquisition device.

Display Name	Parameter	Description	Notes
Image Width (in Pixels)	CORACQ_PRM_CROP_WIDTH	Cropped width of the acquisition image, in pixels; this parameter defines the width of the image transferred to the frame buffer. The maximum width is the active horizontal of the image source (see the Horizontal Active parameter in the Basic Timing category). Cropping increments depend on the selected acquisition server; CamExpert automatically adjusts numerical entries to valid increments.	Note: image data is not scaled.
Image Height (in Lines)	CORACQ_PRM_CROP_HEIGHT	Cropped height of the acquisition image, in lines; this parameter defines the vertical dimension of the image transferred to the frame buffer. The maximum height is the active vertical width of the image source (see the Vertical Active parameter in the Basic Timing category). Cropping increments depend on the selected acquisition server; CamExpert automatically adjusts numerical entries to valid increments.	Note: image data is not scaled.
Image Left Offset (in Pixels)	CORACQ_PRM_CROP_LEFT	Number of pixels to crop from the left side of the acquisition image before transfer to the frame buffer. The maximum left offset is the active horizontal width of the image source less one increment step. Cropping increments depend on the selected acquisition server; CamExpert automatically adjusts numerical entries to valid increments.	Note: image data is not scaled.
Image Top Offset (in Lines)	CORACQ_PRM_CROP_TOP	Number of lines to crop from the top of the acquisition image before transfer to the frame buffer. The maximum top offset is the active vertical height of the image source less one increment step. Cropping increments are acquisition hardware dependent; CamExpert automatically adjusts numerical entries to valid increments.	Note: image data is not scaled.

Image Buffer Format	CORACQ_PRM_OUTPUT_FORMAT	Data format for the acquisition image transfer to the frame buffer.	The data buffer format is dependent on the selected acquisition server; for details refer to the CORACQ_PRM_OUTPUT_FORMAT parameter description
Image Flip	CORACQ_PRM_FLIP	Enables real-time on-board horizontal image flip function. The Xtium-CLHS PX4 also supports a vertical flip operation using CORXFER_PRM_FLIP.	
Acquisition Frame Length method	CORACQ_PRM_FRAME_LENGTH	Specifies if the images output by the acquisition device have a fixed or variable frame length. Variable frame length is of interest with linescan applications where the external frame trigger timing changes. External frame trigger could be active high or low pulse width controlled, or external frame trigger could be from a double pulse control.	Applies to linescan cameras only.

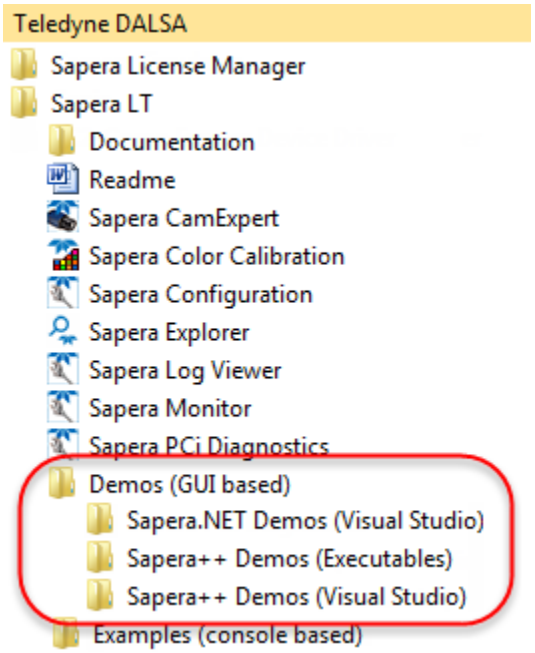
Sapera Demo Applications

Grab Demo Overview

The Grab Demo program demonstrates the basic acquisition functions included in the Sapera library. The program either allows you to acquire images, in continuous or in one-time mode, while adjusting the acquisition parameters. The program code may be extracted for use within your own application.

The Grab Demo is available as a compiled binary; source code is provided for both C++ and .NET projects using Visual Studio 2010/2012/2013/2015/2017.

All demos are available through the Start menu.



Grab Demo Workspace Details

Program file	…\...\Sapera\Demos\Binaries\GrabDemo.exe
Visual C++ Solution	…\...\Sapera\Demos\Classes\Vc\SapDemos_2010.sln …\...\Sapera\Demos\Classes\Vc\SapDemos_2012.sln …\...\Sapera\Demos\Classes\Vc\SapDemos_2013.sln …\...\Sapera\Demos\Classes\Vc\SapDemos_2015.sln …\...\Sapera\Demos\Classes\Vc\SapDemos_2017.sln
Visual .NET Solution	…\...\Sapera\Demos\NET\SapDemos_2010.sln …\...\Sapera\Demos\NET\SapDemos_2012.sln …\...\Sapera\Demos\NET\SapDemos_2013.sln …\...\Sapera\Demos\NET\SapDemos_2015.sln …\...\Sapera\Demos\NET\SapDemos_2017.sln
Remarks	This demo is based on Sapera LT classes. See the Sapera User's and Reference manuals for more information.

Using the Grab Demo

Server Selection

Run the grab demo from the start menu:
Start•Programs•Sapera LT•Demos•Frame Grabbers•Grab Demo.

The demo program first displays the acquisition configuration menu. The first drop menu displayed permits selecting from any installed Sapera acquisition servers (installed Teledyne DALSA acquisition hardware using Sapera drivers). The second drop menu permits selecting from the available input devices present on the selected server.

CCF File Selection

Use the acquisition configuration menu to select the required camera configuration file for the connected camera. Sapera camera files contain timing parameters and video conditioning parameters. The default folder for camera configuration files is the same used by the CamExpert utility to save user generated or modified camera files.

Use the Sapera CamExpert utility program to generate the camera configuration file based on timing and control parameters entered. The CamExpert live acquisition window allows immediate verification of those parameters. CamExpert reads both Sapera *.cca and *.cvi for backward compatibility with the original Sapera camera files.

Grab Demo Main Window

The Grab Demo program provides basic acquisition control for the selected frame grabber. The loaded camera file (.ccf) defines the Frame buffer defaults.

Refer to the Sapera LT User's Manual, in section "Demos and Examples – Acquiring with Grab Demo", for more information on the Grab Demo and others provided with Sapera LT.

Xtium-CLHS PX4 Reference

Block Diagram

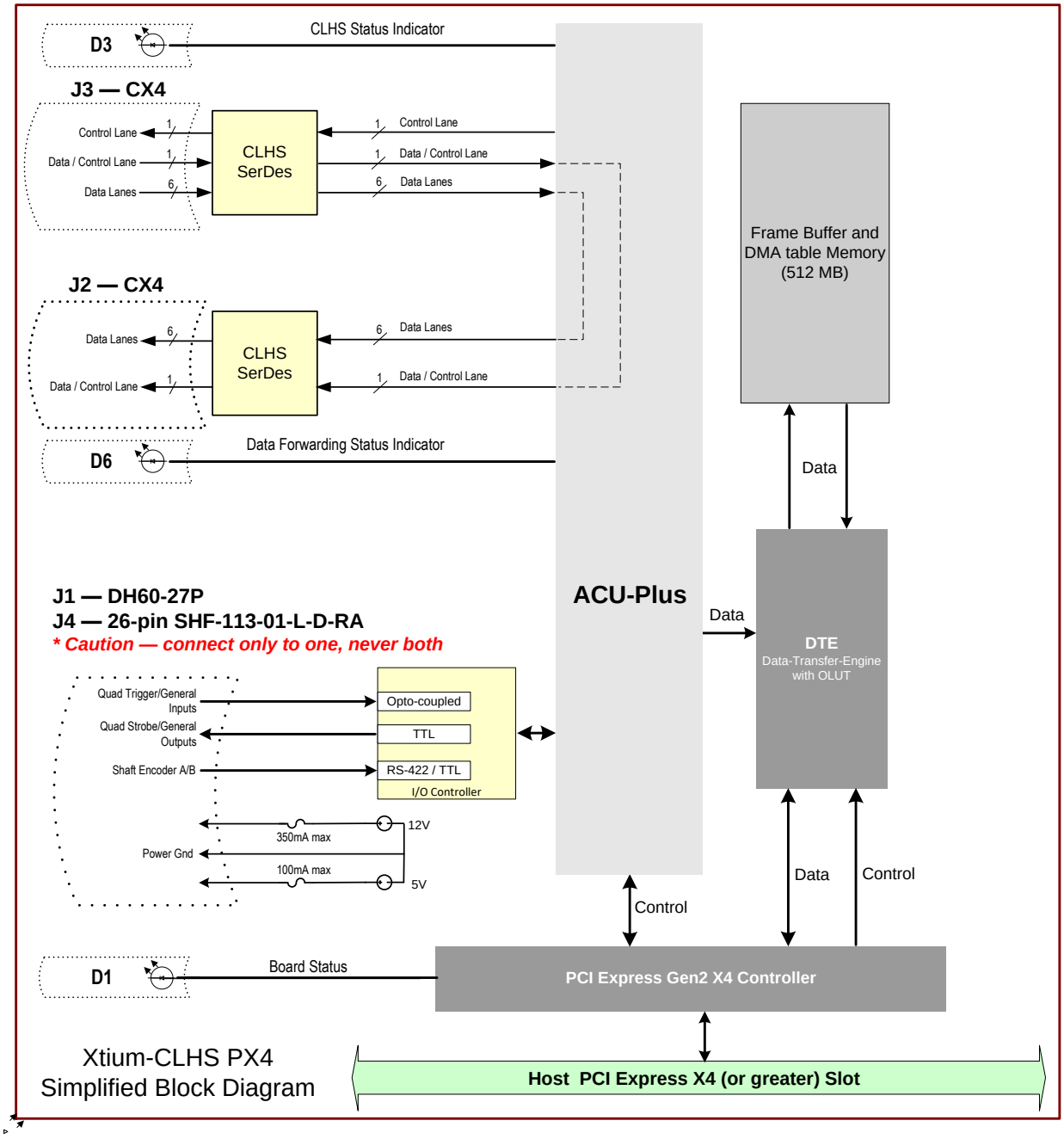


Figure 10: Xtium-CLHS PX4 Block Diagram

Xtium-CLHS Flow Diagram

The following diagram represents the sequence in which the camera data acquired is processed through the Xtium-CLHS.

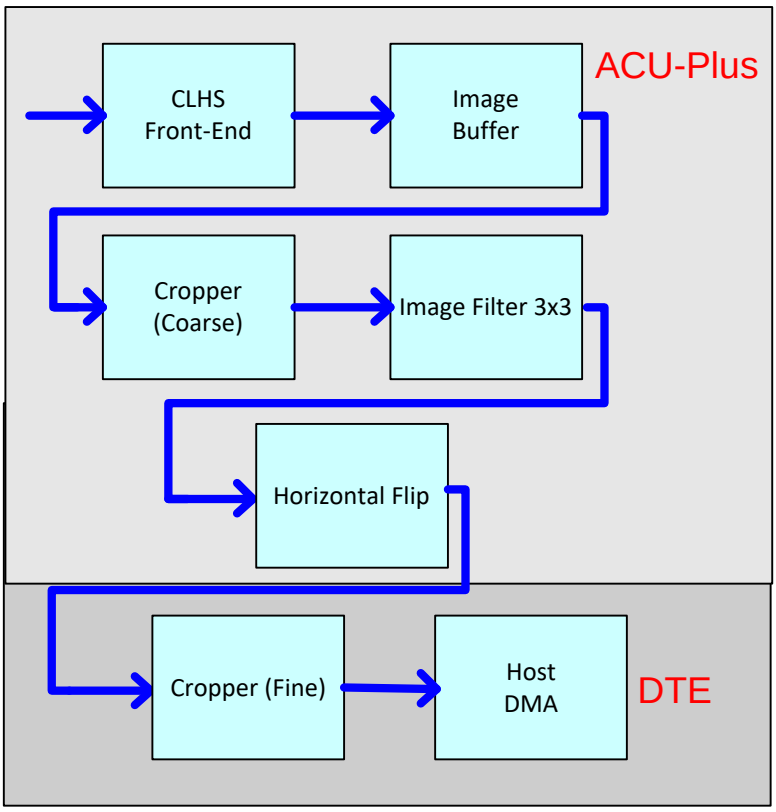


Figure 11: Xtium-CLHS Flow Diagram

- **Camera Link HS Front End:** Extracts the video data packets from the Camera Link HS port.
- **Image Buffer:** Stores the video data using the model of video frames.
- **Cropper (Coarse):** Horizontal cropper used when reading out from the memory.
- **Image Filter 3x3:** Apply filter to the image.
- **Horizontal Flip:** Performs the line data flip process.
- **Cropper (Fine):** Crops the resulting image when used, using an 8-byte resolution.
- **Host DMA:** Transfers the data from frame grabber into the host buffer memory. This module will also perform the vertical flip if enabled.

CLHS Camera Implementation

The following figure defines the Xtium CLHS PX4 camera interface as per the *Camera Link HS (CLHS) specification version 1.0*. The key parameters are:

- A single camera connector (J3) which is a copper hardwired interface with a thumbscrew locking mechanism – not an optical interface.
- Supports the M-Protocol definition of the Physical and Data Link Layer.
- There is one command channel to/from the camera.
- Supports single connector cameras that have 1 to 7 data Lanes.

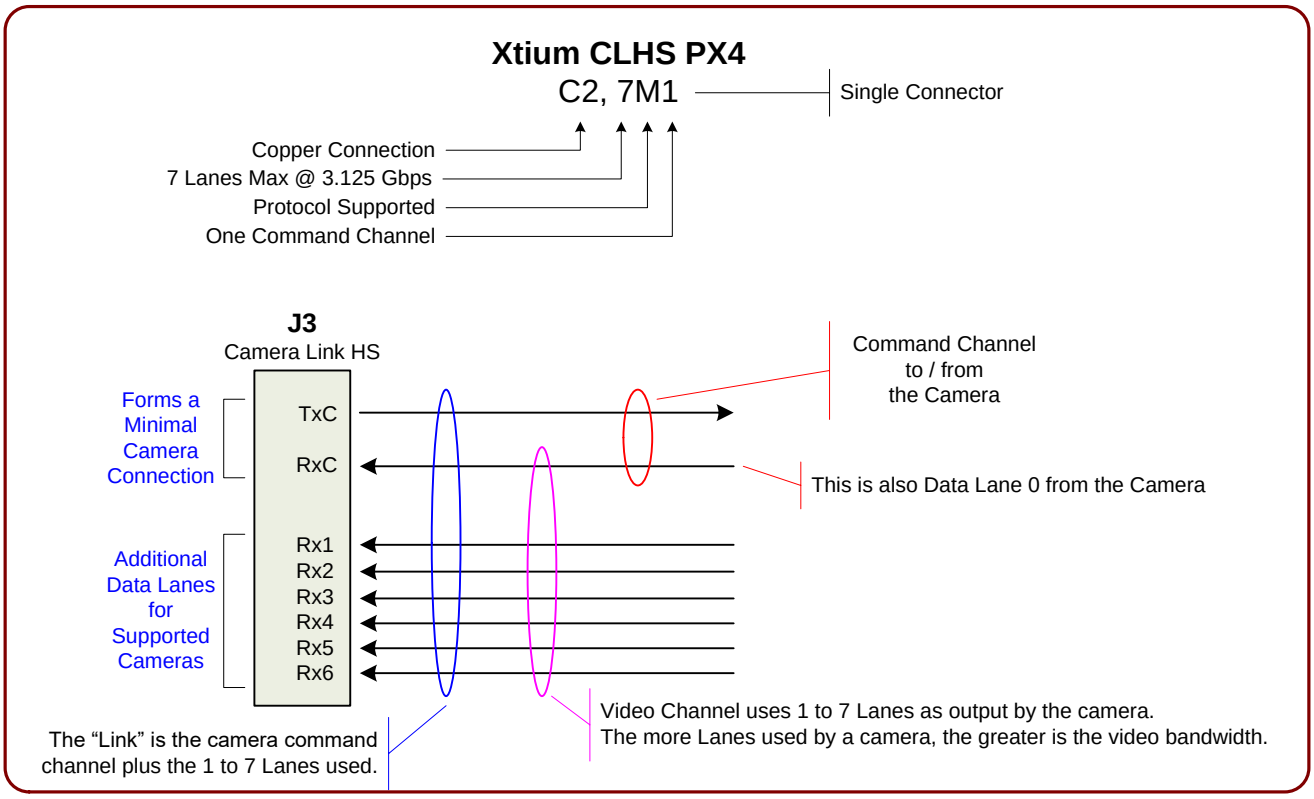


Figure 12:CLHS Camera Interface

Line Trigger Source Selection for Line scan Applications

Line scan imaging applications require some form of external event trigger to synchronize line scan camera exposures to the moving object. This synchronization signal is either an external trigger source (one exposure per trigger event) or a shaft encoder source composed of a single or dual phase (also known as a quadrature) signal.

The Xtium-CLHS PX4 shaft encoder inputs provide additional functionality with pulse drop, pulse multiply and pulse direction support.

The following table describes the line-trigger source types supported by the Xtium-CLHS PX4. Refer to the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00) for descriptions of the Sapera parameters.

CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE – Parameter Values Specific to the Xtium-CLHS PX4

PRM Value	Input used as: External Line Trigger	Input used as: External Shaft Encoder
	if CORACQ_PRM_EXT_LINE_ TRIGGER_ENABLE = *true*	*if* CORACQ_PRM_SHAFT_ ENCODER_ENABLE =*true*
0	From Shaft Encoder Phase A	From Shaft Encoder Phase A & B
1	From Shaft Encoder Phase A	From Shaft Encoder Phase A
2	From Shaft Encoder Phase B	From Shaft Encoder Phase B
3	n/a	From Shaft Encoder Phase A & B
4	From Board Sync #1	n/a
5	From Board Sync #2	n/a

CVI/CCF File Parameters Used

- External Line Trigger Source = parameter value
- External Line Trigger Enable = true/false
- Shaft Encoder Enable = true/false

Shaft Encoder Interface Timing

Dual Balanced Shaft Encoder RS-422 Inputs:

- Input Phase A: Connector J1/J4: Pin 3 (Phase A +) & Pin 2 (Phase A -)
- Input Phase B: Connector J1/J4: Pin 6 (Phase B+) & Pin 5 (Phase B-)
- See J1: External I/O Signals Connector (Female DH60-27P) for complete connector signal details)

Web inspection systems with variable web speeds typically provide one or two synchronization signals from a web mounted encoder to coordinate trigger signals. These trigger signals are used by the acquisition linescan camera. The Xtium-CLHS PX4 supports single or dual phase shaft encoder signals. Dual encoder signals are typically 90 degrees out of phase relative to each other and provide greater web motion resolution.

Example using any Encoder Input with Pulse-drop Counter

When enabled, the triggered camera acquires one scan line for each shaft encoder pulse-edge. To optimize the web application, a second Sapera parameter defines the number of triggers to skip between valid acquisition triggers. The figure below depicts a system where a valid camera trigger is any pulse edge from either shaft encoder signal. After a trigger, the two following triggers are ignored (as defined by the Sapera pulse drop parameter).

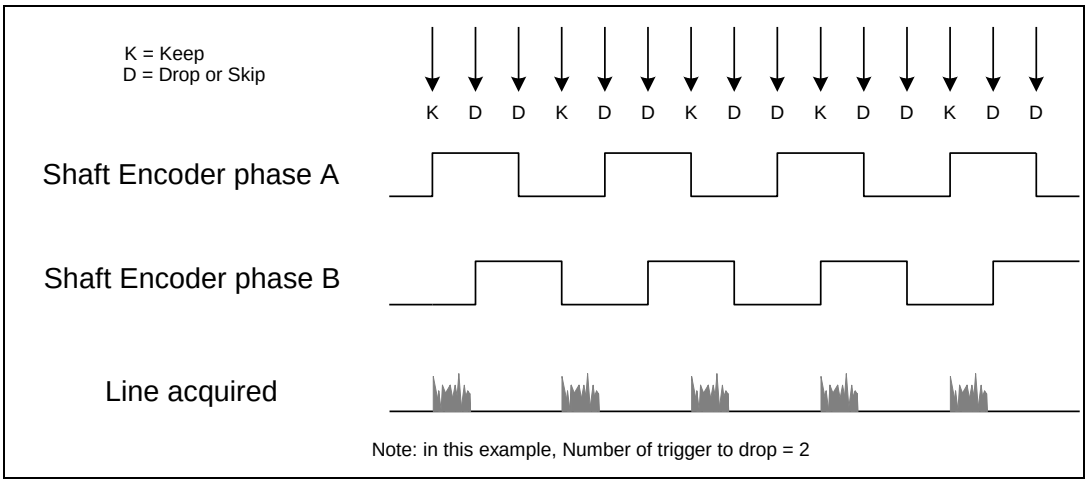


Figure 13: Encoder Input with Pulse-drop Counter

Example using Sequential Encoder Input

Support of a dual phase encoder should consider the direction of motion of one phase signal to the other. Such a case might exist where system vibrations and/or conveyor backlash can cause the encoder to briefly travel backwards. The acquisition device must in those cases count the reverse steps and subtract the forward steps such that only pulses after the reverse count reaches zero are considered. By using the event "Shaft Encoder Reverse Counter Overflow", an application can monitor an overflow of this counter.

Also, if a maximum line rate camera trigger source is a high jitter shaft encoder, the parameter CORACQ_PRM_LINE_TRIGGER_AUTO_DELAY can be used to automatically delay line triggers to avoid over-triggering a camera, and thus not miss a line. Note that some cameras integrate this feature. See also the event "Line Trigger Too Fast" that can be enabled when using the 'auto delay' feature.

The example figure below shows shaft encoder signals with high jitter. If the acquisition is triggered when phase B follows phase A, with jitter present phase B may precede phase A. Use of the *Shaft Encoder Direction* parameter will prevent false trigger conditions.

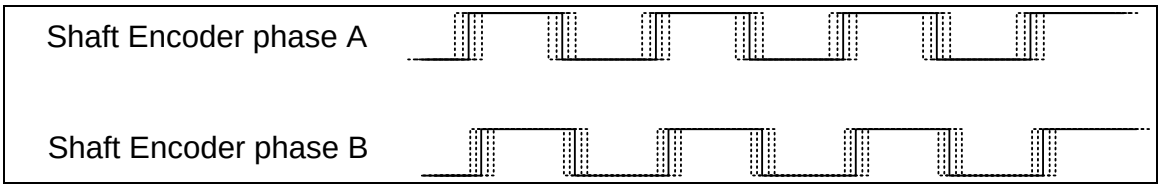


Figure 14: Using Shaft Encoder Direction Parameter

Note: Modify camera file parameters easily with the Sapera CamExpert program.

CVI/CCF File Parameters Used

Shaft Encoder Enable = X, where:

- If X = 1, Shaft Encoder is enabled
- If X = 0, Shaft Encoder is disabled

Shaft Encoder Pulse Drop = X, where:

- X = number of trigger pulses ignored between valid triggers

Shaft Encoder Pulse Multiply = X, where:

- X = number of trigger pulses generated for each shaft encoder pulses

Shaft Encoder Pulse Drop/Multiply Order = X, where:

- If X = 1, the drop operation will be done first, followed by the multiplier operation
- If X = 0 or 2, the multiplier operation will be done first, followed by the drop operation

Shaft Encoder Direction = X, where:

- X = 0, Ignore direction
- X = 1, Forward steps are detected by pulse order A/B (forward motion)
- X = 2, Forward steps are detected by pulse order B/A (reverse motion)

Shaft Encoder Level = X, where:

- X = 1, TTL (Rev B Only)
- X = 2, RS-422

Note: For information on camera configuration files, see the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

Virtual Frame Trigger for Line Scan Cameras

When using line scan cameras, a frame buffer is allocated in host system memory to store captured video lines. To control when a video line is stored as the first line in this "virtual" frame buffer, an external frame trigger signal is used.

For **fixed length** frames, the Sapera vertical cropping parameter controls the number of lines sequentially grabbed and stored in the virtual frame buffer.

For **variable length** frames, the External Frame Trigger (when a level or dual input type is selected) controls the number of lines sequentially grabbed up to the maximum of lines in the virtual frame buffer.

For both fixed and variable length frames, choosing an active low/high or dual input permits grabbing multiple consecutive images as long as the chosen signal is active. This action is also called "rolling over" to the next buffer. When choosing a single rising or falling edge, a single frame will be acquired, there is never any roll over.

External Frame Trigger Detection	Fixed Frame	Variable Frame
Active Low/High	Roll Over	Roll Over
Rising/Falling Edge	No Roll Over	No Roll Over
Dual Input Rising/Falling Edge	Roll Over	Roll Over

Virtual Frame Trigger Timing Diagram

- The virtual frame trigger signal (generated by some external event) connects to the Xtium-CLHS PX4 trigger input.
- Virtual frame trigger can be differential (RS-422) or single ended (TTL, 12V, 24V) industry standard, and be rising or falling edge active, active high or low, or double pulse rising or falling edge.
- Virtual frame trigger connects to the Xtium-CLHS PX4 via the External Trigger Input 1 & 2 inputs.
  - Trigger Input #1 on connector J1: pin 8
  - Trigger Input #2 on connector J1: pin 9
- The Sapera vertical cropping parameter specifies the number of lines captured (maximum size of virtual frame).

Synchronization Signals for a 10 Line Virtual Frame

The following timing diagram shows an example of grabbing 10 image lines from a line scan camera and the use of a virtual frame trigger to define when a video line is stored at the beginning of the virtual frame buffer.

In this example, virtual frame trigger control is configured for rising edge trigger.

- Camera control signals are active at all times. These continually trigger the camera acquisition in order to avoid corrupted video lines at the beginning of a virtual frame.
- The camera control signals are either timing controls on Xtium-CLHS PX4 shaft encoder inputs, or line triggers generated internally by the Xtium-CLHS PX4.

The following timing diagram shows the relationship between External Frame Trigger input, External Shaft Encoder input (one phase used with the second terminated), and camera control output to the camera.

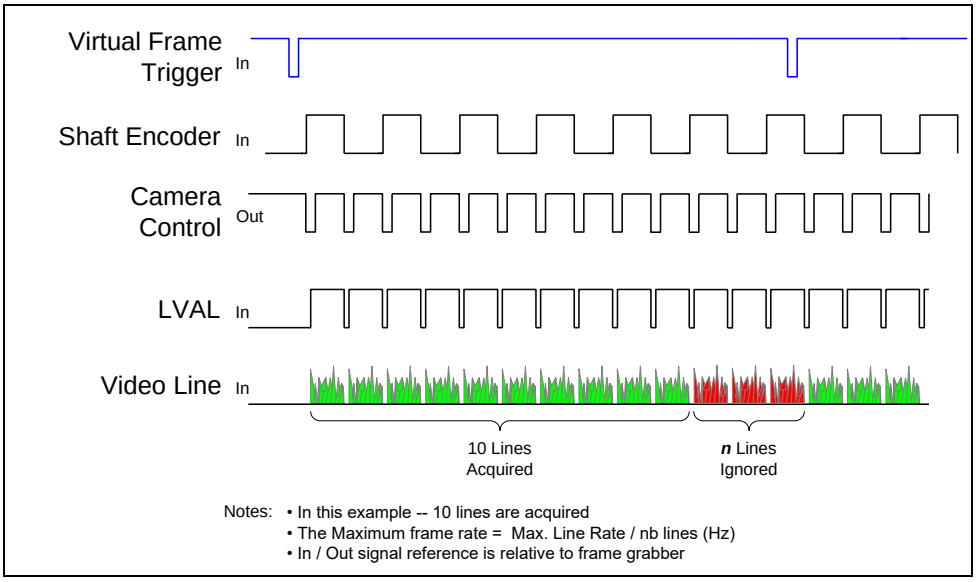


Figure 15: Synchronization Signals for a 10 Line Virtual Frame

Synchronization Signals for Fixed Frame Length Acquisition

A trigger event is only generated when a grab is active; when not grabbing no trigger events are generated. When a frame is complete, the frame grabber checks for the specified active trigger level and, if present, grabs the next frame; otherwise, it waits for the next detected active trigger level.

In the following diagrams:

"*T*" indicates a valid external trigger event (SapAcquisition::EventExternalTrigger).
"*Ignored*" is an ignored event (SapAcquisition::EventExternalTriggerIgnored).

such that

Ignored + *T* = total triggers received by frame grabber

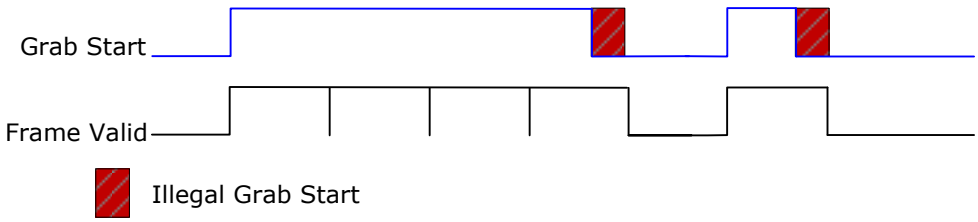


Figure 16: Line scan, Fixed Frame, No Trigger

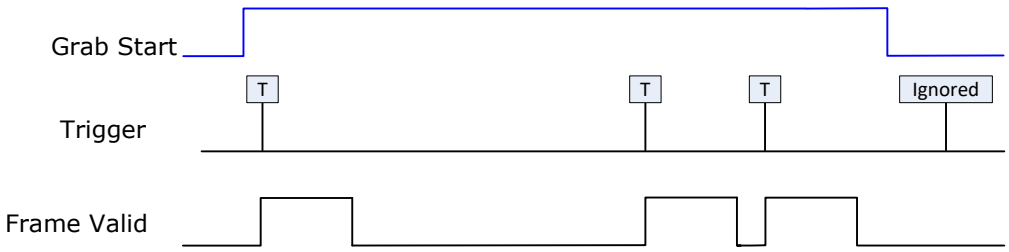


Figure 17: Line scan, Fixed Frame, Edge Trigger

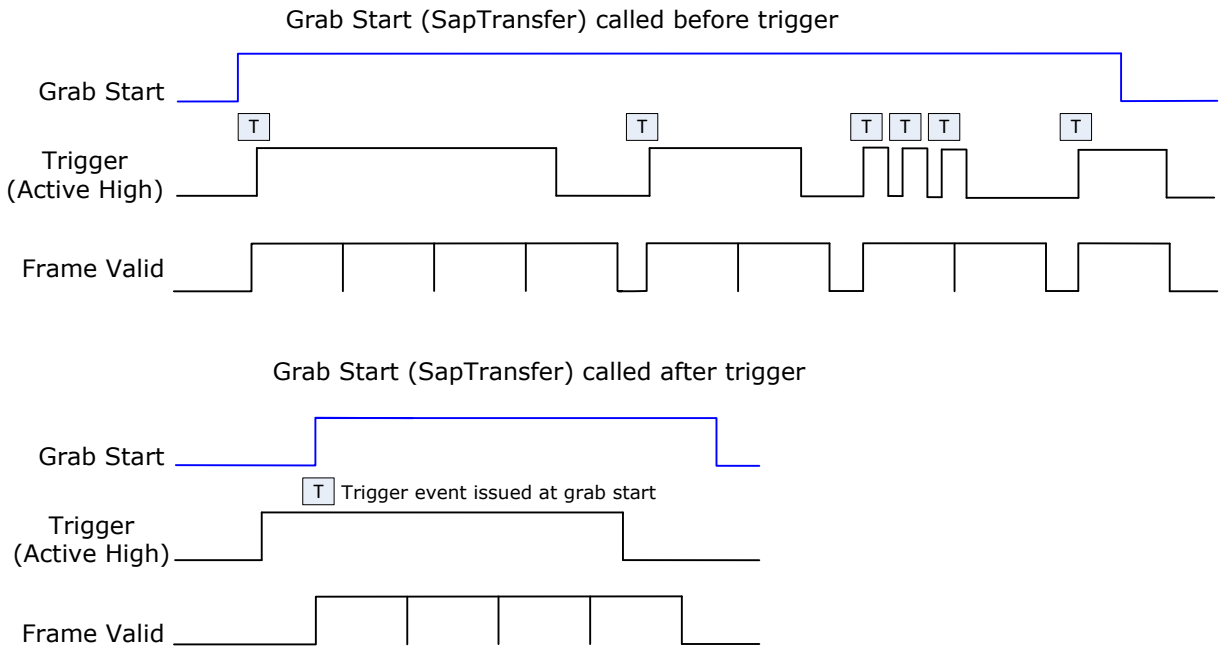


Figure 18: Line scan, Fixed Frame, Level Trigger (Roll-Over to Next Frame)

Synchronization Signals for Variable Frame Length Acquisition

For variable length frames, trigger ignored events are not issued (SapAcquisition::EventExternalTriggerIgnored); a valid trigger event always initiates either a frame start or frame end.

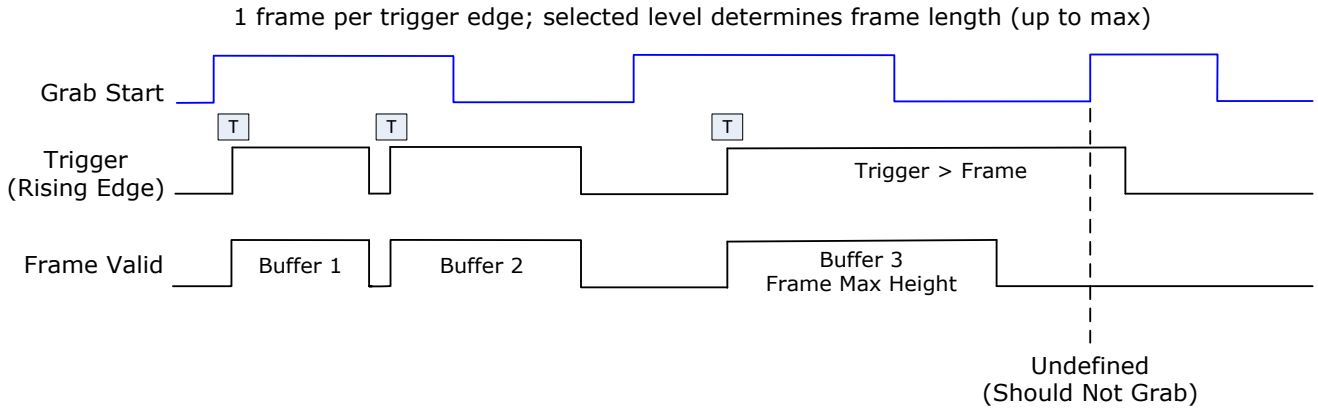


Figure 19: Line scan, Variable Frame, Edge Trigger (Active High determines Frame Length)

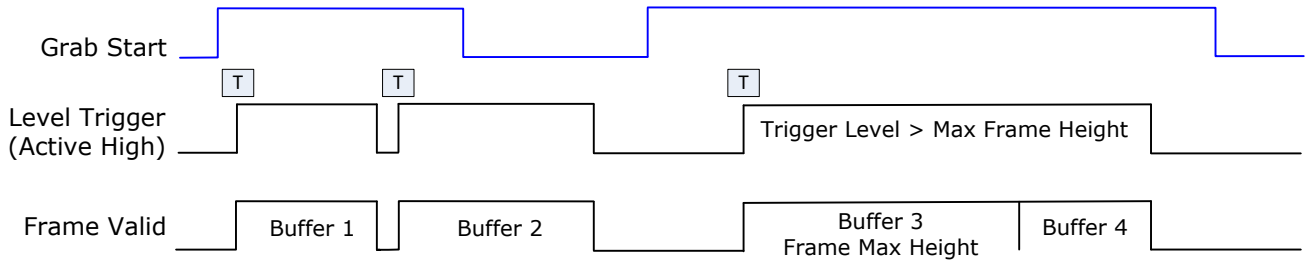


Figure 20: Line scan, Fixed Frame, Level Trigger (Roll-Over)

CVI File (VIC) Parameters Used

The VIC parameters listed below provide the control functionality for virtual frame reset. Sapera applications load pre-configured CVI files or change VIC parameters during runtime.

Note: Sapera camera file parameters are easily modified by using the CamExpert program.

External Frame Trigger Enable = X, where: (*with Virtual Frame Trigger enabled*)

- If X = 1, External Frame Trigger is enabled
- If X = 0, External Frame Trigger is disabled

External Frame Trigger Detection = Y, where: (*with Virtual Frame Trigger edge select*)

- If Y= 1, External Frame Trigger is active low
- If Y= 2, External Frame Trigger is active high
- If Y= 4, External Frame Trigger is active on rising edge
- If Y= 8, External Frame Trigger is active on falling edge
- If Y= 32, External Frame Trigger is dual-input rising edge
- If Y= 64, External Frame Trigger is dual-input falling edge

Note:. For dual-input triggers, Trigger Input #1 signals the start of the frame trigger, Trigger Input #2 signals the end of the frame trigger.

External Frame Trigger Level = Z, where: (*with Virtual Frame Trigger signal type*)

- If Z= 1, External Frame Trigger is a TTL signal
- If Z = 2, External Frame Trigger is a differential signal (RS-422)
- If Z = 8, External Frame Trigger is a 24V signal
- If Z = 64, External Frame Trigger is a 12V signal

Note: For information on camera configuration files, see the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

Sapera Acquisition Methods

Sapera acquisition methods define the control and timing of the camera and frame grabber board. Various methods are available, grouped as:

- Camera Trigger Methods (method 3 supported)
- Line Trigger Methods (method 2)
- Line Integration Methods (methods 8, 9 and 10 supported)
- Time Integration Methods (method 10, 11 and 12)
- Strobe Methods (method 1, 3, 4 and 5 supported)

Refer to the Sapera LT Acquisition Parameters Reference manual (OC-SAPM-APR00) for detailed information concerning camera and acquisition control methods.

Trigger to Image Reliability

Trigger-to-image reliability incorporates all stages of image acquisition inside an integrated controller to increase reliability and simplify error recovery. The trigger-to-image reliability model brings together all the requirements for image acquisition to a central management unit. These include signals to control camera timing, on-board frame buffer memory to compensate for PCI bus latency, and comprehensive error notification. If the Xtium-CLHS PX4 detects a problem, the application can take appropriate action to return to normal operation.

The Xtium-CLHS PX4 is designed with a robust ACU (Acquisition and Control Unit). The ACU monitors in real-time, the acquisition state of the input plus the DTE (Data Transfer Engine) which transfers image data from on-board memory into PC memory. In general, these management processes are transparent to end-user applications. With the Xtium-CLHS PX4, applications ensure trigger-to-image reliability by monitoring events and controlling transfer methods as described below:

Supported Events and Transfer Methods

Listed below are the supported acquisition and transfer events. Event monitoring is a major component to the Trigger-to-Image Reliability framework.

Acquisition Events

Acquisition events pertain to the acquisition module and provide feedback on the image capture phase.

Event	Description
External Trigger (Used/Ignored)	Generated when the external trigger pin is asserted, which indicates the start of the acquisition process. There are two types of external trigger events: 'Used' or 'Ignored'. Following an external trigger, if the event generates a captured image, an External Trigger Used event will be generated (CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER). If there is no captured image, an External Trigger Ignored event will be generated (CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED). An external trigger event is ignored if the event rate is higher than the possible frame rate of the camera.
Start of Frame	Event generated during acquisition, with the detection of the start of a video frame by the board acquisition hardware. The Sapera event value is CORACQ_VAL_EVENT_TYPE_START_OF_FRAME.
End of Frame	Event generated during acquisition, with the detection of the end of a video frame by the board acquisition hardware. The Sapera event value is CORACQ_VAL_EVENT_TYPE_END_OF_FRAME.

Data Overflow	The Data Overflow event indicates that there is not enough bandwidth for the acquired data transfer without loss. Data Overflow would occur with limitations of the acquisition module and should never occur. The Sapera event value is CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW.
Frame Valid	Event generated on detection of the start of a video frame by the board acquisition hardware. Acquisition does not need to be active; therefore, this event can verify a valid signal is connected. The Sapera event value is CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC.
Link (Lock/Unlock)	Event generated on the transition from locking or not locking, of the required lanes. The Sapera event values are: CORACQ_VAL_EVENT_TYPE_LINK_LOCK CORACQ_VAL_EVENT_TYPE_LINK_UNLOCK.
Frame Lost	The Frame Lost event indicates that an acquired image failed to transfer to on-board memory. An example is if there are no free on-board buffers available for the new image. This may be the case if the image transfer from onboard buffers to host PC memory is not sustainable due to bus bandwidth issues or no host buffers are available to receive an image. The Sapera event value is CORACQ_VAL_EVENT_TYPE_FRAME_LOST.
External Line Trigger Too Slow	Event which indicates that the detected shaft encoder input tick rate is too slow for the device to take into account the specified shaft encoder multiplier value. The Sapera event value is CORACQ_VAL_EVENT_TYPE_EXT_LINE_TRIGGER_TOO_SLOW.
Line Trigger Too Fast	Event which indicates a previous line-trigger did not generate a complete video line from the camera. Note that due to jitter associated with using shaft encoders, the acquisition device can delay a line trigger if a previous line has not yet completed. This event is generated if a second line trigger comes in while the previous one is still pending. This event is generated once per virtual frame. The Sapera event value is CORACQ_VAL_EVENT_TYPE_LINE_TRIGGER_TOO_FAST.
Shaft Encoder Reverse Count Overflow	Event which indicates that the shaft encoder has travelled in the opposite direction expected and that the number of pulses encountered during that travel has exceeded the acquisition device counter. The acquisition device will thus not be able to skip the appropriate number of pulses when the expected direction is detected. The Sapera event value is CORACQ_VAL_EVENT_TYPE_SHAFT_ENCODER_REVERSE_COUNT_OVERFLOW.
Camera Missed Trigger	Event which indicates that the camera could not respond to a trigger request as it was busy servicing a previous trigger request. The Sapera event value is CORACQ_VAL_EVENT_TYPE_CAMERA_MISSED_TRIGGER
Camera Overrun	Event which indicates that the camera data and/or video has been corrupted due to insufficient buffer space in the camera. The Sapera event value is CORACQ_VAL_EVENT_TYPE_CAMERA_OVERRUN
Link Error	Event which indicates that an error has occurred on one or more of the lanes. Information about the source of the link error and the number of occurances of this error can be retreived using the SapAcqCallbackInfo class. *GetGenericParam0*: returns the source of the error: • 1: CRC Error • 2: 8B/10B Error • 3: Packet Buffer Overflow • 4: Packet Resend *GetGenericParam1*: returns a bitfield indicating which lane(s) generated the error: Bit 0 = Lane 1, Bit 1= Lane 2, … *GetCustomSize*: returns 7 * UINT32 *GetCustomData*: returns the number of errors per lane. There are 7 entries, each entry being a UINT32.

Transfer Events

Transfer events are related to the transfer module and provide feedback on image transfer from onboard memory frame buffers to PC memory frame buffers.

Event	Description
Start of Frame	Start of Frame event generated when the first image pixel is transferred from on-board memory into PC memory. The Sapera event value is CORXFER_VAL_EVENT_TYPE_START_OF_FRAME.
End of Frame	End of Frame event generated when the last image pixel is transferred from on-board memory into PC memory. The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_FRAME.
End of Line	The End of Line event is generated after a video line is transferred to a PC buffer. The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_LINE.
End of N Lines	The End of N Lines event is generated after a set number of video lines are transferred to a PC buffer. The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_NLINES.
End of Transfer	End of Transfer event generated at the completion of the last image transfer from on-board memory into PC memory. Issue a stop command to the transfer module to complete a transfer (if transfers are already in progress). If a frame transfer of a fixed number of images is requested, the transfer module will stop transfer automatically. The Sapera event value is CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER.

Trigger Signal Validity

The ACU ignores external trigger signal noise with its programmable debounce control. Program the debounce parameter for the minimum pulse duration considered as a valid external trigger pulse. For more information see Note 1: General Inputs / External Trigger Inputs Specifications.

Supported Transfer Cycling Methods

The Xtium-CLHS PX4 supports the following transfer modes, which are either synchronous or asynchronous.

Images are accumulated in on-board memory in a FIFO type manner.On-board memory can get filled up if the rate at which the images are acquired is greater than the rate at which the DMA engine can write them to host buffer memory. On-board memory can also get filled-up if there are no more empty buffers available to transfer the on-board images.

When no memory is available for a new image to be stored in on-board memory, the image is discarded and a CORACQ_VAL_EVENT_TYPE_FRAME_LOST or trash buffer callback is generated. If a CORACQ_VAL_EVENT_TYPE_FRAME_LOST occurs when host buffers are available, it can indicate a problem with the PX4 bus bandwidth.

If image buffers are constructed using a trash buffer (SapBufferWithTrash using a transfer cycle mode with trash), when no host buffers are available and no memory is available for a new image to be stored in on-board memory, the SapXferCallBackInfo::IsTrash (C++) function or SaxXferNotifyEventsArgs.Trash (.NET) property returns true. If a trash callback function has been registered during construction of the SapTransfer object, it will be executed when a trash event occurs.

When stopping the image acquisition, the event CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER will occur once all images currently in the on-board memory are transferred to host buffer memory. Note that if the application does not provide enough empty buffers, the Xtium event will not occur and an acquisition abort will be required.

- CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_WITH_TRASH
  Before cycling to the next buffer in the list, the transfer device will check the next buffer's state. If its state is full, the transfer will keep the image in on-board memory until the next buffer's state changes to empty. If the on-board memory gets filled, trash callbacks will be generated.
- CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_NEXT_EMPTY_WITH_TRASH
  When starting an acquisition, the buffer list is put in an empty buffer queue list in the exact order they were added to the transfer. Whenever a user sets a buffer to empty, it is added to the empty buffer queue list, so that after cycling once through the original buffer list, the buffers acquired into will follow the order in which they are put empty by the user. So in this mode, the on-board images will be transferred to host buffer memory as long as there are buffers in the empty buffer queue list. If no buffers are available on the host and the on-board memory gets filled, trash callbacks will be generated.
- CORXFER_VAL_CYCLE_MODE_ASYNCHRONOUS
  The transfer device cycles through all buffers in the list without concern about the buffer state.

The following table describes the possible buffer states and resulting behavior:

Trash Buffer (cycling mode with trash)	**Xtium On-Board Memory State**	**Host Sapera Buffer State**	**Resulting Event**
NO	Empty buffer available (at least 1)	Empty buffer available (at least 1)	Normal acquisition events
NO	Empty buffer available (at least 1)	Full	Acquire into Xtium on-board memory
NO	Full	Empty buffer available (at least 1)	Frame Lost Event
NO	Full	Full	Frame Lost Event
YES	Empty buffer available (at least 1)	Empty buffer available (at least 1)	Normal acquisition events
YES	Empty buffer available (at least 1)	Full	Acquire into Xtium on-board memory
YES	Full	Empty buffer available (at least 1)	Frame Lost Event
YES	Full	Full	Trash Callback

- By default, the buffer state (empty or full) is automatically managed by Sapera LT; it can be managed manually by the user if necessary.

Output LUT Availability

Note: Contact Teledyne DALSA for availability.

Metadata: Theory of Operation

The following provides additional details on the Metadata implementation.

Metadata Data Structure

The Xtium-CLHS PX4 supports metadata at the end of each line when enabled through the parameter CORACQ_PRM_META_DATA. The metadata consists of 64 bytes. The content of the metadata represents a snapshot of the state of the frame grabber at the beginning of each LVAL received.

```
typedef struct
{
  ULONGLONG shaftEncoderCount;
  ULONGLONG lineCount;
  ULONGLONG lineTriggerCount;
  ULONGLONG timeStamp;
  ULONG frameCounter;
  UCHAR generalInputs;
  UCHAR generalOutputs;
  UCHAR biDirectionalIOs;
  UCHAR reserved[25];


} PX4_METADATA, *PPX4_METADATA;
```

- **shaftEncoderCount**: 64-bit counter of pulses received on the shaft encoder. This is a 'machine counter' that increments in one direction (forward) and decrements (reverse) in the opposite direction.
- **lineCount**: 64-bit counter of line valid (LVAL) received.
- **lineTriggerCount**: 64-bit counter of line triggers sent to the camera.
- **timeStamp**: 64-bit counter of the frame grabber on-board timestamp. See also CORACQ_PRM_TIME_STAMP_BASE and CORACQ_PRM_TIME_STAMP.
- **frameCounter**: 32-bit counter of frames received. This represents the frame number that the line belongs to.
- **generalInputs**: status of the general inputs (for example, Low, bit = 0 or High, bit = 1).
- **generalOutputs**: status of the general outputs (for example, Low, bit =0 or High, bit = 1).
- **biDirectionalIOs**: status of the bi-directional I/Os (for example, Low, bit = 0 or High, bit = 1).
- **reserved**: 25 bytes reserved for future usage.

For a demo application showing this feature, please contact Teledyne DALSA technical support.

Xtium-CLHS PX4 Supported Parameters

The tables below describe the Sapera capabilities supported by the Xtium-CLHS PX4. Unless specified, each capability applies to all configuration modes and all acquisition modes.

The information here is subject to change. The application needs to verify capabilities. New board driver releases may change product specifications.

Sapera describes the Xtium-CLHS PX4 family as:

- Board Server: Xtium-CLHS_PX4_1
- Acquisition Module: *dependent on firmware used*

Camera Related Capabilities

Capability	Values
CORACQ_CAP_CONNECTOR_TYPE	CORACQ_VAL_CONNECTOR_TYPE_CLHS (0x10)

Camera Related Parameters

Parameter	Values
CORACQ_PRM_CHANNEL	CORACQ_VAL_CHANNEL_SINGLE (0x1)
CORACQ_PRM_FRAME	CORACQ_VAL_FRAME_PROGRESSIVE (0x2)
CORACQ_PRM_INTERFACE	CORACQ_VAL_INTERFACE_DIGITAL (0x2)
CORACQ_PRM_SCAN	CORACQ_VAL_SCAN_AREA (0x1) CORACQ_VAL_SCAN_LINE (0x2)
CORACQ_PRM_SIGNAL	CORACQ_VAL_SIGNAL_DIFFERENTIAL (0x2)
CORACQ_PRM_VIDEO	CORACQ_VAL_VIDEO_MONO (0x1) CORACQ_VAL_VIDEO_BAYER (0X10)
CORACQ_PRM_PIXEL_DEPTH	8 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO8 10 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO16 12 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO16 14 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO16 16 bits, # LUT = 0, LUT format = CORDATA_FORMAT_MONO16
CORACQ_PRM_VIDEO_STD	CORACQ_VAL_VIDEO_STD_NON_STD (0x1)
CORACQ_PRM_FIELD_ORDER	CORACQ_VAL_FIELD_ORDER_NEXT_FIELD (0x4)
CORACQ_PRM_HACTIVE	min = 32 pixel max = 65536 pixel step = 32 pixel * minimum is per lane
CORACQ_PRM_VACTIVE	min = 1 line max = 16777215 line step = 1 line
CORACQ_PRM_TIME_INTEGRATE_METHOD	CORACQ_VAL_TIME_INTEGRATE_METHOD_10 (0x200) CORACQ_VAL_TIME_INTEGRATE_METHOD_11 (0x400) CORACQ_VAL_TIME_INTEGRATE_METHOD_12 (0x800)
CORACQ_PRM_CAM_TRIGGER_METHOD	CORACQ_VAL_CAM_TRIGGER_METHOD_3 (0x4)
CORACQ_PRM_CAM_NAME	Default Camera Link HS Line Scan Mono
CORACQ_PRM_LINE_INTEGRATE_METHOD	CORACQ_VAL_LINE_INTEGRATE_METHOD_8 (0x80) CORACQ_VAL_LINE_INTEGRATE_METHOD_9 (0x100) CORACQ_VAL_LINE_INTEGRATE_METHOD_10 (0x200)
CORACQ_PRM_LINE_TRIGGER_METHOD	CORACQ_VAL_LINE_TRIGGER_METHOD_2 (0x2)
CORACQ_PRM_LINE_TRIGGER_DELAY	min = 0 nsec max = 4294967295 nsec step = 1 nsec
CORACQ_PRM_CHANNELS_ORDER	CORACQ_VAL_CHANNELS_ORDER_NORMAL (0x1)
CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MIN	1 Hz
CORACQ_PRM_CAM_LINE_TRIGGER_FREQ_MAX	10000000 Hz
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MIN	1 µs
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MAX	42949672 µs

CORACQ_PRM_DATA_VALID_ENABLE	TRUE FALSE
CORACQ_PRM_CAM_IO_CONTROL (*)	
CORACQ_PRM_BAYER_ALIGNMENT	Not available
CORACQ_PRM_CAM_CONTROL_DURING_READOUT	CORACQ_VAL_CAM_CONTROL_DURING_READOUT_INVALID (0x0) CORACQ_VAL_CAM_CONTROL_DURING_READOUT_VALID (0x01) CORACQ_VAL_CAM_CONTROL_DURING_READOUT_IGNORE (0x2)
CORACQ_PRM_DATA_LANES	min = 1 lane, max = 7 lanes, step = 1 lane
CORACQ_PRM_BIT_TRANSFER_RATE	3.125 Gbps
CORACQ_PRM_CLHS_CONFIGURATION	CORACQ_VAL_CLHS_CONFIGURATION_CAM_PORT_SLAVE (0x4) CORACQ_VAL_CLHS_CONFIGURATION_MANUAL_ACQ_START_STOP (0x8)

VIC Related Parameters

Parameter	Values
CORACQ_PRM_CAMSEL	CAMSEL_MONO = from 0 to 0
CORACQ_PRM_CROP_LEFT	min = 0 pixel max = 65528 pixel step = 4 pixel
CORACQ_PRM_CROP_TOP	min = 0 line max = 16777215 line step = 1 line
CORACQ_PRM_CROP_WIDTH	min =32 pixel max = 65536 pixel step =4 pixel
CORACQ_PRM_CROP_HEIGHT	min = 1 line max = 16777215 line step = 1 line
CORACQ_PRM_DECIMATE_METHOD	CORACQ_VAL_DECIMATE_DISABLE (0x1)
CORACQ_PRM_LUT_ENABLE	Not Available
CORACQ_PRM_LUT_NUMBER	Default = 0
CORACQ_PRM_STROBE_ENABLE	TRUE FALSE
CORACQ_PRM_STROBE_METHOD	CORACQ_VAL_STROBE_METHOD_1 (0x1) CORACQ_VAL_STROBE_METHOD_3 (0x4) CORACQ_VAL_STROBE_METHOD_4 (0x8) CORACQ_VAL_STROBE_METHOD_5 (0x10)
CORACQ_PRM_STROBE_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_STROBE_DURATION	min = 1 µs max = 42949672 µs step = 1 µs
CORACQ_PRM_STROBE_DELAY	min = 0 µs max = 42949672 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_ENABLE	TRUE FALSE
CORACQ_PRM_TIME_INTEGRATE_DURATION	min = 1 µs max = 42949672 µs step = 1 µs
CORACQ_PRM_CAM_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_OUTPUT_FORMAT	CORACQ_VAL_OUTPUT_FORMAT_MONO8 CORACQ_VAL_OUTPUT_FORMAT_MONO16
CORACQ_PRM_EXT_TRIGGER_ENABLE	CORACQ_VAL_EXT_TRIGGER_OFF (0x1) CORACQ_VAL_EXT_TRIGGER_ON (0x8)
CORACQ_PRM_VIC_NAME	Default Camera Link HS Line Scan Mono
CORACQ_PRM_LUT_MAX	0
CORACQ_PRM_EXT_TRIGGER_DETECTION	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2) CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8)
CORACQ_PRM_LUT_FORMAT	Default = CORDATA_FORMAT_MONO8

CORACQ_PRM_LINE_INTEGRATE_ENABLE	TRUE FALSE
CORACQ_PRM_LINE_INTEGRATE_DURATION	min = 1 nsec max = 4294967295 nsec step = 1 nsec
CORACQ_PRM_LINE_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_FRAME_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_FRAME_TRIGGER_DETECTION	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2) CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8) CORACQ_VAL_DOUBLE_PULSE_RISING_EDGE (0x20) CORACQ_VAL_DOUBLE_PULSE_FALLING_EDGE (0x40)
CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION	CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8)
CORACQ_PRM_SNAP_COUNT	Not Available
CORACQ_PRM_INT_LINE_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_INT_LINE_TRIGGER_FREQ	Default = 5000 Hz
CORACQ_PRM_BIT_ORDERING	CORACQ_VAL_BIT_ORDERING_STD (0x1)
CORACQ_PRM_EXT_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2) CORACQ_VAL_LEVEL_12VOLTS (0x040) CORACQ_VAL_LEVEL_24VOLTS (0x8)
CORACQ_PRM_STROBE_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1)
CORACQ_PRM_EXT_FRAME_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2) CORACQ_VAL_LEVEL_12VOLTS (0x040) CORACQ_VAL_LEVEL_24VOLTS (0x8)
CORACQ_PRM_EXT_LINE_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) : Rev B Only CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MIN	8 Hz
CORACQ_PRM_INT_LINE_TRIGGER_FREQ_MAX	500000 Hz
CORACQ_PRM_MASTER_MODE	Not available
CORACQ_PRM_SHAFT_ENCODER_DROP	min = 0 tick max = 254 tick step = 1 tick
CORACQ_PRM_SHAFT_ENCODER_ENABLE	TRUE FALSE
CORACQ_PRM_EXT_TRIGGER_FRAME_COUNT	min = 1 frame max = 262142 frame step = 1 frame Note: Infinite not supported
CORACQ_PRM_INT_FRAME_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_INT_FRAME_TRIGGER_FREQ	min = 1 milli-Hz max = 1000000000 milli-Hz step = 1 milli-Hz
CORACQ_PRM_STROBE_DELAY_2	Not Available
CORACQ_PRM_FRAME_LENGTH	CORACQ_VAL_FRAME_LENGTH_FIX (0x1) CORACQ_VAL_FRAME_LENGTH_VARIABLE (0x2)
CORACQ_PRM_FLIP	CORACQ_VAL_FLIP_OFF (0x00) CORACQ_VAL_FLIP_HORZ (0x01)
CORACQ_PRM_EXT_TRIGGER_DURATION	min = 0 µs max = 255 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_DELAY	min = 0 µs max = 42949672 µs step = 1 µs
CORACQ_PRM_CAM_TRIGGER_DELAY	min = 0 µs max = 42949672 µs step = 1 µs

CORACQ_PRM_SHAFT_ENCODER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) : Rev B Only CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_EXT_FRAME_TRIGGER_SOURCE (*)	min = 0 max = 5 step = 1
CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE (*)	min = 0 max = 5 step = 1
CORACQ_PRM_EXT_TRIGGER_SOURCE (*)	min = 0 max = 5 step = 1
CORACQ_PRM_SHAFT_ENCODER_MULTIPLY	min = 1 max = 32 step = (2^N)
CORACQ_PRM_EXT_TRIGGER_DELAY	min = 0 max = 16777215 step = 1
CORACQ_PRM_EXT_TRIGGER_DELAY_TIME_BASE	CORACQ_VAL_TIME_BASE_LINE_VALID (0x4) CORACQ_VAL_TIME_BASE_LINE_TRIGGER (0x8) CORACQ_VAL_TIME_BASE_SHAFT_ENCODER (0x40) CORACQ_VAL_TIME_BASE_NS (0x80)
CORACQ_PRM_BAYER_DECODER_ENABLE	Not Available
CORACQ_PRM_EXT_TRIGGER_IGNORE_DELAY	min = 0 max = 42949672 step = 1
CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE (*)	min = 0 max = 6 step = 1
CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE (*)	min = 0 max = 6 step = 1
CORACQ_PRM_EXT_TRIGGER_SOURCE_STR	[0] = Automatic [1] = External Trigger #1 [2] = External Trigger #2 [3] = Board Sync #1 [4] = Board Sync #2 [5] = Software Trigger
CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE_STR	[0] = Automatic [1] = Shaft Encoder Phase A [2] = Shaft Encoder Phase B [3] = Shaft Encoder Phase A & B [4] = Board Sync #1 [5] = Board Sync #2
CORACQ_PRM_VERTICAL_TIMEOUT_DELAY	Not Available
CORACQ_PRM_POCL_ENABLE	TRUE FALSE * For powering up AOC module.
CORACQ_PRM_SHAFT_ENCODER_DIRECTION	CORACQ_VAL_SHAFT_ENCODER_DIRECTION_IGNORE (0x00) CORACQ_VAL_SHAFT_ENCODER_DIRECTION_FORWARD (0x01) CORACQ_VAL_SHAFT_ENCODER_DIRECTION_REVERSE (0x02)
CORACQ_PRM_LINE_TRIGGER_AUTO_DELAY	CORACQ_VAL_LINE_TRIGGER_AUTO_DELAY_DISABLE (0x0) CORACQ_VAL_LINE_TRIGGER_AUTO_DELAY_FREQ_MAX (0x2)
CORACQ_PRM_TIME_STAMP_BASE	CORACQ_VAL_TIME_BASE_US (0x1) CORACQ_VAL_TIME_BASE_LINE_VALID (0X4) CORACQ_VAL_TIME_BASE_LINE_TRIGGER (0X8) CORACQ_VAL_TIME_BASE_SHAFT_ENCODER (0X40) CORACQ_VAL_TIME_BASE_100NS (0x200)
CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE_STR	[0] = Disabled [1] = External Frame Trigger [2] = Reserved [3] = External Trigger Ignore Region [4] = Shaft Encoder Before Mult/Drop [5] = Shaft Encoder After Mult/Drop [6] = Internal Line Trigger
CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE_STR	[0] = Disabled [1] = External Frame Trigger [2] = Reserved [3] = External Trigger Ignore Region [4] = Shaft Encoder Before Mult/Drop [5] = Shaft Encoder After Mult/Drop [6] = Internal Line Trigger

CORACQ_PRM_SHAFT_ENCODER_ORDER	CORACQ_VAL_SHAFT_ENCODER_ORDER_AUTO (0X0) CORACQ_VAL_SHAFT_ENCODER_ORDER_DROP_MULTIPLY (0X1) CORACQ_VAL_SHAFT_ENCODER_ORDER_MULTIPLY_DROP (0X2) * For auto mode, the order is multiply/drop.
CORACQ_PRM_CAM_FRAMES_PER_TRIGGER	Not Available
CORACQ_PRM_LINE_INTEGRATE_TIME_BASE	CORACQ_VAL_TIME_BASE_NS (0X80)
CORACQ_PRM_EXT_TRIGGER_IGNORE_REGION_DURATION	min = 0 µs max = 6553 µs step = 1 µs

ACQ Related Parameters

Parameter	Values
CORACQ_PRM_LABEL	Camera Link HS Mono
CORACQ_PRM_EVENT_TYPE	CORACQ_VAL_EVENT_TYPE_START_OF_FRAME CORACQ_VAL_EVENT_TYPE_END_OF_FRAME CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC CORACQ_VAL_EVENT_TYPE_FRAME_LOST CORACQ_VAL_EVENT_TYPE_DATA_OVERFLOW CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_IGNORED CORACQ_VAL_EVENT_TYPE_EXT_LINE_TRIGGER_TOO_SLOW CORACQ_VAL_EVENT_TYPE_LINK_ERROR CORACQ_VAL_EVENT_TYPE_SHAFT_ENCODER_REVERSE_COUNT_OVERFLOW CORACQ_VAL_EVENT_TYPE_LINE_TRIGGER_TOO_FAST CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER_END
CORACQ_PRM_EVENT_TYPE_EX	CORACQ_VAL_EVENT_TYPE_LINK_LOCK CORACQ_VAL_EVENT_TYPE_LINK_UNLOCK CORACQ_VAL_EVENT_TYPE_CAMERA_MISSED_TRIGGER CORACQ_VAL_EVENT_TYPE_CAMERA_OVERRUN
CORACQ_PRM_SIGNAL_STATUS	CORACQ_VAL_SIGNAL_HSYNC_PRESENT CORACQ_VAL_SIGNAL_VSYNC_PRESENT CORACQ_VAL_SIGNAL_POWER_PRESENT CORACQ_VAL_SIGNAL_POCL_ACTIVE CORACQ_VAL_SIGNAL_POCL_ACTIVE_2 CORACQ_VAL_SIGNAL_LINK_LOCK CORACQ_VAL_SIGNAL_LANE1_LOCK CORACQ_VAL_SIGNAL_LANE2_LOCK CORACQ_VAL_SIGNAL_LANE3_LOCK CORACQ_VAL_SIGNAL_LANE4_LOCK CORACQ_VAL_SIGNAL_LANE5_LOCK CORACQ_VAL_SIGNAL_LANE6_LOCK CORACQ_VAL_SIGNAL_LANE7_LOCK
CORACQ_PRM_FLAT_FIELD_ENABLE	Not Available
CORACQ_PRM_TIME_STAMP	Available
CORACQ_CAP_SERIAL_PORT_INDEX	Not Available
CORACQ_PRM_IMAGE_FILTER_ENABLE	TRUE FALSE
CORACQ_PRM_IMAGE_FILTER_KERNEL_SIZE	CORACQ_VAL_IMAGE_FILTER_KERNEL_SIZE_3x3 (0x4)
CORACQ_CAP_IMAGE_FILTER_KERNEL_VALUE	min = -32768 max = 32767 step = 1
CORACQ_CAP_IMAGE_FILTER_KERNEL_DIVISOR	16384
CORACQ_PRM_SHAFT_ENCODER_REVERSE_COUNT	Max = 65536 ticks
CORACQ_PRM_META_DATA	CORACQ_VAL_META_DATA_PER_LINE_RIGHT (0x2)
CORACQ_PRM_SHAFT_ENCODER_STATUS	CORACQ_VAL_SHAFT_ENCODER_STATUS_DIRECTION_FORWARD/CORACQ_VAL_SHAFT_ENCODER_STATUS_DIRECTION_REVERSE (0x1) CORACQ_VAL_SHAFT_ENCODER_STATUS_TOO_SLOW (0x2) CORACQ_VAL_SHAFT_ENCODER_STATUS_REVERSE_COUNT_OVERFLOW (0x4)
CORACQ_PRM_SHAFT_ENCODER_COUNT	Available

Transfer Related Capabilities

Capability	Values
CORXFER_CAP_NB_INT_BUFFERS	CORXFER_VAL_NB_INT_BUFFERS_AUTO (0x2)
CORXFER_CAP_MAX_XFER_SIZE	4294967040 Bytes
CORXFER_CAP_MAX_FRAME_COUNT	16777215 Frames
CORXFER_CAP_COUNTER_STAMP_AVAILABLE	FALSE
CORXFER_CAP_TRANSFER_SYNC	CORXFER_VAL_TRANSFER_SYNC_SUPPORTED (0x1)

Transfer Related Parameters

Parameter	Values
CORXFER_PRM_EVENT_TYPE CORXFER_PRM_EVENT_TYPE_EX	CORXFER_VAL_EVENT_TYPE_START_OF_FRAME CORXFER_VAL_EVENT_TYPE_END_OF_FRAME CORXFER_VAL_EVENT_TYPE_END_OF_LINE CORXFER_VAL_EVENT_TYPE_END_OF_NLINES CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER
CORXFER_PRM_START_MODE	CORXFER_VAL_START_MODE_ASYNCHRONOUS (0x0) CORXFER_VAL_START_MODE_SYNCHRONOUS (0x1) CORXFER_VAL_START_MODE_HALF_ASYNCHRONOUS (0x2) CORXFER_VAL_START_MODE_SEQUENTIAL (0x3)
CORXFER_PRM_CYCLE_MODE	CORXFER_VAL_CYCLE_MODE_ASYNCHRONOUS (0x0) CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_WITH_TRASH (0x2) CORXFER_VAL_CYCLE_MODE_OFF (0x3) CORXFER_VAL_CYCLE_MODE_SYNCHRONOUS_NEXT_EMPTY_WITH_TRASH (0x5)
CORXFER_PRM_FLIP	CORXFER_VAL_FLIP_OFF (0x0) CORXFER_VAL_FLIP_VERT (0x2)
CORXFER_PRM_INT_BUFFERS	* Depends on acquired image size. By default driver will optimize the number of on-board buffers.
CORXFER_PRM_EVENT_COUNT_SOURCE	CORXFER_VAL_EVENT_COUNT_SOURCE_DST (0x1) CORXFER_VAL_EVENT_COUNT_SOURCE_SRC (0x2)
CORXFER_PRM_BUFFER_TIMESTAMP_MODULE	CORXFER_VAL_BUFFER_TIMESTAMP_MODULE_ACQ (0x1) CORXFER_VAL_BUFFER_TIMESTAMP_MODULE_XFER (0x13)
CORXFER_PRM_BUFFER_TIMESTAMP_EVENT (ACQ Related)	CORACQ_VAL_EVENT_TYPE_START_OF_FRAME (0x80000) CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER (0x1000000)
CORXFER_PRM_BUFFER_TIMESTAMP_EVENT (XFER Related)	CORXFER_VAL_EVENT_TYPE_END_OF_FRAME (0x800000)
CORXFER_PRM_LINE_MERGING	CORXFER_VAL_LINE_MERGING_AUTO (0x0) CORXFER_VAL_LINE_MERGING_OFF (0x2)

General Outputs #1: Related Capabilities (for GIO Module #0)

These are the User Interface Outputs available on connector J1.

Capability	Values
CORGIO_CAP_IO_COUNT	4 I/Os (Rev A) 8 I/Os (Rev B)
CORGIO_CAP_DIR_OUTPUT	0xf (Rev A) 0xff (Rev B)
CORGIO_CAP_DIR_TRISTATE	0xf (Rev A) 0xff (Rev B)
CORGIO_CAP_EVENT_TYPE	Not Available
CORGIO_CAP_READ_ONLY	0x01 (* depends on strobe outputs reserved for acquisition device)

General Outputs #1: Related Parameters (for GIO Module #0)

Parameter	Values
CORGIO_PRM_LABEL	General Outputs #1
CORGIO_PRM_DEVICE_ID	0
CORGIO_PRM_OUTPUT_TYPE	CORGIO_VAL_OUTPUT_TYPE_LVTTL (0x20)
CORGIO_PRM_CONNECTOR	CORGIO_VAL_CONNECTOR_1 (0x1)

General Inputs #1: Related Capabilities (for GIO Module #1)

These are the User Interface Inputs available on connector J1.

Capability	Values
CORGIO_CAP_IO_COUNT	4 I/Os
CORGIO_CAP_DIR_OUTPUT	0x0
CORGIO_CAP_DIR_TRISTATE	0x0
CORGIO_CAP_EVENT_TYPE	CORGIO_VAL_EVENT_TYPE_RISING_EDGE (0x1) CORGIO_VAL_EVENT_TYPE_FALLING_EDGE (0x2)
CORGIO_CAP_READ_ONLY	0x03 (* depends on external trigger inputs reserved for acquisition device)

General Inputs #1: Related Parameters (for GIO Module #1)

Parameter	Values
CORGIO_PRM_LABEL	General Inputs #1
CORGIO_PRM_DEVICE_ID	1
CORGIO_PRM_INPUT_LEVEL	CORGIO_VAL_INPUT_LEVEL_TTL (0x1) CORGIO_VAL_INPUT_LEVEL_422 (0x2) CORGIO_VAL_INPUT_LEVEL_24VOLTS (0x8) CORGIO_VAL_INPUT_LEVEL_12VOLTS (0x40)
CORGIO_PRM_CONNECTOR	CORGIO_VAL_CONNECTOR_1 (0x1)

Bidirectional General I/Os: Related Capabilities (for GIO Module #2)

These are the Open Interface I/Os available on connector J5

Capability	Values
CORGIO_CAP_IO_COUNT	8 I/Os
CORGIO_CAP_DIR_OUTPUT	0xff
CORGIO_CAP_DIR_TRISTATE	0xff
CORGIO_CAP_EVENT_TYPE	Not Available
CORGIO_CAP_READ_ONLY	0x03 (* depends on board syncs reserved for acquisition device)

Bidirectional General I/Os: Related Parameters (for GIO Module #2)

Parameter	Values
CORGIO_PRM_LABEL	Bidirectional General I/Os #1
CORGIO_PRM_DEVICE_ID	2
CORGIO_PRM_OUTPUT_TYPE	CORGIO_VAL_OUTPUT_TYPE_LVTTL (0x20)
CORGIO_PRM_INPUT_LEVEL	CORGIO_VAL_INPUT_LEVEL_LVTTL (0x20)
CORGIO_PRM_CONNECTOR	CORGIO_VAL_CONNECTOR_2 (0x2)

Sapera Servers and Resources

A Sapera Server is an abstract representation of a physical device like a frame-grabber or camera. When using the SapAcquisition or SapAcqDevice constructors, the location parameter specifies the server to use to create the object. Use the Sapera Configuration utility to find the names and indices of all Sapera servers in your system.

In Sapera LT all frame grabbers are configured using the SapAcquisition class. All CLHS cameras are GenCP compliant and are configured in Sapera LT using the SapAcqDevice class.

Note: Currently, CLHS cameras do not have their own server, therefore it is available under the Xtium_CLHS server. For example, in CamExpert the Xtium server displays both the frame grabber and camera resources.

Servers	Resources			
Name	**Type**	**Name**	**Index**	**Description**
Xtium-CLHS_PX4_1	Acquisition Module	Camera Link HS Mono	0	CLHS Monochrome Camera
	Acquisition Device	*<Device Name>* *Name of camera	0	CLHS Camera
	GIO Module	General Outputs #1	0	4 General Outputs
		General Inputs #1	1	4 General Inputs
		Bidirectional General I/Os #1	2	8 Bidirectional General I/Os

Technical Specifications

Xtium-CLHS PX4 Board Specifications

Digital Video Input & Controls

Input Type	Camera Link HS Specifications Rev 1.0 compliant
Common Pixel Formats	Camera Link HS for 8, 10, 12, 14 and 16-bit mono
Scanning	Area scan and Line scan
Resolution *note: these are Xtium-CLHS PX4 maximums, not Camera Link HS specifications*	Horizontal Minimum: 32 Pixels per lane Horizontal Maximum: 8-bits/pixel x 16k Pixels/line 16-bits/pixel x 8k Pixels/line Vertical Minimum: 1 line Vertical Maximum: up to 16,000,000 lines—for area scan sensors infinite line count—for linescan sensors
Bit Transfer Rate	3.125 Gbps
Image Buffer	Available with 512 MB
Bandwidth to Host System	Approximately 1.7GB/s (maximum obtained is dependent on firmware loaded and PC characteristics)
Controls	Compliant with Teledyne DALSA Trigger-to-Image Reliability framework Comprehensive event notifications Timing control logic for camera triggers and strobe signals Rev A: 4 opto-coupled general inputs (TTL/12V/24V) where only 1 input can be connected to a differential input signal (RS-422): ECO #22719 and higher needed. Rev B:4 differential opto-coupled general inputs (RS-422/TTL/12V/24V). Trigger inputs are programmable as active high or low (edge or level trigger, at maximum input frequency of 100 KHz) External trigger latency less than 100 nsec 4 (Rev A) or 8 (Rev B) LVTTL general Outputs where 1 is shared as Strobe Output Quadrature (phase A & B) shaft encoder inputs for external web synchronization: RS-422 or TTL (Rev B Only) input (mutually exclusive) maximum frequency is 5 MHz Supports camera Data Forwarding up to 5 additional boards Supports multi-camera synchronization of 2 to 4 boards I/O available on a DH60-27P connector (J1) and on 26-pin SHF-113-01-L-D-RA (J4)
Processing *Dependent on user loaded firmware configuration*	3x3 Image Filter (Convolution) Output Lookup Table Contact Teledyne DALSA for availability. Bayer Mosaic Filter Contact Teledyne DALSA for availability.

Host System Requirements

Xtium-CLHS PX4 Dimensions

Approximately 4 in. (10 cm) wide by 4 in. (10 cm) high

General System Requirements for the Xtium-CLHS PX4

- PCI Express Gen2 x4 slot compatible;
  (will work in Gen1 x4 slot with reduced bandwidth to host)
- On some computers the Xtium-CLHS PX4 may function installed in a x16 slot. The computer documentation or direct testing by the user is required.
- Xtium-CLHS PX4 operates correctly when installed in a multi-processor system (including Hyper-Threading multi-core processors).

Operating System Support

Windows 7, Windows 8 and Windows 10, each in either 32-bit or 64-bit

Environment

Ambient Temperature:	10° to 50°C (operation) -40° to 75°C (storage)
Relative Humidity:	5% to 90% non-condensing (operating) 0% to 95% (storage)
MTBF @40°C	36.4 years

Note: Ensure adequate airflow for proper functioning of the board across the entire temperature range of 10 – 50°C . We recommend airflow measuring 80 LFM (linear feet per minute) across the surface of the board.

Power Requirements while grabbing

+3.3V:	0.133A
+12V:	1.325A

EMI Certifications

EC & FCC DECLARATION OF CONFORMITY

We : Teledyne DALSA inc.
7075 Place Robert-Joncas, Suite 142,
St. Laurent, Quebec, Canada, H4M 2Z2

Declare under sole legal responsibility that the following products conform to the protection requirements of council directive 2004/108/EC on the approximation of the laws of member states relating to electromagnetic compatibility:

Xtium-CLHS PX4

The products to which this declaration relates are in conformity with the following relevant harmonized standards, the reference numbers of which have been published in the Official Journal of the European Communities:

EN55022 (CISPR22:2008)
EN61000-3-2:2005, A1:2008, A2:2009
EN61000-3-3:2008
EN61000-4-2:2008
EN61000-4-3:2006, A1:2007, A2:2010
EN61000-4-4:2012
EN61000-4-5:2005
EN61000-4-6:2008
EN61000-4-8:2009
EN61000-4-11:2004

Further declare under our sole legal responsibility that the product listed conforms to the code of federal regulations CFR 47 part 15 (2012), subpart B, for a class A product.

St. Laurent, Canada — Location
2014-07-17 — Date

Eric Carey, ing.
Director,
Research and Development

Figure 21: EMI Certifications

Connector and Switch Locations

Xtium-CLHS PX4 Board Layout Drawing

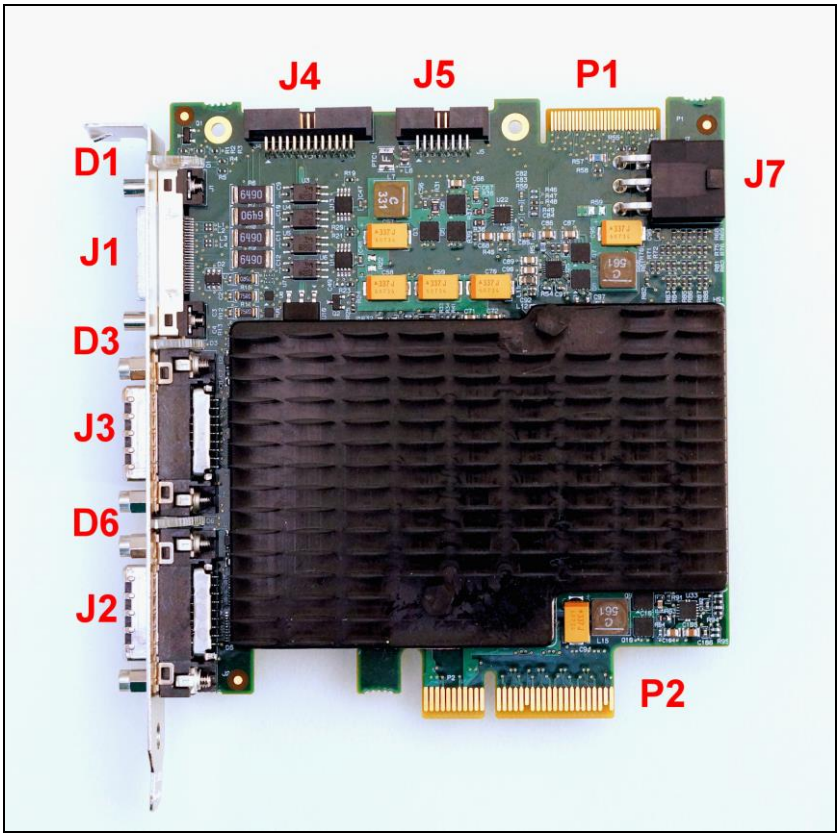


Figure 22: Board Layout

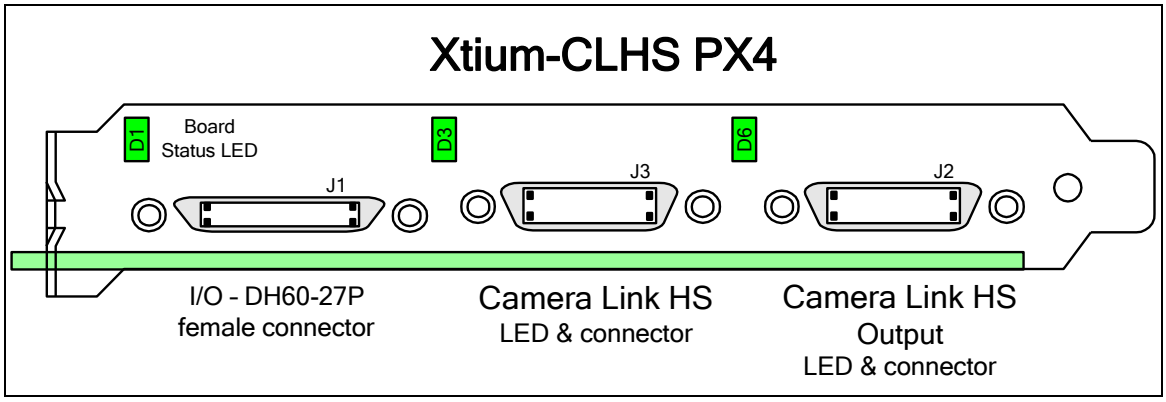
Connector / LED Description List

The following table lists components on the Xtium-CLHS PX4 board. Detailed information concerning the connectors/LEDs follows this summary table.

Location	Description	Location	Description
J1	External I/O Signals connector (DH60-27P)	J5	Multi Board Sync
D1	Boot-up/PCIe Status LED (refer to text)	J7	PC power to J1
J3	Camera Link HS Input Connector	P2	PCIe x4 computer bus connector (Gen2 compliant slot preferred)
D3	Camera Link HS status LED	P1	Reserved
J4	Internal I/O Signals connector (26-pin SHF-113-01-L-D-RA)	J2	Camera Link HS Output Connector (used for Data Forwarding)
D6	Data Forwarding status LED		

Connector and Switch Specifications

Xtium-CLHS PX4 End Bracket Detail



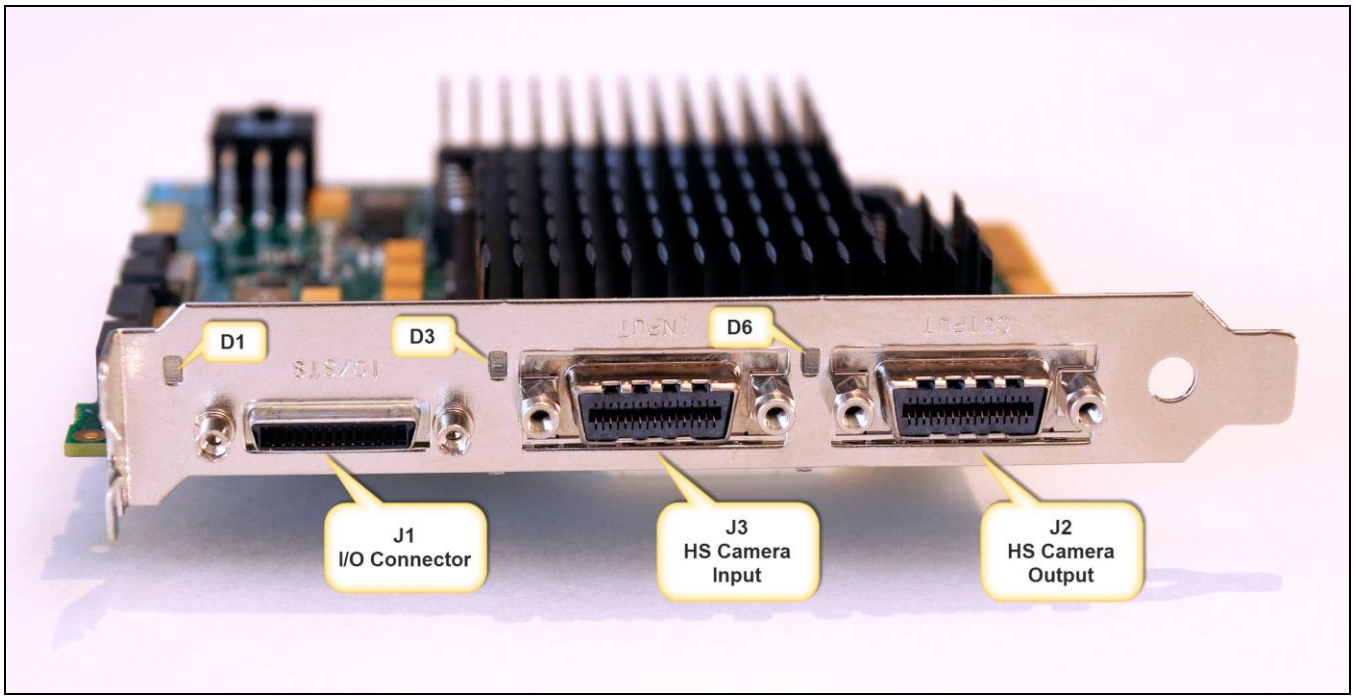


Figure 23: End Bracket Details

The hardware installation process is completed with the connection of a supported camera to the Xtium-CLHS PX4 board using a Camera Link HS cable (see Camera Link HS Cables).

- The Xtium-CLHS PX4 board supports one Camera Link HS camera output.
- Connect the camera to the J3 connector with a Camera Link HS cable.

Data Forwarding Setup

Distributed processing of high bandwidth image data is easily configured by inter-connecting multiple Xtium-CLHS boards. The following description and block diagram shows the simple physical setup. The user has total control to the actual distributed processing task divisions and algorithms.

- Connect a camera to J3 of the first Xtium-CLHS board installed in the first PC. This board is defined as the "Data Forwarding Master".
- Using a second Camera Link HS cable, connect J2 of the Data Forwarding Master Xtium-CLHS board to J3 of second Xtium-CLHS installed in a separate computer or the same as the first Xtium if it can manage the processing. This second board is defined as the "Data Forwarding Slave #1".
- Camera Link HS cables used to interconnect Xtium-CLHS boards could be up to 15 meters.
- Optionally, the J2 connector of the Data Forwarding Slave #1 Xtium-CLHS board can connect to J3 of a third Xtium-CLHS ("Data Forwarding Slave #2").
- The number of Data Forwarding Slave boards should not exceed 5, for a total of 6 boards. The Xtium CLHS boards can either have separate computers or share computers dependent on the distributed processing requirements.
- The Xtium-CLHS driver will automatically detect whether a board is connected to a camera (becoming the Data Forwarding Master) or is connected to forwarded data (becoming a Data Forwarding Slave).
- Each Data Forwarding Slave board has full control of the camera data portion transferred to the host computer for processing.
- The use of the CORACQ_PRM_DATA_VALID parameter can be used in order for all frame grabbers to acquire the same triggered frames and/or lines. Once the parameter is enabled on the master frame grabber, a data valid signal is initiated by the master frame grabber through the camera trigger message. The camera will then pass the data valid control in the video packets. On slave frame grabbers that also have the data valid enabled, only the video packets that have the data valid control enabled will be acquired.

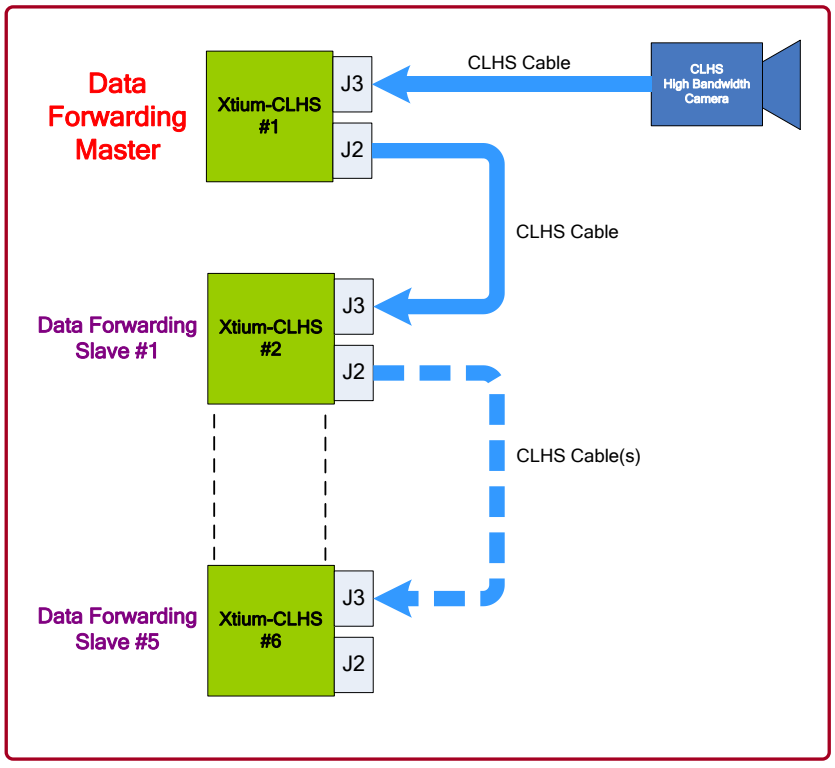


Figure 24: Data Forwarding Block Diagram

Connecting to Dual Output CLHS Cameras

Distributed processing of high bandwidth image data generated by a Dual Output CLHS camera is easily configured by connecting the camera to multiple Xtium-CLHS boards. The following description and block diagram shows the simple physical setup. The user has total control of the actual distributed processing task division and algorithms.

- Connect camera output #1 to J3 of the first Xtium-CLHS board installed in the first PC. This board is defined as the "Master Frame Grabber".
- Using a second Camera Link HS cable, connect camera output #2 to J3 of a second Xtium-CLHS board installed in a separate computer or the same as the first Xtium if it can manage the processing. This second board is defined as the "Camera Slave Port Frame Grabber".
- The Camera Slave Port Frame Grabber must set CORACQ_VAL_CLHS_CONFIGURATION_CAM_PORT_SLAVE in the parameter CORACQ_PRM_CLHS_CONFIGURATION in order to configure the frame grabber as the one connected to a camera slave port. In this mode, camera controls are written via the Camera Master Port Frame Grabber only.
- Dual output cameras control which data portion is transferred by each camera output, as designed by the camera manufacturer.
- The use of the CORACQ_PRM_DATA_VALID parameter can be used in order for all frame grabbers to acquire the same triggered frames and/or lines. Once the CORACQ_PRM_DATA_VALID is enabled on the master frame grabber, a data valid signal is initiated by the master frame grabber through the camera trigger message. The camera will then pass the data valid control in the video packets. On Camera Slave Port Frame Grabbers that also have the data valid enabled, only the video packets that have the data valid control enabled will be acquired.

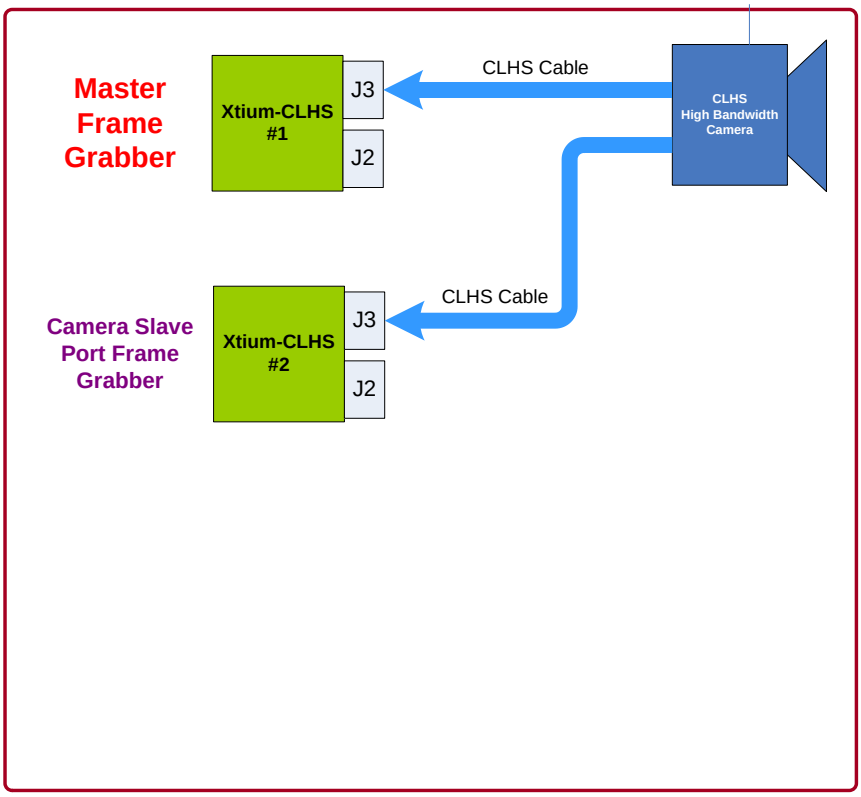


Figure 25: Dual Camera Output Connection Block Diagram

Status LEDs Functional Descriptions

Three LED indicators, mounted on the board bracket, provide information on board and connection status as per the tables below.

D1: Boot-up/PCIe Status LED — Provides general board status information

D3: Camera Link HS status LED — Indicates data status for J3 when connected to a camera or when receiving forwarded data from another Xtium-CLHS system.

D6: Camera Link HS Forwarded Data status LED — Indicates connection status when the data forwarding connector J2 is connected to another Xtium-CLHS.

D1: Boot-up/PCIe Status LED

Color	State	Description
Red	Solid	FPGA firmware not loaded
Green	Solid	Normal FPGA firmware loaded, Gen2 speed, link width x4
Green	Flashing	Normal FPGA firmware loaded, Gen1 speed, link width x4
Yellow	Solid	Normal FPGA firmware loaded, Gen2 speed, link width not x4
Yellow	Flashing	Normal FPGA firmware loaded, Gen1 speed, link width not x4
Blue	Solid	Safe FPGA firmware loaded, Gen2 speed
Blue	Flashing	Safe FPGA firmware loaded, Gen1 speed
Red	Flashing	PCIe Training Issue – Board will not be detected by computer

D3: Camera Link HS Status LED (when a camera is connected)

The Xtium-CLHS PX4 implements the mandatory LED states defined by the Camera Link HS Specification v1.0 RC5. The first column – Priority, defines the signaling order when multiple events are reported simultaneously.

This LED status table reflects activity on input connector J3 when a camera is connected (i.e. the Xtium is the Data Forwarding Master.

LED State	Description
Off	Device not powered and/or waiting for software.
Flashing Orange Medium ~2Hz	The devices have established communication and determined that they are not interoperable. This would be the case when the frame grabber and the camera have different pixel depth, pixel format and/or number of lanes.
Flashing Green Medium ~2Hz	Hardware is fine, but connection not established or recently broken.
Constant Green	Link established and data transfer may take place.
Flashing Green Fast ~4Hz	Acquisition in progress.

D3: Camera Link HS Status LED (as Data Forwarding receiver)

When the Xtium-CLHS PX4 does not have a camera connected but is used as a Data Forwarding Slave, (that is, the board receives data on J3 from another Xtium in a separate computer), the LED D3 describes these two additional conditions.

LED Color	State	Description
Green	Flashing	Connection not established on input connector J3
Green	Constant	Link established on input connector J3 and data transfer may take place.

D6: Data Forwarding Status LED

D6 defines the connection status for when the Camera Link HS output J2 is forwarding acquisition data to another Xtium-CLHS in a separate computer. Note that the Xtium-CLHS PX4 data forwarding feature is not part of the standard CLHS specifications.

LED Color	State	Description
Off	Constant	Connection not established on input connector J3 of the receiving Xtium-CLHS
Green	Constant	Link established with the receiving Xtium-CLHS and data transfer may take place.

J2: Data Forwarding Connector

Note: The Data Forwarding connector on the Xtium-CLHS PX4 has the same specifications as the Camera Link HS camera connector (J3) defined in the AIA document "*Specifications of the Camera Link HS Interface Standard for Digital Cameras and Frame Grabbers" version 1.0 RC5*, ©2012 AIA. Typically there is no need to be concerned with the physical pinout of the connector or cables. Refer to their site www.visiononline.org for additional information.

J3: Camera Link HS Connector

Note: The Camera Link HS camera connector is defined in the AIA document "*Specifications of the Camera Link HS Interface Standard for Digital Cameras and Frame Grabbers" version 1.0 RC5*, ©2012 AIA. Typically there is no need to be concerned with the physical pinout of the connector or cables. Refer to their site www.visiononline.org for additional information.

J1: External I/O Signals Connector (Female DH60-27P)

Warning: J1 and J4 have the same pinout assignment. Signals are routed to both connectors directly from their internal circuitry. Therefore never connect both J1 and J4 to external devices at the same time.
See DH40-27S Cable to Blunt End (OR-YXCC-27BE2M1, Rev B1) and Cable assemblies for I/O connector J4 for available cables.

J4: Internal I/O Signals Connector (26-pin SHF-113-01-L-D-RA)

Important: The table below describes the I/O signals available on both J1 and J4.
(*applies to* ***Xtium-CLHS PX4 rev. B***)

Use only one of the two I/O connectors — never both!

Xtium-CLHS PX4 rev. B

Description	Pin #	Pin #	Description
Ground	1	15	General Input 3 (+)
RS-422 Shaft Encoder Phase A (-)	2	16	General Input 4 (+)
TTL/RS-422 Shaft Encoder Phase A (+) (*see note 3*)	3	17	General Input 4 (-)
Ground	4	18	General Input 3 (-)
RS-422 Shaft Encoder Phase B (-)	5	19	Power Output 5 Volts, 100mA max
TTL/RS-422 Shaft Encoder Phase B (+)	6	20	External Trigger Input 2 or General Input 2 (-)
External Trigger Input 1/General Input 1 (-)	7	21	General Output 3
External Trigger Input 1/General Input 1 (+)	8	22	General Output 4
External Trigger Input 2/General Input 2 (+)	9	23	General Output 5
Ground	10	24	General Output 6
Strobe 1 / General Output 1 (*See note 2*)	11	25	General Output 7
Strobe 2 / General Output 2 (*See note 2*)	12	26	General Output 8
Ground	13	27	NC
Power Output 12 Volts, 350mA max (*from Aux Power Connector, see J7*)	14		

Important: The table below describes the I/O signals available on both J1 and J4.
(*applies to* ***Xtium-CLHS PX4 rev. A***)

Use only one of the two I/O connectors — never both!

Xtium-CLHS PX4 rev. A

Description	Pin #	Pin #	Description
Ground	1	15	General Input 3
RS-422 Shaft Encoder Phase A (-)	2	16	General Input 4
RS-422 Shaft Encoder Phase A (+) (*see note 3*)	3	17	Reserved
Ground	4	18	Reserved
RS-422 Shaft Encoder Phase B (-)	5	19	Reserved
RS-422 Shaft Encoder Phase B (+)	6	20	Reserved
General Input Common External Trigger Input 1 (-) General Input 1 (-)	7	21	General Output 3
External Trigger Input 1 (+) General Input 1 (+) (*Opto-coupled — see note 1*)	8	22	General Output 4
External Trigger Input 2 / General Input 2	9	23	Reserved
Ground	10	24	Reserved
Strobe 1 General Output 1 (*See note 2*)	11	25	Reserved
Strobe 2 General Output 2	12	26	Reserved
Ground	13	27	Reserved (J1 only)
Power Output 12 Volts, 350mA max (*from Aux Power Connector, see J7*)	14		

Note 1: General Inputs / External Trigger Inputs Specifications

Each of the four General Inputs are opto-coupled and able to connect to single ended source signals. General Input 1 and 2 can also act as External Trigger Inputs. See "Board Information" user settings. These inputs generate individual interrupts and are read by the Sapera application.

- **Note:** On Rev A, only General Input 1 can be connected to a differential source signal. ECO *#22719 needed.* In this specific case, the other 3 General Inputs cannot be used.
- The following figure is typical for each General Input.

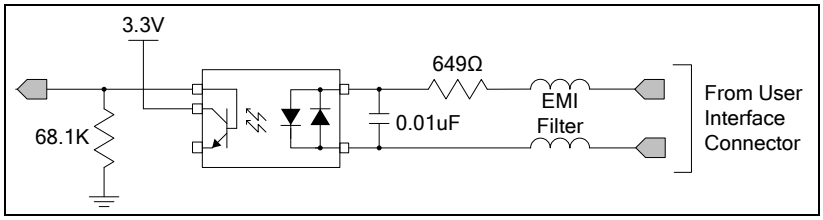


Figure 26: General Inputs Electrical Diagram

Input Details:

- Maximum input voltage is 26V.
- Maximum input signal frequency is 100 KHz.
- Each input has a 649-ohm series resistor on the opto-coupler input.
- The 0.01uF capacitor provide high frequency noise filtering.
- Minimum current is dependent on input voltage applied: $I_{optoin}(min) = (V_{optoin} - 0.5)/649\Omega$
- The switch point is software programmable to support differential RS-422 or single ended TTL, 12V or 24V input signals.

For External Trigger usage:

- Input signal is "debounced" to ensure that no voltage glitch is detected as a valid transition. This debounce circuit time constant can be programmed from 1μs to 255μs. Any pulse smaller than the programmed value is blocked and therefore not seen by the board. If no debounce value is specified (value of 0μs), the minimum value of 1μs will be used.
- Refer to Sapera parameters:
  CORACQ_PRM_EXT_TRIGGER_SOURCE
  CORACQ_PRM_EXT_TRIGGER_ENABLE
  CORACQ_PRM_EXT_TRIGGER_LEVEL
  CORACQ_PRM_EXT_FRAME_TRIGGER_LEVEL
  CORACQ_PRM_EXT_TRIGGER_DETECTION
  CORACQ_PRM_EXT_TRIGGER_DURATION
- See also *.cvi file entries:
  External Trigger Level, External Frame Trigger Level, External Trigger Enable, External Trigger Detection.
- External Trigger Input 2 used for two pulse external trigger with variable frame length line scan acquisition.

Trigger Signal Total Delay

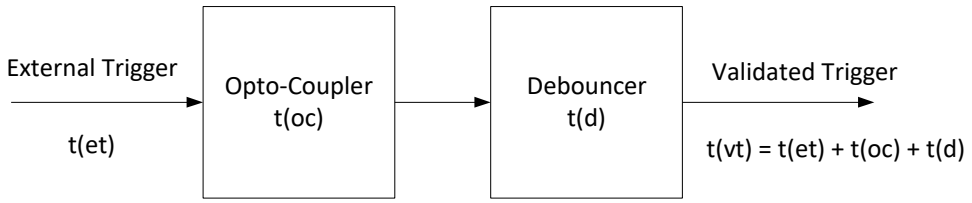


Figure 27: External Trigger Input Validation & Delay

Let	t(et) = time of external trigger in µs t(oc) = time opto-coupler takes to change state (time varies dependent on input voltage) t(d) = user set debounce duration from 1 to 255µs t(vt) = time of validated trigger in µs

Note: Teledyne DALSA recommends using the fastest transition to minimize the time it takes for the opto-coupler to change state.

If the duration of the external trigger is > t(oc) + t(d), then a valid acquisition trigger is detected.

It is possible to emulate an external trigger using the software trigger which is generated by a function call from an application.

Input Switching Points and Propagation Delay

Trigger Level	Switch Point	Propagation Delay t(oc) (*rising edge signal* ↑)	Propagation Delay t(oc) (*falling edge signal* ↓)
RS-422	1.6V	1.75 µs	5.5 µs
TTL	1.6V	1.75 µs	5.5 µs
12V	6V	2.6 µs	2.6 µs
24V	12V	1.9 µs	3.1 µs

Block Diagram: Connecting External Drivers to General Inputs on J1

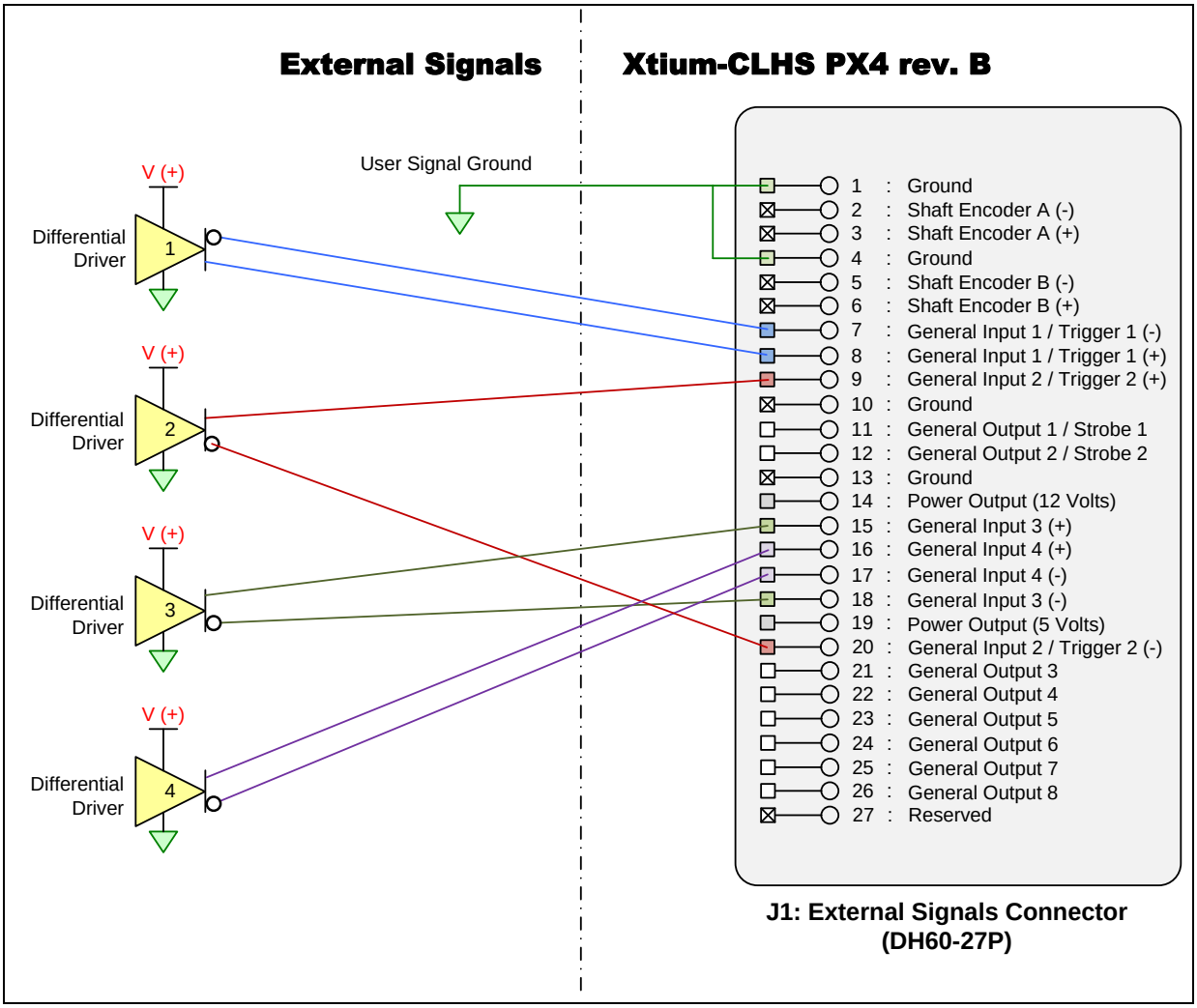


Figure 28:Rev B: External Signals Connection Diagram

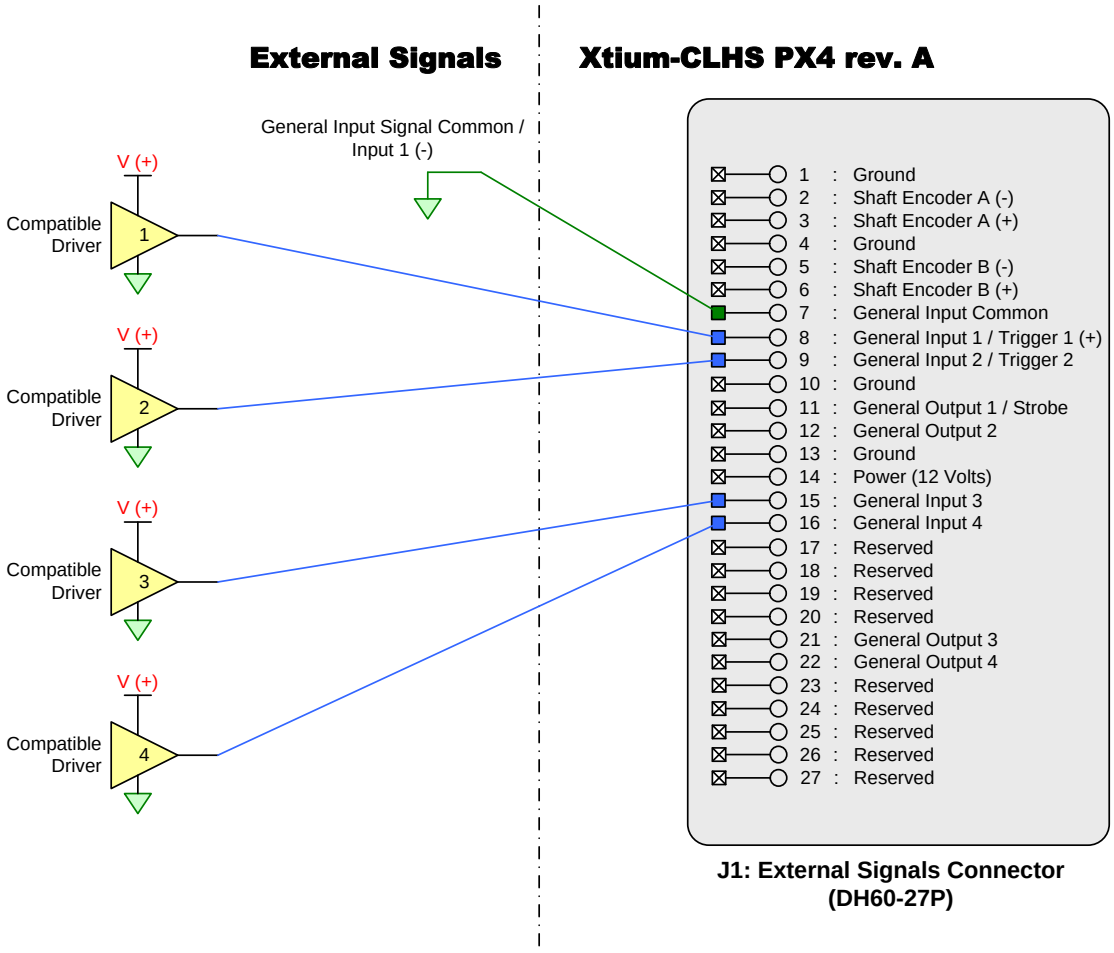


Figure 29:Rev A: External Signals Connection Diagram

External Driver Electrical Requirements

The Xtium-CLHS PX4 allows user selected (software programmable) input switching points to support differential (RS-422) input signals and single ended (TTL, 12V or 24V) input signals. The following table defines the external signal voltage requirements from the driver circuits connected to the Xtium external inputs.

Input Level	Description	MIN	MAX
RS-422	Output Voltage High (V_{OH})	2.4 V	13.0 V
	Output Voltage Low (V_{OL})	-2.4 V	-13.0 V
TTL	Output Voltage High (V_{OH})	2.4 V	5.5 V
	Output Voltage Low (V_{OL})	0 V	0.8 V
12V	Output Voltage High (V_{OH})	9 V	13.2 V
	Output Voltage Low (V_{OL})	0 V	3 V
24V	Output Voltage High (V_{OH})	18 V	26.4 V
	Output Voltage Low (V_{OL})	0 V	6 V

Note 2: General Outputs /Strobe Output Specifications

Each of the eight (four on Rev A) General Outputs are TTL (3.3V) compatible. General Output 1 also functions as the Strobe Output controlled by Sapera strobe control functions. See "Board Information" user settings. The following figure is typical for each General Output.

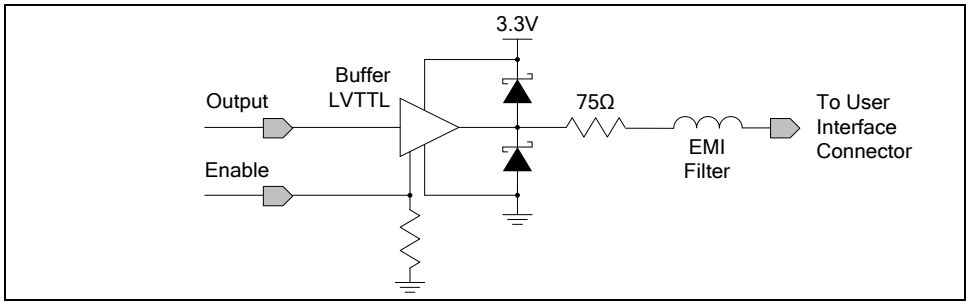


Figure 30: General Outputs Electrical Diagram

Output Details:

- Each output has a 75-ohm series resistor
- The 2 diodes protects the LVTTL buffer against overvoltage
- Each output is a tri-state driver, enabled by software
- Minimum guaranteed output current is +/- 24mA @ 3.3V
- Maximum output current is 50mA
- Maximum short circuit output current is 44mA
- Minimum voltage for output level high is 2.4V, while maximum voltage for output low is 0.55V
- Maximum output switching frequency is limited by driver and register access on the PCIe bus.

For Strobe Usage:

- Refer to Sapera Strobe Methods parameters:
  CORACQ_PRM_STROBE_ENABLE
  CORACQ_PRM_STROBE_POLARITY
  CORACQ_PRM_STROBE_LEVEL
  CORACQ_PRM_STROBE_METHOD
  CORACQ_PRM_STROBE_DELAY
  CORACQ_PRM_STROBE_DURATION
- See also *.cvi file entries:
  Strobe Enable, Strobe Polarity, Strobe Level, Strobe Method, Strobe Delay, Strobe Duration.

Block Diagram: Connecting External Receivers to the General Outputs

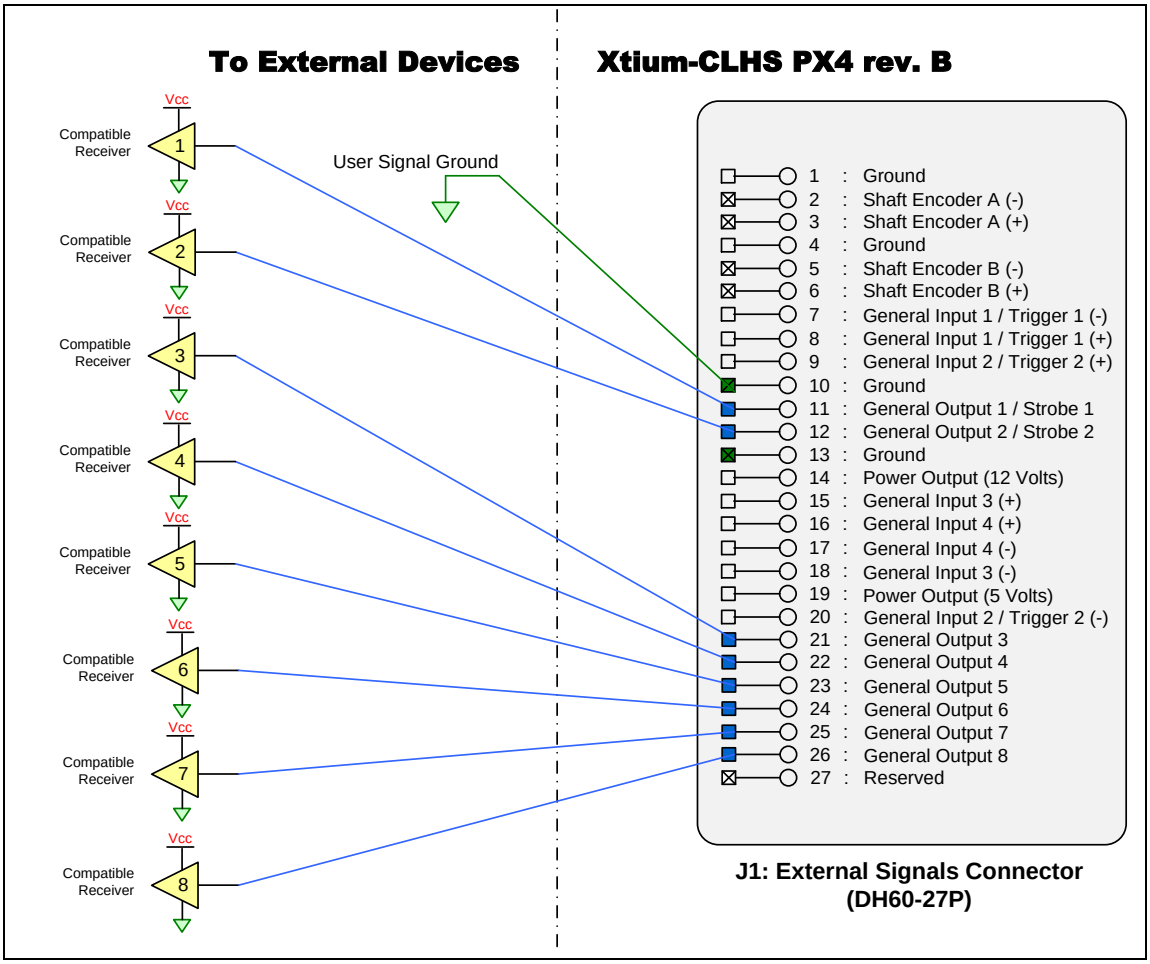


Figure 31:Rev B: Output Signals Connection Diagram

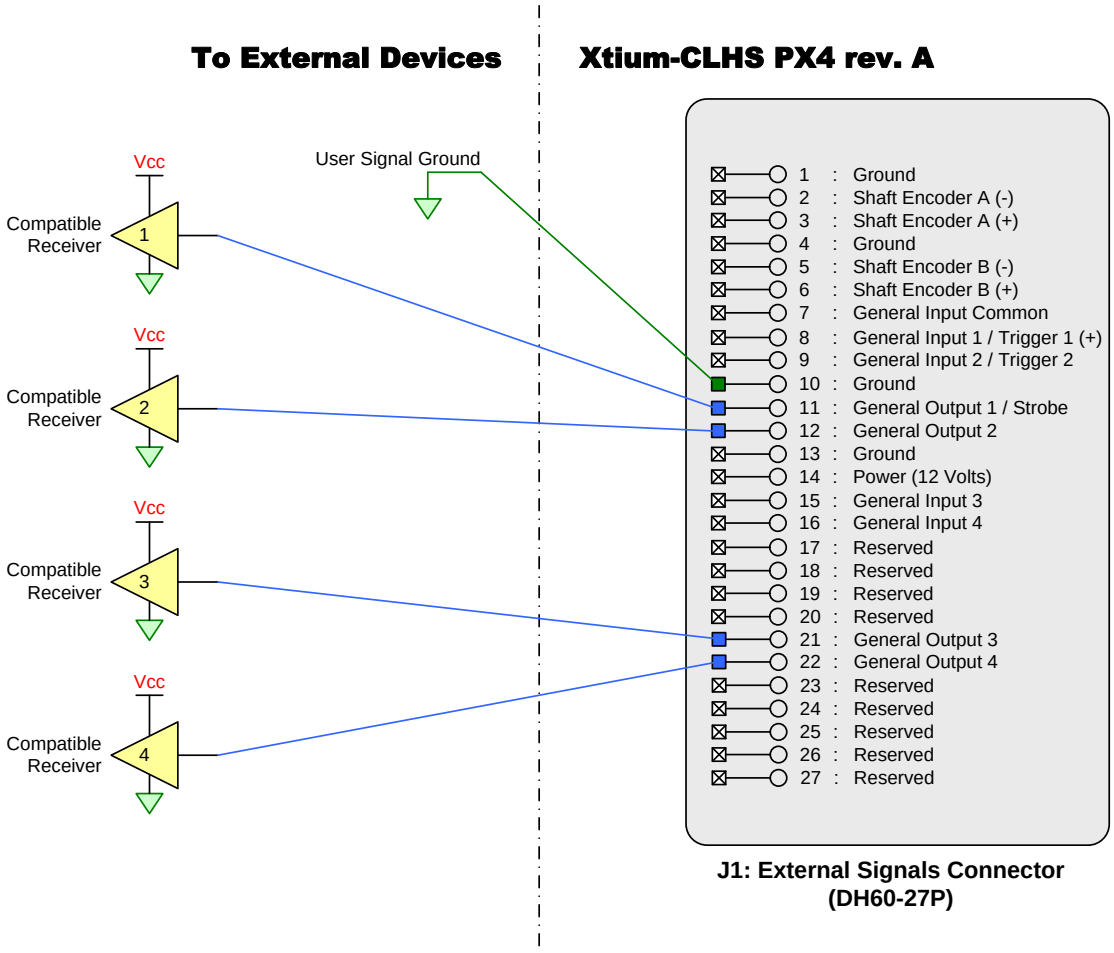


Figure 32:Rev A: Output Signals Connection Diagram

External Receiver Electrical Requirements

- Xtium General Outputs are standard TTL logic levels.
- External receiver circuits must be compatible to TTL signals.

Input Level	Description	MIN	MAX
TTL	Input Voltage High (V_{IH})	2.0 V	–
	Input Voltage Low (V_{IL})	–	0.8 V

Note 3: RS-422/TTL Shaft Encoder Input Specifications

Dual Quadrature Shaft Encoder Inputs (phase A and phase B) connect to differential signals (RS-422), single ended signals, or TTL signals (Rev B Only). The figure below shows the simplified representation of these inputs.

	**WARNING:** When connecting shaft encoders to Xtium-CLHS PX4, make sure to connect a common ground between the shaft encoder and the frame grabber. See RED boxed connections in the diagram below. Failure to follow the described instructions could damage the board resulting in the shaft encoder functionality not working properly. Ensure that these grounding measures are followed when migrating from boards with opto-coupled shaft encoders (such as the Xcelera).

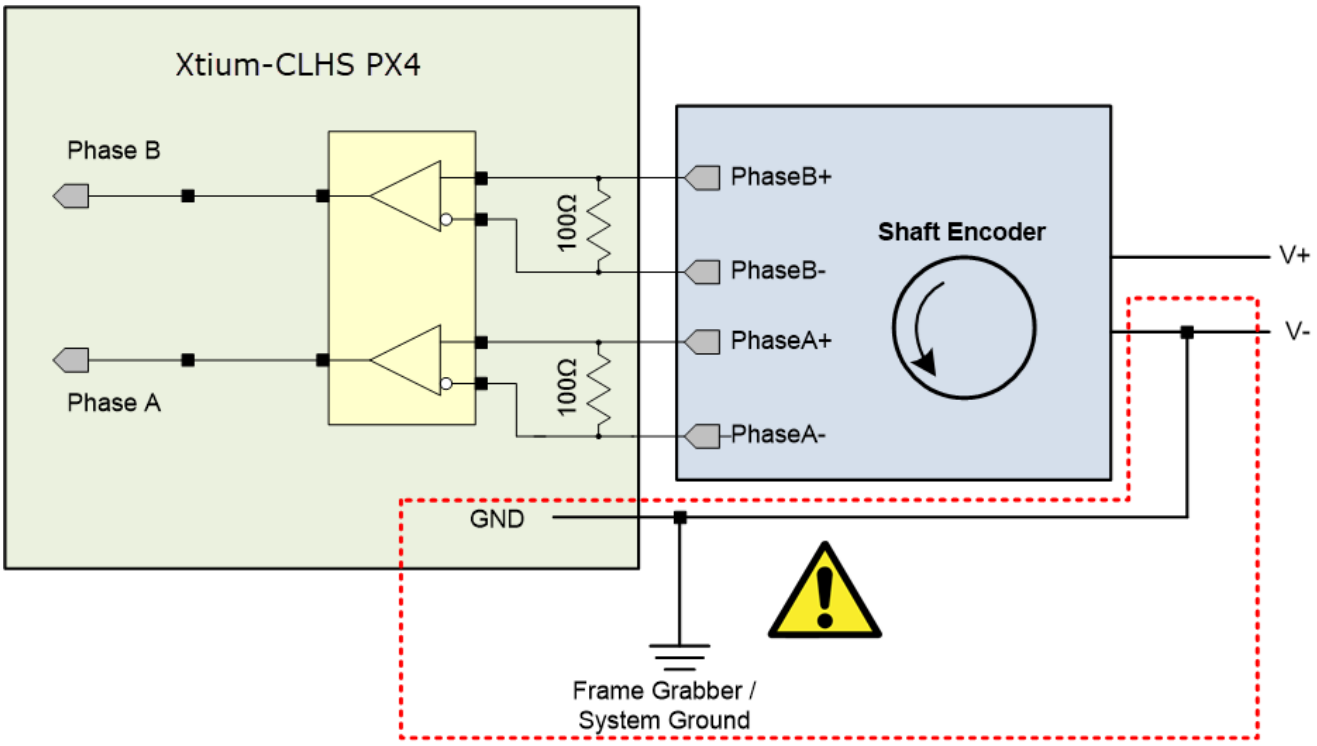


Figure 33: RS-422 Shaft Encoder Input Electrical Diagram

- The shaft encoder ground and the Xtium-CLHS PX4 computer system ground must be connected together.
- RS-422 Input Specifications:
  - Input signals must meet the following
    - Maximum differential input voltage is +/- 7V.
    - Minimum differential voltage level is +/- 200mV.
  - Both inputs have a 100-ohm differential resistor.

- TTL Input Specifications (Rev B Only):
  - Input signals must meet the following
    - Input voltage high minimum = 2V
    - Input voltage low maximum = 0.8V
  - Input Current Max = 5mA

- RS-422 differential line receiver used is am26lv32.
- Maximum input signal frequency is 10 MHz.
- The Xtium-CLHS provides ESD filtering on-board.
- See Line Trigger Source Selection for Line scan Applications for more information.
- Refer to Sapera parameters:
  CORACQ_PRM_SHAFT_ENCODER_ENABLE CORACQ_PRM_SHAFT_ENCODER_DROP
  or refer to CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE
  CORACQ_PRM_EXT_LINE_TRIGGER_DETECTION
  CORACQ_PRM_EXT_LINE_TRIGGER_LEVEL (fixed at RS-422)
  CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE
- See also *.cvi file entries:
  Shaft Encoder Enable, Shaft Encoder Pulse Drop,
  or see External Line Trigger Enable, External Line Trigger Detection, External Line Trigger Level, External Line Trigger Source.
- For single ended signals, connect a bias voltage to the RS-422 (-) input to ensure correct detection of the logic state of the signal connected to the RS-422 (+) input.
- For TTL signal (Rev B only), connect directly to RS-422 (+) input. See the following section for connection methods.

Note 3.1: Interfacing to an RS-422 Driver Output

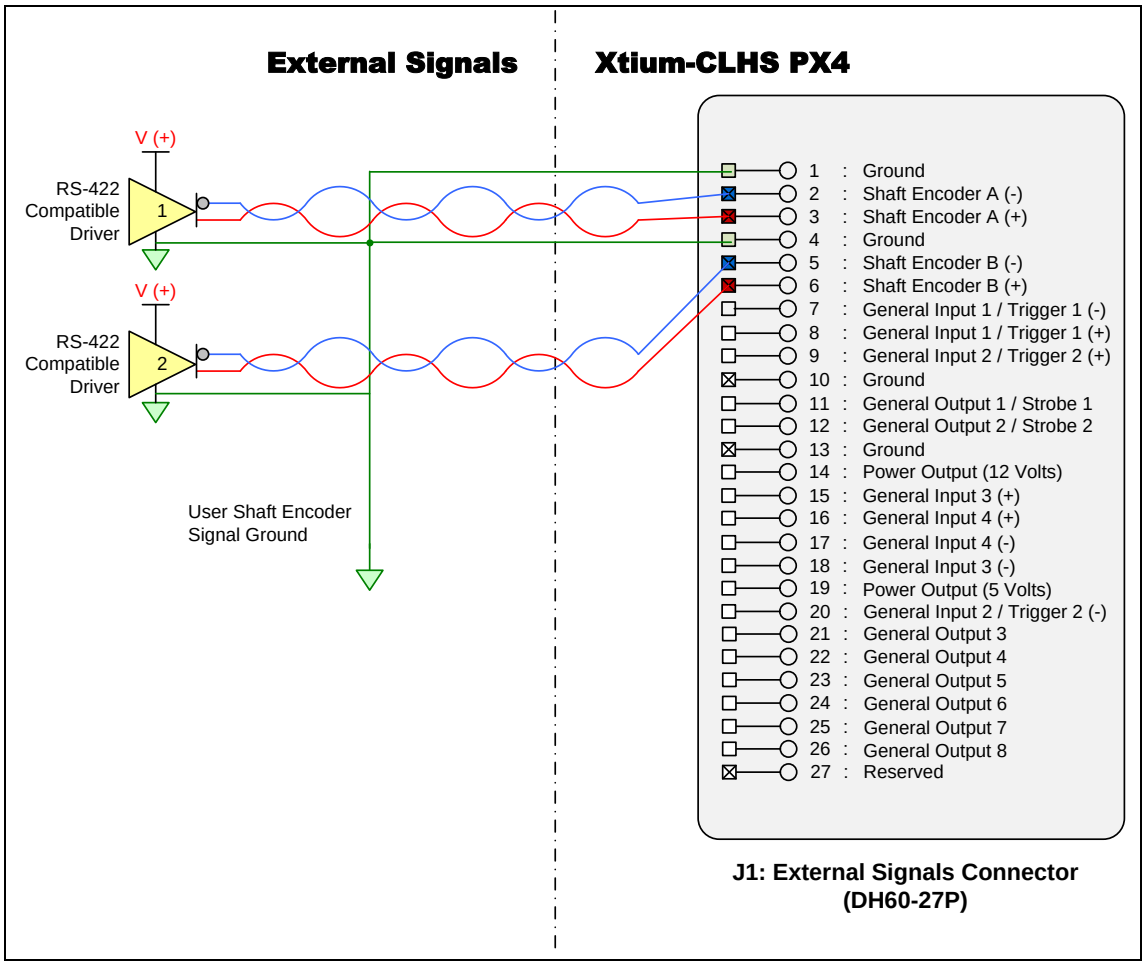


Figure 34:External RS-422 Signals Connection Diagram

Note 3.2: Interfacing to a TTL (also called Push-Pull) Output

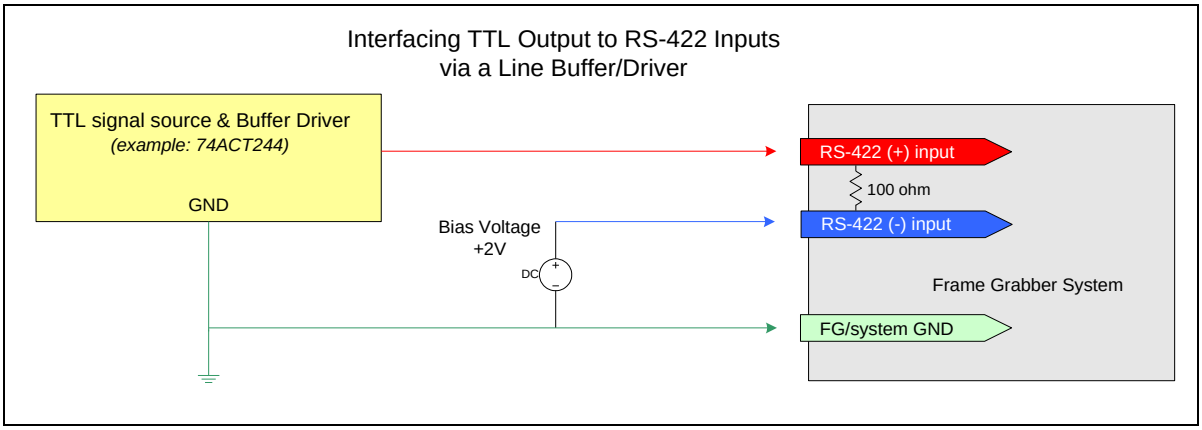


Figure 35: Interfacing TTL to RS-422 Shaft Encoder Inputs

- If necessary, a TTL input can be connected to the RS-422 input using a bias voltage; however, for board revision B, it is recommended to use the Shaft Encoder TTL mode described in Note 3.5).
- RS-422 (-) input is biased to a DC voltage of +2 volts.
- This guarantees that the TTL signal connected to the RS-422 (+) input will be detected as a logic high or low relative to the (-) input.

- The TTL shaft encoder ground, the bias voltage ground, and the Xtium-CLHS PX4 computer system ground must be connected together.
- DC voltage for the RS-422 (-) input can be generated by a resister voltage divider.
- Use a single battery cell if this is more suitable to your system.

Note: User must select the Shaft Encoder RS-422 level when using this mode.

Note 3.3: Interfacing to a Line Driver (also called Open Emitter) Output

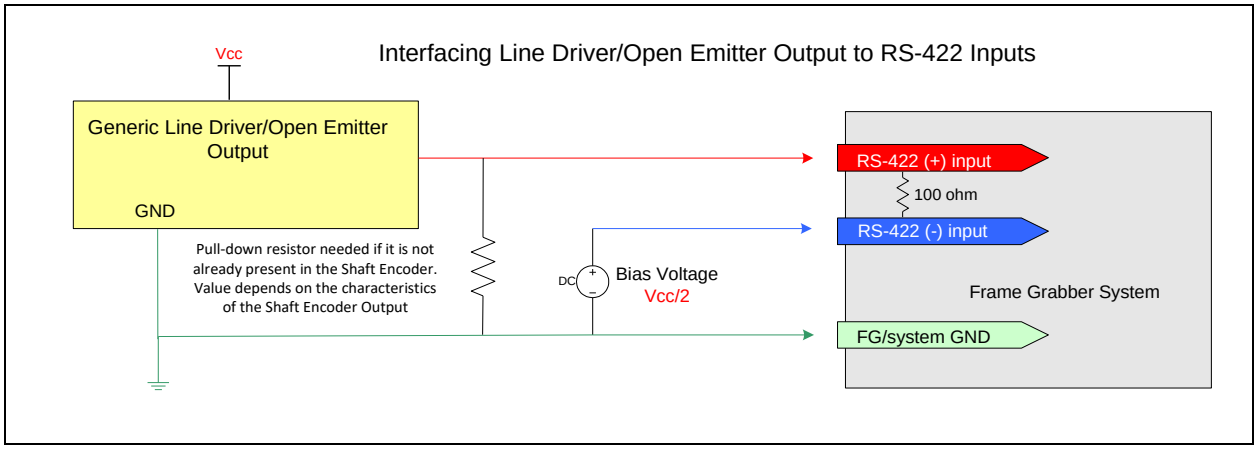


Figure 36: Interfacing to a Line Driver Output

Note: User must select the Shaft Encoder RS-422 level when using this mode.

Note 3.4: Interfacing to an Open Collector Output

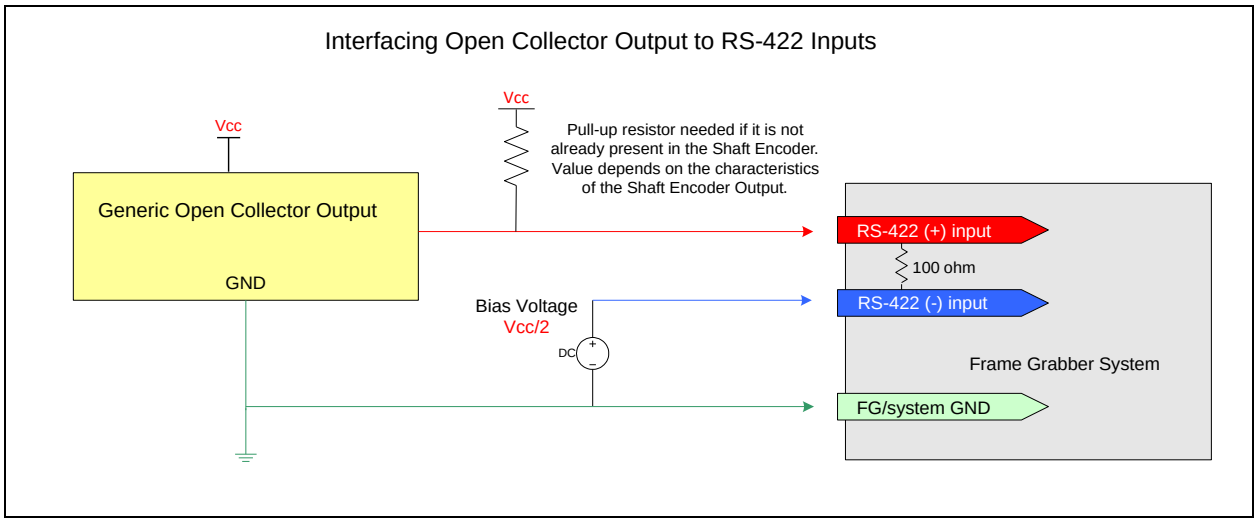


Figure 37: Interfacing to an Open Collector Output

Note: User must select the Shaft Encoder RS-422 level when using this mode.

Note 3.5: Interfacing directly to a TTL (also called Push-Pull) Output (Rev B Only)

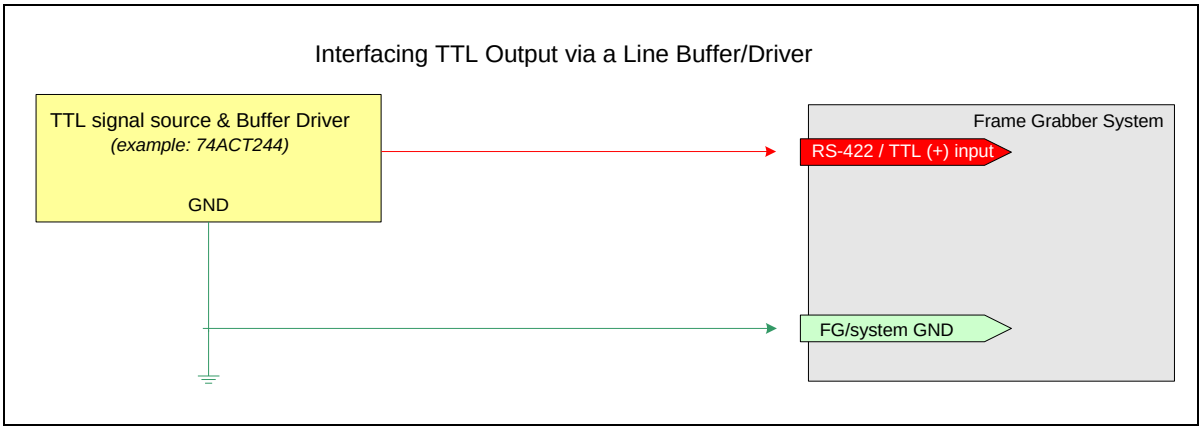


Figure 38: Interfacing TTL to TTL Shaft Encoder Inputs

	**Note**: User must select the Shaft Encoder TTL level when using this mode (CORACQ_PRM_SHAFT_ENCODER_LEVEL = CORACQ_VAL_LEVEL_TTL (0x1)).

J5: Multi-Board Sync / Bi-Directional General I/Os

There are 8 bi-directional General I/Os that can be interconnected between multiple boards. These bi-directional I/Os can be read/written by Sapera application. Bi-directional General I/Os no.1 and no.2 also can also act as the multi-board sync I/Os.

The multi-board sync feature permits interconnecting multiple Xtium boards to synchronize acquisitions to one or two triggers or events. The trigger source origin can be either an external signal or a software control signal. The board sending the trigger(s) is the "Sync Master" board, while the one or more boards receiving the control signal(s) are "Sync Slaves".

Setup of the boards is done either by setting parameters via a Sapera application or by using CamExpert to configure two camera files (.ccf). For testing purposes, two instances of CamExpert (one for each board) can be run on the system where the frame grabbers are installed.

Hardware Preparation

- Interconnect two, three, or four Xtium boards via their J5 connector using the OR-YXCC-BSYNC20 cable (for 2 boards) or the OR-YXCC-BSYNC40 cable (see Board Sync Cable Assembly OR-YXCC-BSYNC40 for 3 or 4 boards).

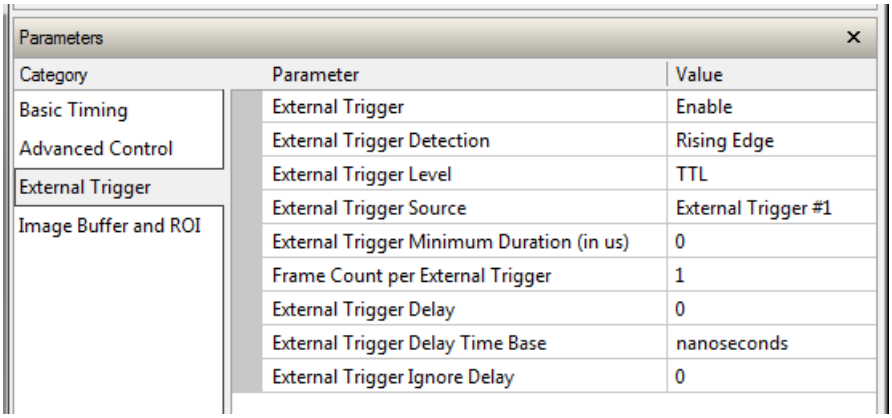
Warning: Multi-Board Sync / Bi-directional General I/Os are only for use with Teledyne DALSA frame grabbers within the same PC, otherwise electrical damage to boards can occur.

Configuration via Sapera Application Programming

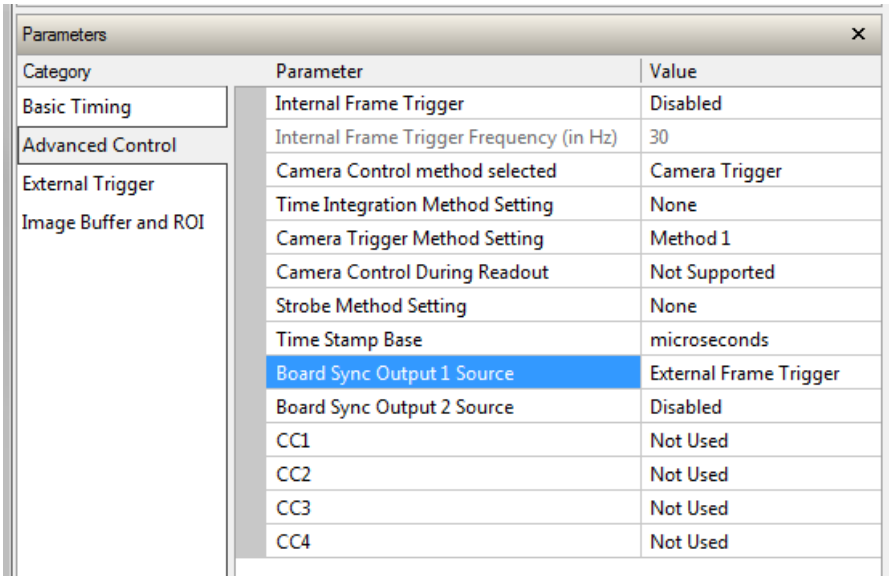
- **Sync Master Board** Software Setup: Choose one Xtium as "Sync Master".
  The Sapera parameter CORACQ_PRM_BOARD_SYNC_OUTPUT1_SOURCE and/or CORACQ_PRM_BOARD_SYNC_OUTPUT2_SOURCE select the signal(s) to send to the "Sync Slave" boards.
- Other sync master board parameters are set as for any external trigger application, such as External Trigger enable, detection, and level. See Sapera documentation for more details.
- **Sync Slave Board** Software Setup: The Sapera parameter CORACQ_PRM_EXT_TRIGGER_SOURCE and/or CORACQ_PRM_EXT_LINE_TRIGGER_SOURCE are set to Board Sync #1 or #2.

Configuration via Sapera CamExpert

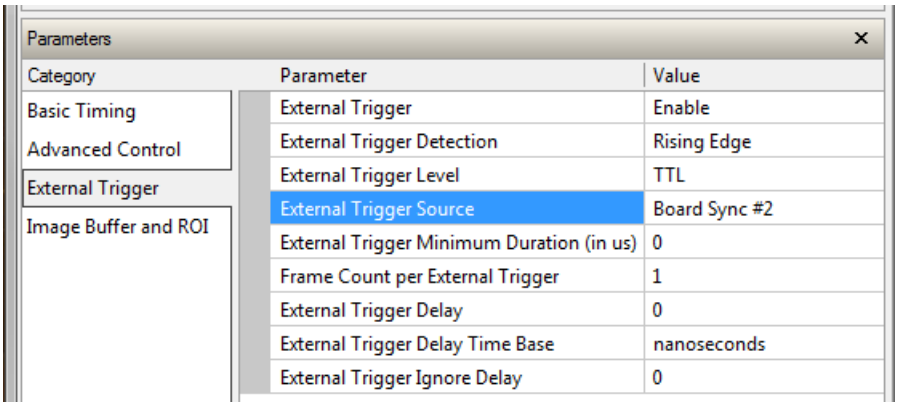
- Start the first instance of CamExpert and select one installed **Xtium board** to be the **master**. As shown in the following image, this board is configured to use an external trigger on input #1.



- The M**aster Xtium board** is also configured to output the external trigger on board sync #1, as shown in the following image.



- The **Slave Xtium board** is configured to receive its trigger on the board sync signal. As an example the following image shows the Xtium board configured for an external sync on board sync #2.



- **Test Setup:** Start the acquisition on all slave boards. The acquisition process is now waiting for the control signal from the master board. Trigger master board acquisition and the acquisition start signal is sent to each slave board.

J7: Power Connector

DC Power Details

Warning: Never remove or install any hardware component with the computer power on. Never connect a power cable to J7 when the computer is powered on.

- Connect a computer 6-pin PCI Express power connector to J7 to supply DC power to connector J1. Older computers may need a power cable adapter (see Power Cable Assembly OR-YXCC-PWRY00).
- The 12 Volt can supply up to 6W to J1 or J4. Note that J1 and J4 have a 500 mA re-settable fuse on the board. If the fuse trips open, turn off the host computer power. When the computer is powered again, the fuse is automatically reset.

Differences between Rev A and Rev B

Board Revision	A	B
User Interface Outputs	4	8
Power on J1/J4	12V	5V and 12V
User Interface Inputs	1 differential (LVDS/RS-422) / Single Ended + 3 Single Ended	4 differential (LVDS/RS-422) / Single Ended
Shaft Encoder Input	RS-422	RS-422 or TTL

Cables & Accessories

The following cables and accessories are available for purchase via third party vendors or Teledyne DALSA. Contact sales for information.

Camera Link HS Cables

In general, a CX4 compliant cable assembly is acceptable for use as a CLHS interface cable with the exception that it must have a thumbscrew type junction shell. This cable assembly is primarily intended as a point-to-point interface of up to 15 meters.

A manufactured CX4 cable shall use the SFF-8470 multi-sourced connector as specified by the published standard "*SFF-8470 Specification for Shielded High Speed Serial Multilane Copper Connector (Rev 3.3 April 3, 2006 or later)*".

For additional information on cables and their specifications, visit the following web sites and search for "Camera Link HS" cables:

Components Express	http://www.componentsexpress.com/
Nortech Systems	http://www.intercon-1.com/intercon1/

DH40-27S Cable to Blunt End (OR-YXCC-27BE2M1, Rev B1)

Cable assembly consists of a 2000 mm (~6 ft.) blunt end cable to mate to Xtium external connector **J1**. Note: The applicable wiring color code table is included with the printed Product Notice shipped with the cable package — no other wiring table should be used.

Important: Cable part number OR-YXCC-27BE2M0 rev.3 is obsolete and should not be used with any Xtium series boards.

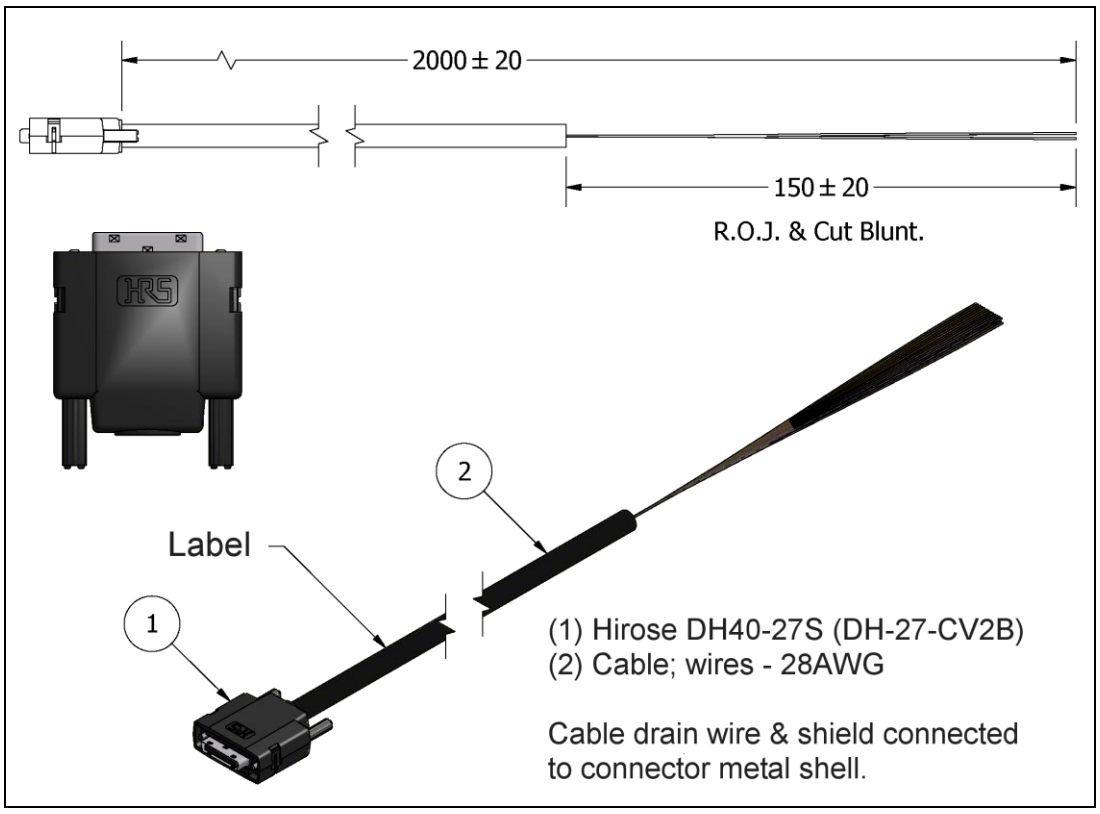
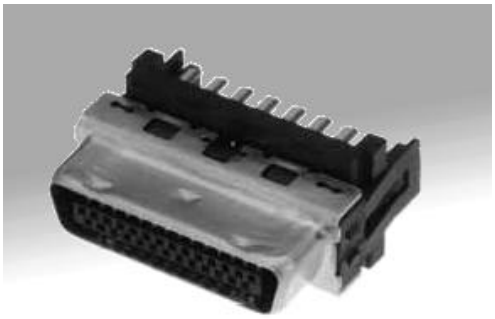


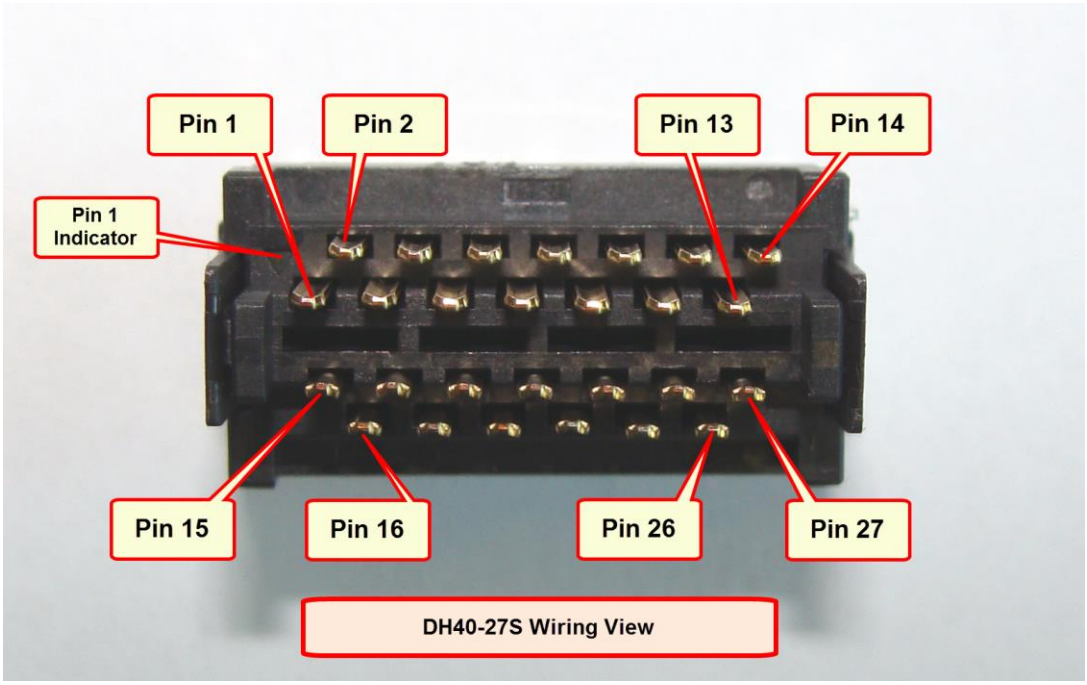
Figure 39: DH60-27P Cable No. OR-YXCC-27BE2M1 Detail

Figure 40: Photo of cable OR-YXCC-27BE2M1

DH40-27S Connector Kit for Custom Wiring

Teledyne DALSA makes available a kit comprised of the DH40-27S connector plus a screw lock housing package, for clients interested in assembling their own custom I/O cable. Order part number "OR-YXCC-H270000", (package as shown below).





Cable assemblies for I/O connector J4

Flat ribbon cables for connecting to J4 can be purchased from Teledyne DALSA or from third part suppliers, as described below.

Teledyne DALSA I/O Cable (part #OR-YXCC-TIOF120)

Contact Teledyne DALSA Sales to order the 12 inch (~30cm) I/O cable with connectors on both ends, as shown in the following picture.

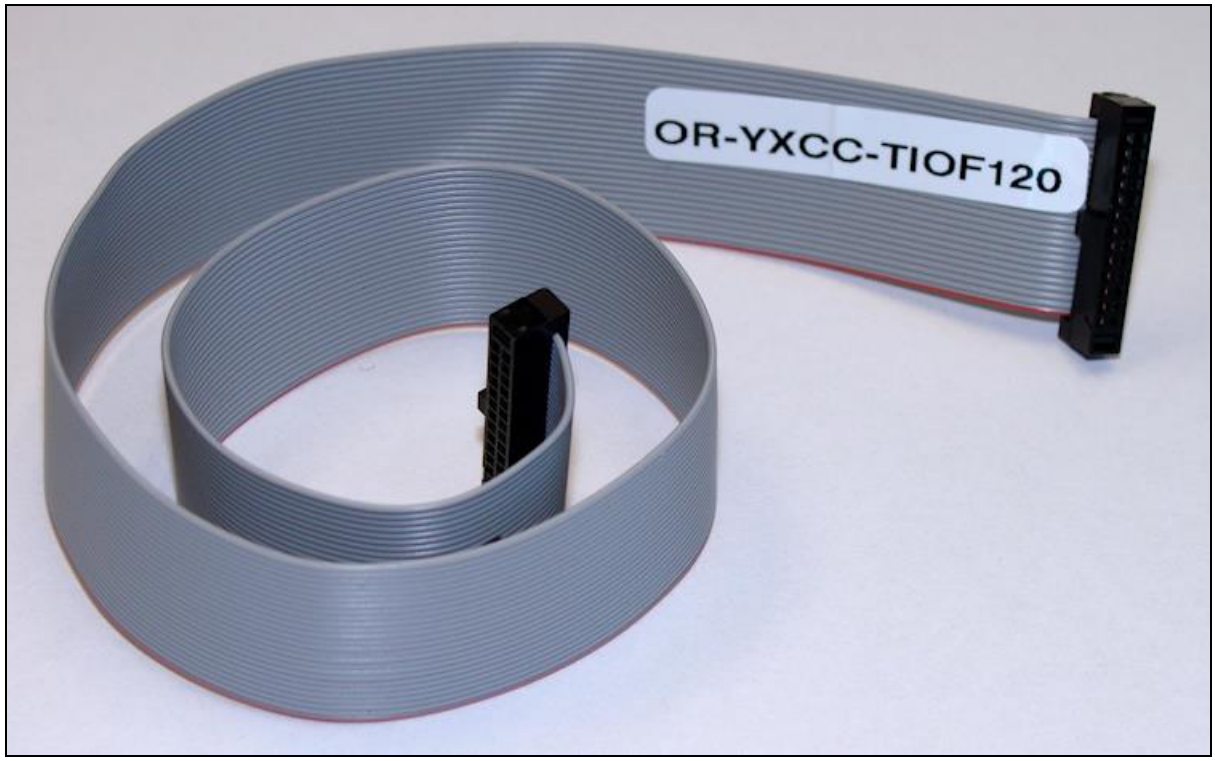


Figure 41: I/O Cable #OR-YXCC-TIOF120

Third Party I/O Cables for J4

Suggested third party cables are available from SAMTEC. Below are two examples:

- Connector to connector (FFSD-13-D-xx.xx-01-N)
- Connector to blunt end (FFSD-13-S-xx.xx-01-N)
- Note: xx.xx denotes length, where 06.00 is a 6 inch (~15 cm) length cable
- URL: http://cloud.samtec.com/catalog_english/FFSD.PDF

Board Sync Cable Assembly OR-YXCC-BSYNC40

This cable connects 3 to 4 Xtium boards for the board sync function as described in section J5: Multi-Board Sync / Bi-Directional General I/Os. For a shorter 2 board cable, order cable assembly OR-YXCC-BSYNC20.

For a third party source of cables, see http://cloud.samtec.com/catalog_english/FFSD.PDF.

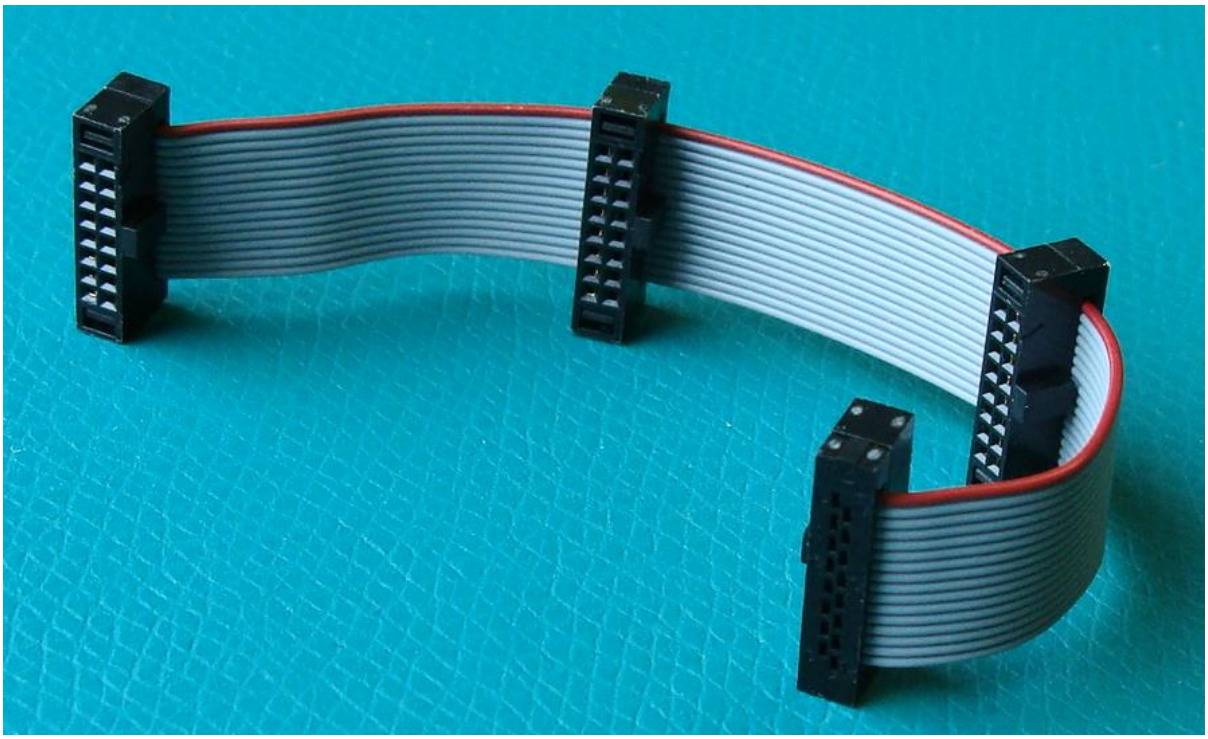


Figure 42: Photo of cable OR-YXCC-BSYNC40

Power Cable Assembly OR-YXCC-PWRY00

When the Xtium-CLHS PX4 supplies power to external devices via the J1 I/O connector, PC power must be connected to the Xtium external power source connector (J7).

Recent computer power supplies provide multiple 6-pin power source connectors for PCI Express video cards, where one is connected to J7 on the Xtium-CLHS. But if the computer is an older model, this power supply adapter converts 2 standard 4-pin large power connectors to a 6-pin power connector.

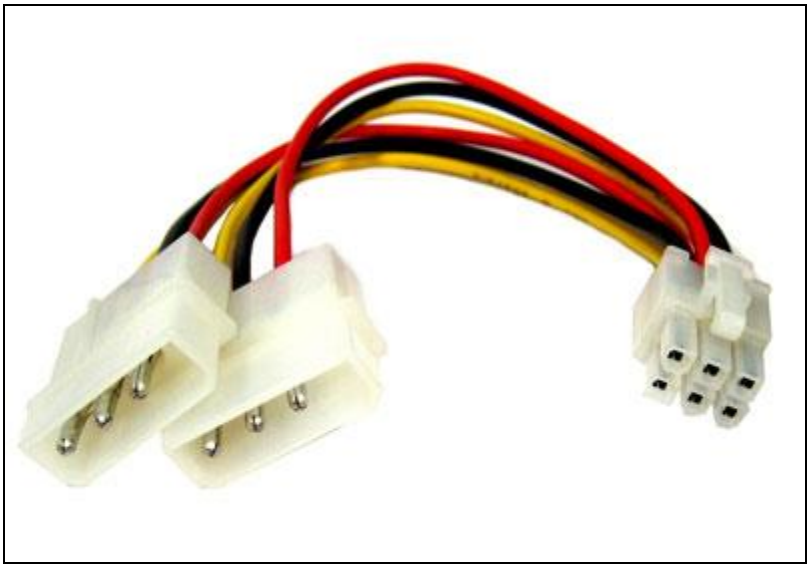


Figure 43: Photo of cable assembly OR-YXCC-PWRY00

This is an industry standard adapter cable which can be purchased from Teledyne DALSA.

Camera Link HS Interface

Camera Link HS Overview

Note: The following text is extracted from the AIA document "*Specifications of the Camera Link HS Interface Standard for Digital Cameras and Frame Grabbers" version 1.0 RC5*, ©2012 AIA. Refer to their site www.visiononline.org for additional information.

Camera Link HS (CLHS) is a global standard defining the communications between a camera and a frame grabber. The CLHS standard offers high performance control functions and scalable data transfer bandwidths between the camera and frame grabber. The data transmission technology employed in CLHS is available from multiple suppliers and has roadmaps to higher bit rates driven by the telecom market. The use of widely used technology guarantees a low component cost and long term supply for machine vision customers.

The packet based protocol used in CLHS is machine vision specific, thus delivering the high image reliability needed in modern machine vision systems. CLHS Messages are defined independent of the physical layer, allowing CLHS to adopt new physical layers as they become available.

Currently CLHS employs simple 8b/10b technology in the M-Protocol and the XAUI-64/66 encoding for the X-Protocol. CLHS supports real time triggers (Pulse) and General Purpose Input/Output (GPIO), using a priority methodology that results in CLHS having the lowest latency and jitter of any packet based protocol. Designed with forward error correction for real time messages, plus CRC and hardware based resend mechanisms for video and command packets, ensure data reliability.

Rights and Trademarks

The AIA, as sponsor of the Camera Link HS committee, owns the U.S. trademark registration for the Camera Link HS logo as a certification mark for the mutual benefit of the industry. Usage of the Camera Link HS logo with any product(s) implies compliancy with the Camera Link HS standard.

Appendix A: Silent Installation

Both Sapera LT and the Xtium-CLHS PX4 driver installations share the same installer technology. When the installations of Teledyne DALSA products are embedded within a third party's product installation, the installation mode can either have user interaction or be completely silent. The following installation mode descriptions apply to both Sapera and the hardware driver.

Note: You must reboot after the installation of Sapera LT. However, to streamline the installation process, Sapera LT can be installed without rebooting before installing the board hardware device drivers. The installations then complete with a single final system reboot.

Perform Teledyne DALSA embedded installations in either of these two ways:

- **Normal Mode**
  The default mode is interactive. This is identical to running the setup.exe program manually from Windows (either run from Windows Explorer or the Windows command line).
- **Silent Mode**
  This mode requires no user interaction. A preconfigured "response" file provides the user input. The installer displays nothing.

Silent Mode Installation

A Silent Mode installation is recommended when integrating Teledyne DALSA products into your software installation. The silent installation mode allows the device driver installation to proceed without the need for mouse clicks or other input from a user.

Preparing a Silent Mode Installation requires two steps:

- Prepare the response file, which emulates a user.
- Invoke the device driver installer with command options to use the prepared response file.

Creating a Response File

Create the installer response file by performing a device driver installation with a command line switch "-r". The response file is automatically named **`setup.iss`** and is saved in the \windows folder. If a specific directory is desired, the switch –f1 is used.

As an example, to save a response file in the same directory as the installation executable of the Xtium-CLHS PX4, the command line would be:

```
Xtium-CLHS_PX4_1.00.00.0000 –r –f1".\setup.iss"
```

Running a Silent Mode Installation

A device driver silent installation, whether done alone or within a larger software installation requires the device driver executable and the generated response file **`setup.iss`**.

Execute the device driver installer with the following command line:

```
Xtium-CLHS_PX4_1.00.00.0000 -s -f1".\setup.iss"
```

Where the **–s** switch specifies the silent mode and the **–f1** switch specifies the location of the response file. In this example, the switch –f1".\setup.iss" specifies that the **`setup.iss`** file be in the same folder as the device driver installer.

Note: On Windows 7 and 8, the Windows Security dialog box will appear unless one has already notified Windows to 'Always trust software from "Teledyne DALSA Inc." during a previous installation of a driver.

Silent Mode Uninstall

Similar to a silent installation, a response file must be prepared first as follows.

Creating a Response File

The installer response file is created by performing a device driver un-installation with a command line switch "-r". The response file is automatically named **`setup_uninstall.iss`** which is saved in the \windows folder. If a specific directory is desired, the switch "–f1" is used.

As an example, to save a response file in the same directory as the installation executable of the Xtium-CLHS PX4, the command line would be:

```
Xtium-CLHS_PX4_1.00.00.0000 –r –f1".\setup_uninstall.iss"
```

Running a Silent Mode Uninstall

Similar to the device driver silent mode installation, the un-installation requires the device driver executable and the generated response file **`setup.iss`**.

Execute the device driver installer with the following command line:

```
Xtium-CLHS_PX4_1.00.00.0000 -s -f1".\setup_uninstall.iss"
```

Where the **–s** switch specifies the silent mode and the **–f1** switch specifies the location of the response file. In this example, the switch –f1".\setup_uninstall.iss" specifies that the **`setup_uninstall.iss`** file be in the same folder as the device driver installer.

Silent Mode Installation Return Code

A silent mode installation creates a file "corinstall.ini" in the Windows directory. A section called [SetupResult] contains the 'status' of the installation. A value of **1** indicates that the installation has started and a value of **2** indicates that the installation has terminated.

A silent mode installation also creates a log file "setup.log" which by default is created in the same directory and with the same name (except for the extension) as the response file. The /f2 option enables you to specify an alternative log file location and file name, as in Setup.exe /s /f2"C:\Setup.log".

The "setup.log" file contains three sections. The first section, [InstallShield Silent], identifies the version of InstallShield used in the silent installation. It also identifies the file as a log file. The second section, [Application], identifies the installed application name, version, and the company name. The third section, [ResponseResult], contains the 'ResultCode' indicating whether the silent installation succeeded. A value of **0** means the installation was successful.

Installation Setup with CorAppLauncher.exe

The installation setup can be run with the CorAppLauncher.exe tool provided with the driver.

- Install the board driver and get CorAppLauncher.exe from the \bin directory of the installation.
- When running the installation, CorAppLauncher.exe will return only when the installation is finished.
- When run from within a batch file, obtain the installation exit code from the ERRORLEVEL value.
- The arguments to CorAppLauncher.exe are
  -l: Launch application
  -f: Application to launch. Specify a fully qualified path.

As an example:

- CorAppLauncher –l –f"c:\driver_install\Xtium-CLHS_PX4_1.00.00.0000.exe"
- IF %ERRORLEVEL% NEQ 0 goto launch error

Note: There is a 32-bit and 64-bit version of CorAppLauncher.exe. When installing the driver, only the version related to the OS is installed. However, the 32-bit version is usable on either 32-bit or 64-bit Windows.

Custom Driver Installation Using install.ini

Customize the driver installation by parameters defined in the file "install.ini".
By using this file, the user can:

- Select the user default configuration.
- Select different configurations for systems with multiple boards.
- Assign a standard Serial COM port to board.

Creating the install.ini File

- Install the driver in the target computer. All Xtium-CLHS PX4 boards required in the system must be installed.
- Configure each board's acquisition firmware using the Teledyne DALSA Device Manager tool (see Device Manager – Board Viewer).
- When each board setup is complete, using the Teledyne DALSA Device Manager tool, click on the **Save Config File** button. This will create the "install.ini" file.

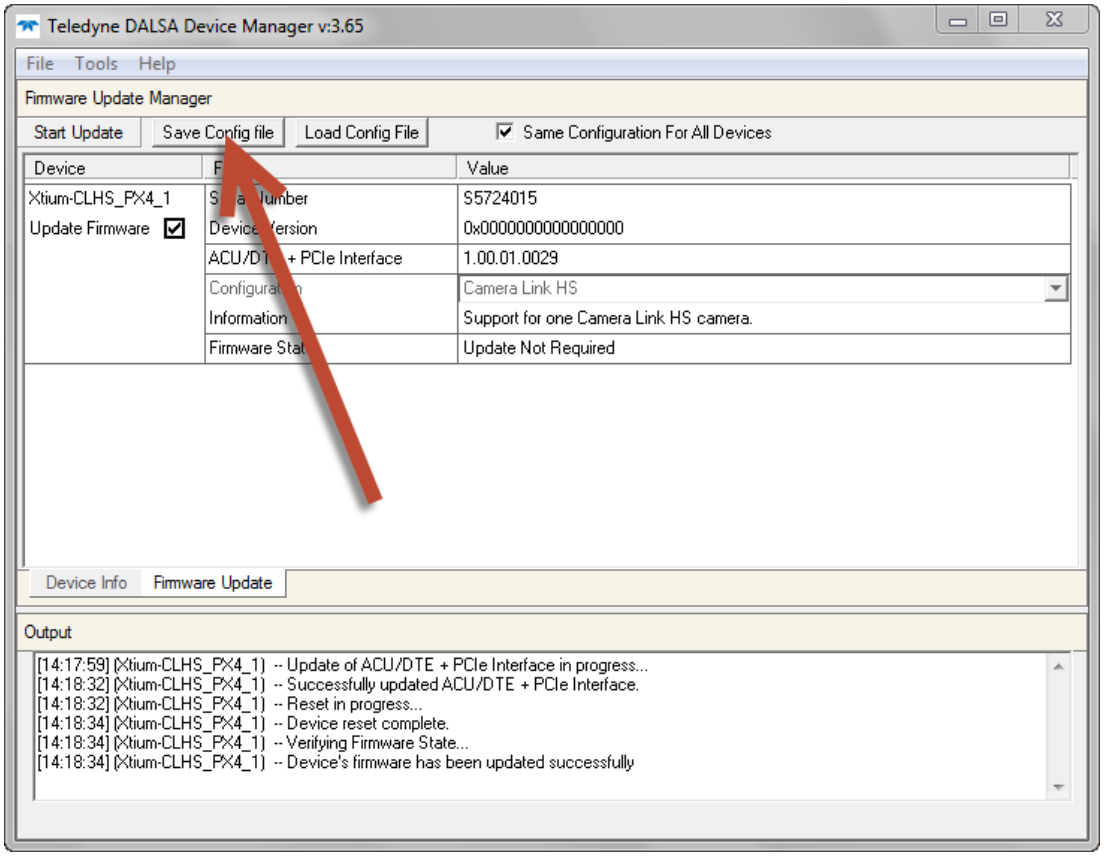


Figure 44: Create an install.ini File

Run the Installation using install.ini

Copy the install.ini file into the same directory as the setup installation file. Run the setup installation as normal. The installation will automatically check for an install.ini file and if found, use the configuration defined in it.

In the Teledyne DALSA Device Manager start-up dialog the use of an *install.ini* is indicated in the INI Configuration column.

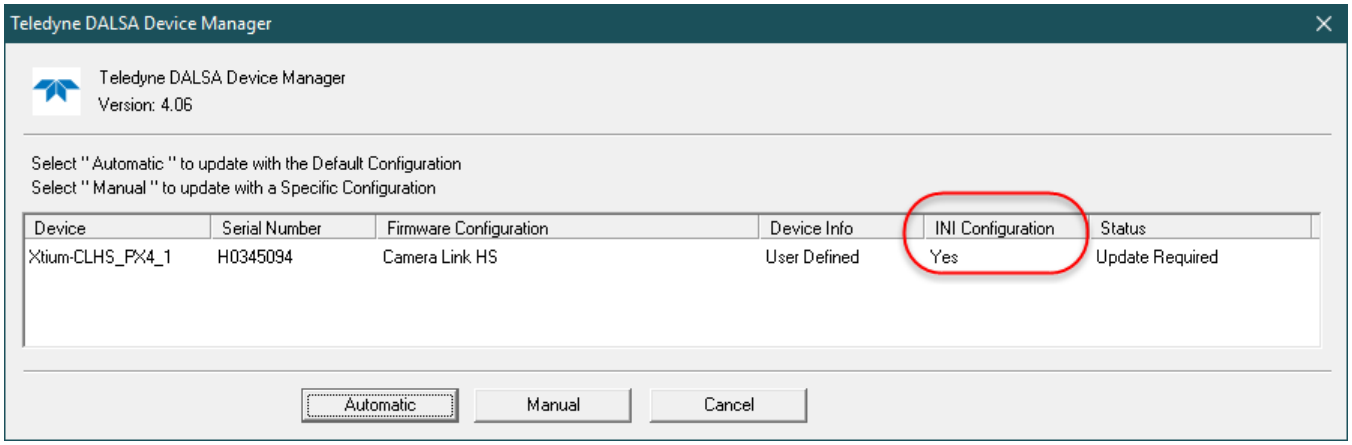


Figure 45: INI Configuration

Appendix B: Troubleshooting Problems

Overview

The Xtium-CLHS PX4 (and the Xtium family of products) is tested by Teledyne DALSA in a variety of computers. Although unlikely, installation problems may occur due to the constant changing nature of computer equipment and operating systems. This section describes what the user can verify to determine the problem or the checks to make before contacting Teledyne DALSA Technical Support.

If you require help and need to contact Teledyne DALSA Technical Support, make detailed notes on your installation and/or test results for our technical support to review. See Technical Support for contact information.

Problem Type Summary

Xtium-CLHS PX4 problems are either installation types where the board hardware is not recognized on the PCIe bus (that is, trained), or function errors due to camera connections or bandwidth issues. The following links jump to various topics in this troubleshooting section.

First Step: Check the Status LED

Status LED D1 should be **BLUE** or flashing **BLUE** just after power up. If it remains flashing **RED**, the board firmware did not load correctly. Once the Windows driver is started, LED D1 should be **GREEN** or flashing **GREEN**. If LED D1 remains **BLUE** or flashing **BLUE**, the board is still running from the safe mode load. This could indicate that the normal load in the flash is corrupted or not present.

CLHS Link status is indicated by LED D3 – above the camera connector. The status colors displayed follow industry specifications for Camera Link HS.

The complete Status LED descriptions are available in the technical reference section.

Possible Installation Problems

Hardware PCI bus conflict: When a new installation produces PCI bus error messages or the board driver does not install, it is important to verify that there are no conflicts with other PCI or system devices already installed. Use the Teledyne DALSA PCI Diagnostic tool as described in the following section "Diagnostic Tool Overview".

- **Check for PCI Bus Conflicts**. Verify the installation via the Windows Device Manager.
- **BSOD (blue screen) following a board reset:** After programming the board with different firmware, the computer displays the BSOD when the board is reset (see BSOD (blue screen) Following a Board Reset).
- **Verify Sapera and Board drivers:** If there are errors when running applications, confirm that all Sapera and board drivers are running. See Sapera and Hardware Windows Drivers for details. In addition, Teledyne DALSA technical support will ask for the log file of messages by Teledyne DALSA drivers. Follow the instructions describe in Teledyne DALSA Log Viewer.
- **Firmware update error:** There was an error during the Xtium-CLHS PX4 firmware update procedure. The user can usually easily correct this. Follow the instructions Recovering from a Firmware Update Error.

- **Board stops working**. Installation went well but the board doesn't work or stopped working. Review these steps described in Symptoms: CamExpert Detects no Boards.
- **Using Windows 8/10 Fast Boot option:** When adding, removing, or moving boards while the PC is shutdown with the Windows Fast Boot option activated, it is possible that the boards don’t get mapped properly on the next reboot of the computer. The driver will detect such a situation and the Device Manager launched at startup will display a message indicating that a reboot is required.

Possible Functional Problems

- **Driver Information:** Use the Teledyne DALSA device manager program to view information about the installed Xtium-CLHS PX4 board and driver. See Driver Information via the Device Manager Program.
- **On-Board Image Memory Requirements:** The Xtium-CLHS PX4 on-board memory can provide two frame buffers large enough for most imaging situations. See On-board Image Memory Requirements for Acquisitions for details on the on board memory and possible limitations.

Sometimes the problem symptoms are not the result of an installation issue but due to other system issues. Review the sections described below for solutions to various Xtium-CLHS PX4 functional problems.

- Symptoms: Xtium-CLHS PX4 Does Not Grab
- Symptoms: Card grabs black
- Symptoms: Card acquisition bandwidth is less than expected

Troubleshooting Procedures

The following sections provide information and solutions to possible Xtium-CLHS PX4 installation and functional problems. The previous section of this manual summarizes these topics.

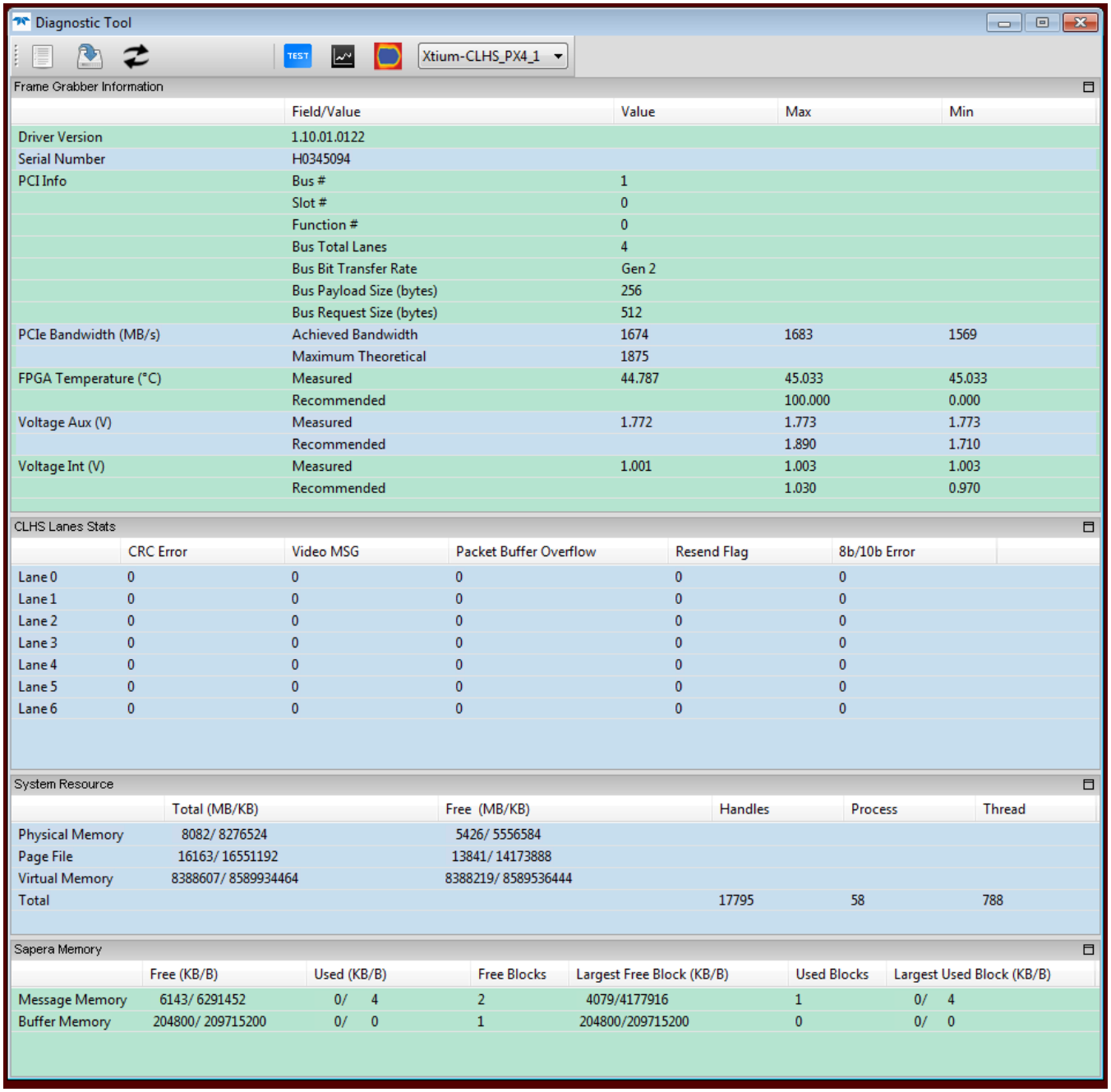
Diagnostic Tool Overview

The Xtium-CLHS PX4 Board Diagnostic Tool provides a quick method to see board status and health. It additionally provides live monitoring of FPGA temperature and voltages, which may help in identifying problems.

Diagnostic Tool Main Window

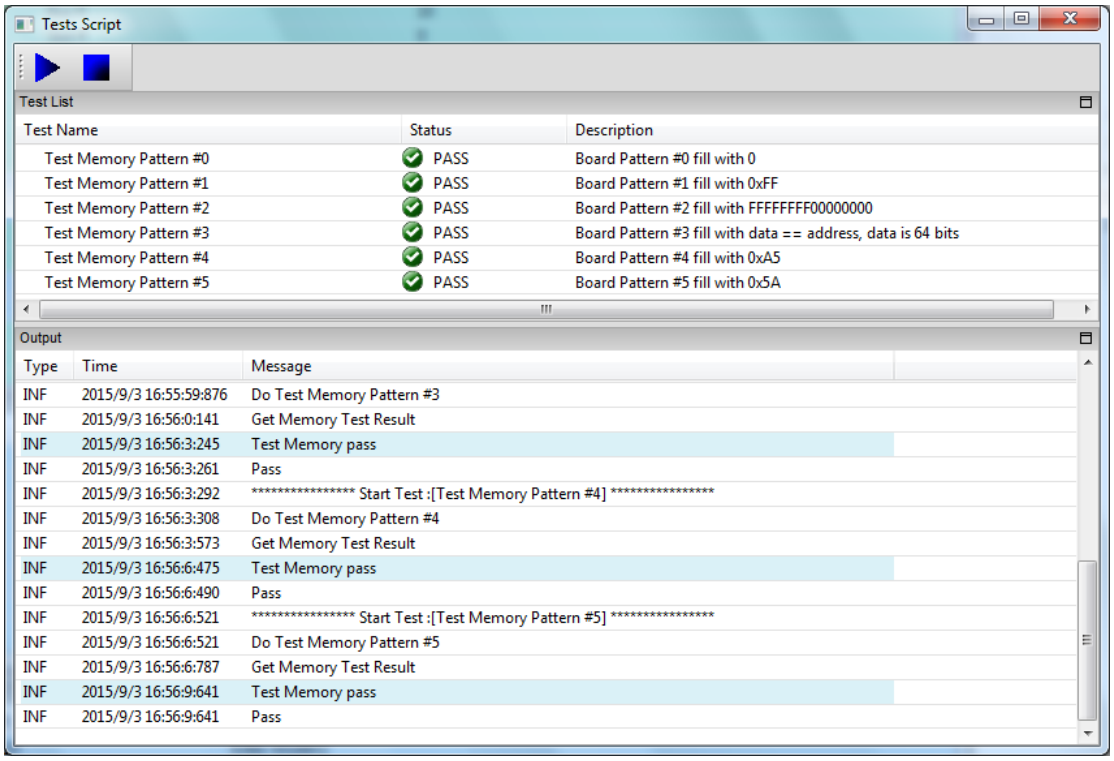
The main window provides a comprehensive view of the installed Xtium board. Toolbar buttons execute the board self-test function and open a FPGA live status window.

Important parameters include the PCI Express bus transfer supported by the host computer and the internal Xtium FPGA temperature. The bus transfer defines the maximum data rate possible in the computer, while an excessive FPGA temperature may explain erratic acquisitions due to poor computer ventilation.


Diagnostic Tool
Xtium-CLHS_PX4_1
Frame Grabber Information
Field/Value
Value
Max
Min
Driver Version
1.10.01.0122
Serial Number
H0345094
PCI Info
Bus #
1
Slot #
0
Function #
0
Bus Total Lanes
4
Bus Bit Transfer Rate
Gen 2
Bus Payload Size (bytes)
256
Bus Request Size (bytes)
512
PCIe Bandwidth (MB/s)
Achieved Bandwidth
1674
1683
1569
Maximum Theoretical
1875
FPGA Temperature (°C)
Measured
44.787
45.033
45.033
Recommended
100.000
0.000
Voltage Aux (V)
Measured
1.772
1.773
1.773
Recommended
1.890
1.710
Voltage Int (V)
Measured
1.001
1.003
1.003
Recommended
1.030
0.970
CLHS Lanes Stats
CRC Error
Video MSG
Packet Buffer Overflow
Resend Flag
8b/10b Error
Lane 0
0
0
0
0
0
Lane 1
0
0
0
0
0
Lane 2
0
0
0
0
0
Lane 3
0
0
0
0
0
Lane 4
0
0
0
0
0
Lane 5
0
0
0
0
0
Lane 6
0
0
0
0
0
System Resource
Total (MB/KB)
Free (MB/KB)
Handles
Process
Thread
Physical Memory
8082/ 8276524
5426/ 5556584
Page File
16163/ 16551192
13841/ 14173888
Virtual Memory
8388607/ 8589934464
8388219/ 8589536444
Total
17795
58
788
Sapera Memory
Free (KB/B)
Used (KB/B)
Free Blocks
Largest Free Block (KB/B)
Used Blocks
Largest Used Block (KB/B)
Message Memory
6143/ 6291452
0/ 4
2
4079/4177916
1
0/ 4
Buffer Memory
204800/ 209715200
0/ 0
1
204800/209715200
0
0/ 0

Diagnostic Tool Self-Test Window

Click the Start button to initiate the board memory self-test sequence. A healthy board will pass all memory test patterns.

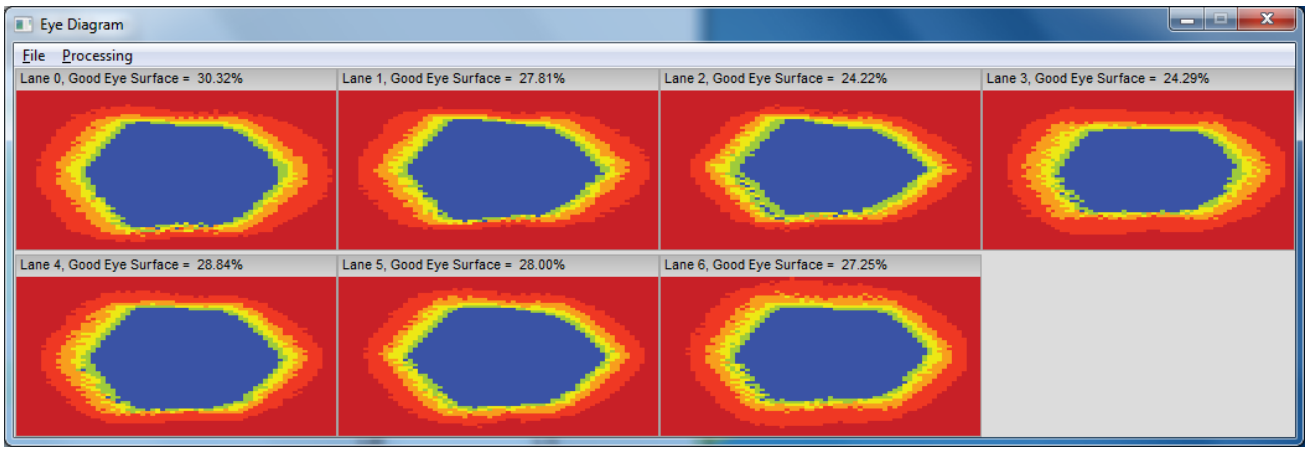


Camera Input Eye Diagram Monitor

Eye Diagrams allow the user to visibly evaluate signal integrity between camera data lanes or between different cable sets. This tool does not provide specific measurements but will help to identify signal noise or jitter issues associated with bad cables or overly long cables.

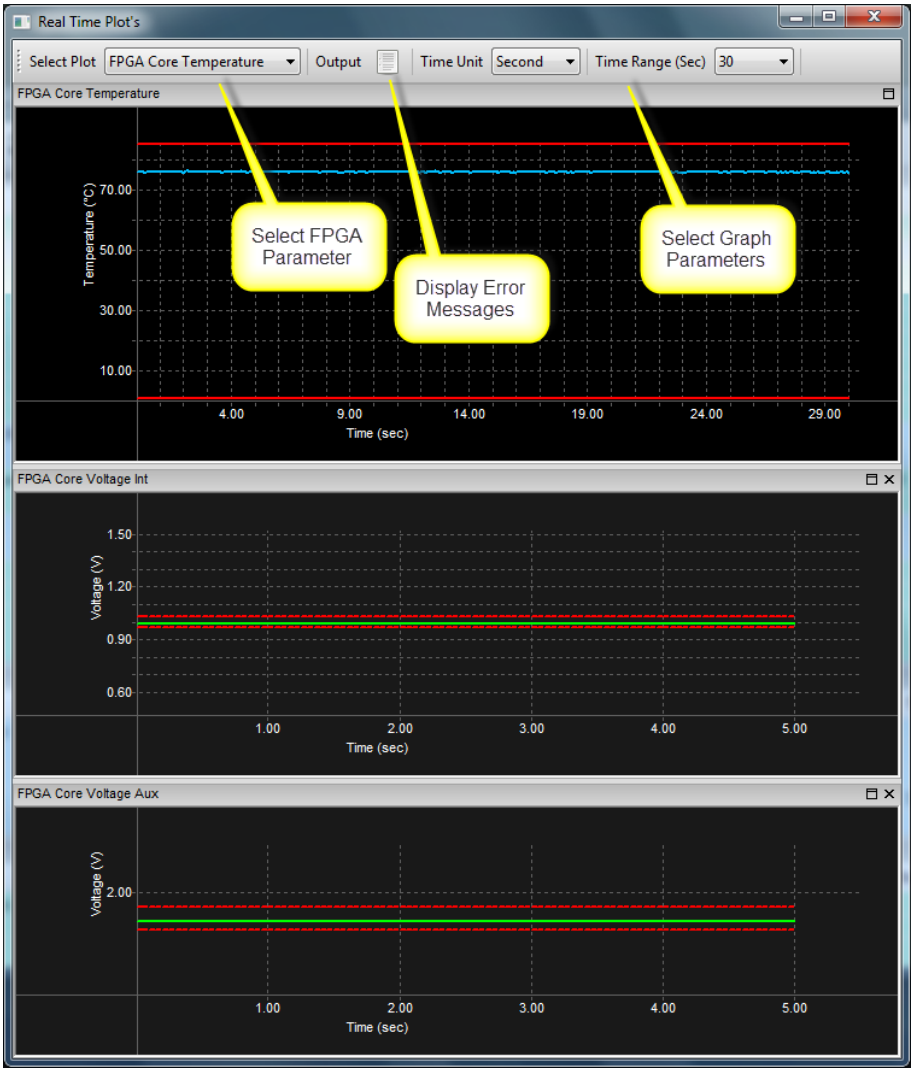
The screen capture below shows a camera with 7 data lanes, where each digital signal is repetitively sampled and overlaid over itself, showing relative low-high transitions of the differential signal. The blue center area (eye surface) seems similar between each lane, typical for a good cable set.

The closure (collapse or horizontal shortening) of the eye surface would indicate problems such as poor signal to noise, high cable capacitance, multipath interference, among many possible digital transmission faults.



Diagnostic Tool Live Monitoring Window

The three FPGA parameters listed on the main window can also be monitored in real time. Choosing a parameter puts that graph at the top where the user can select the time unit and time range. Clicking the Output button will open a window displaying any error messages associated with that parameter.



Checking for PCI Bus Conflicts

One of the first items to check when there is a problem with any PCI board is to examine the system PCI configuration and ensure that there are no conflicts with other PCI or system devices. The *PCI Diagnostic* program (**cpcidiag.exe**) allows examination of the PCI configuration registers and can save this information to a text file. Run the program via the Windows Start Menu shortcut **Start • Programs • Teledyne DALSA • Sapera LT • Tools • PCI Diagnostics**.

As shown in the following screen image, use the first drop menu to select the PCI device to examine. Select the device from Teledyne DALSA. Note the bus and slot number of the installed board (this will be unique for each system unless systems are setup identically). Click on the **Diagnostic** button to view an analysis of the system PCI configuration space.

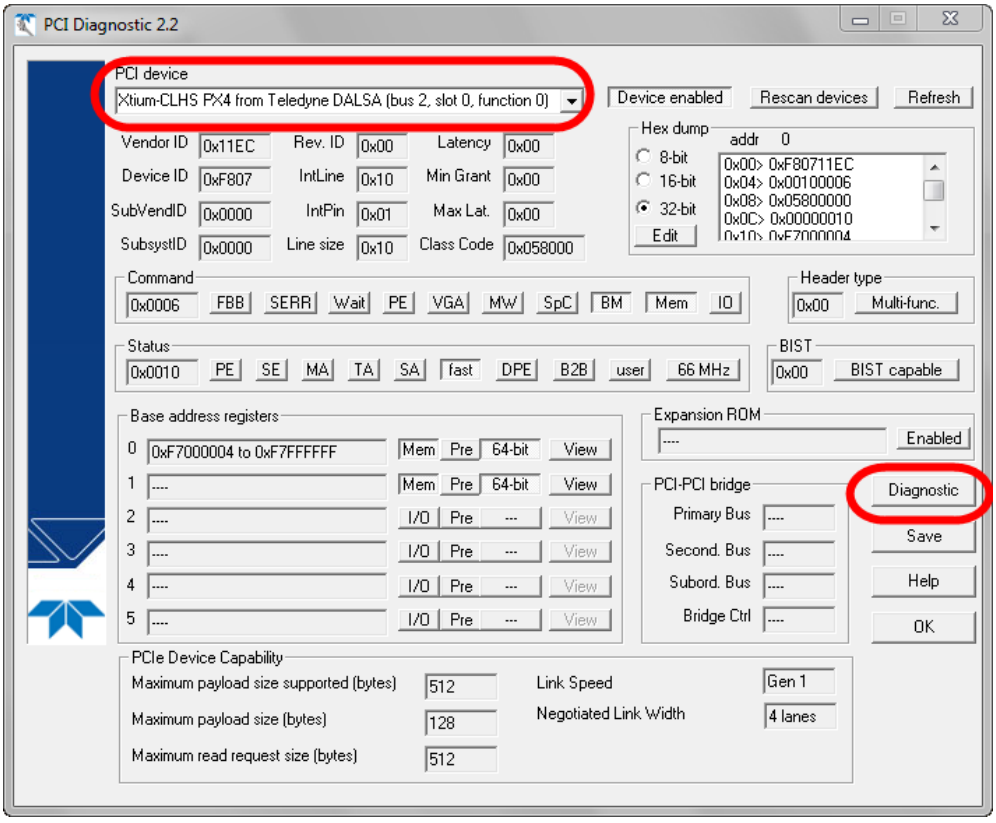


Figure 46: PCI Diagnostic Program

Clicking on the **Diagnostic** button opens a new window with the diagnostic report. From the PCI Bus Number drop menu, select the bus number that the Xtium-CLHS PX4 is installed in—in this example the slot is bus 2.

The window now shows the I/O and memory ranges used by each device on the selected PCI bus. The information display box will detail any PCI conflicts. If there is a problem, click on the **Save** button. A file named '**pcidiag.txt'** is created (in the Sapera\bin directory) with a dump of the PCI configuration registers. Email this file when requested by the Teledyne DALSA Technical Support group along with a full description of your computer.

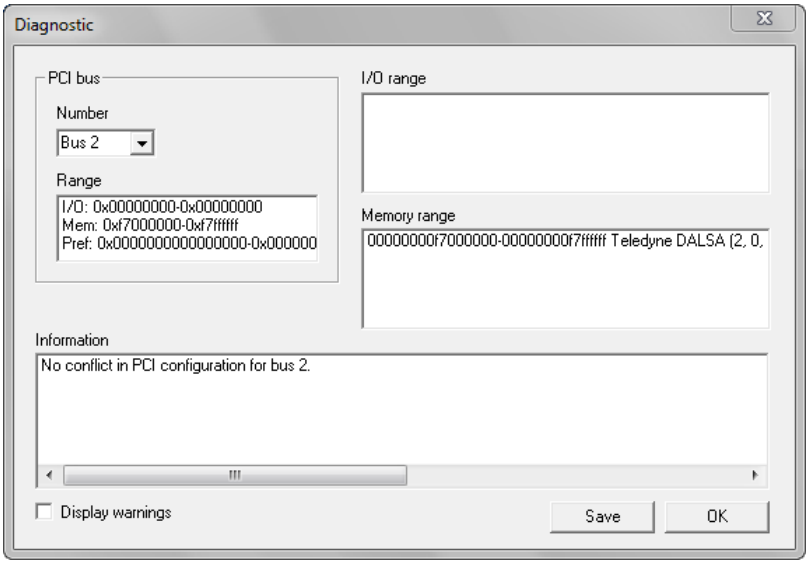


Figure 47: PCI Diagnostic Program – PCI bus info

Windows Device Manager

An alternative method to confirm the installation of the Xtium-CLHS PX4 board and driver is to use the Windows Device manager tool. Use the Start Menu shortcut **Start ● Control Panel ● System ● Device Manager**. As shown in the following screen images, look for *Xtium-CLHS PX4* board under "Imaging Devices". Double-click and look at the device status. You should see "This device is working properly." Go to "Resources" tab and make certain that the device has an interrupt assigned to it, without conflicts.

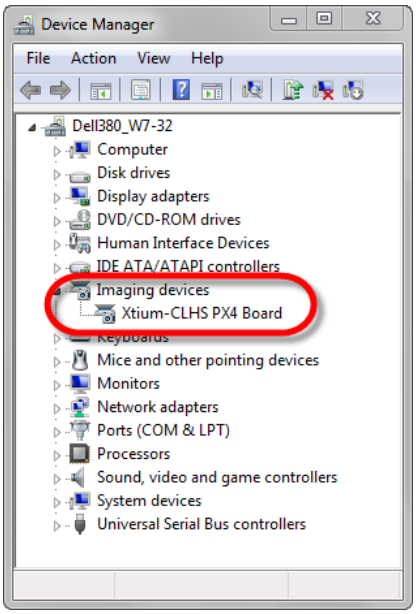


Figure 48: Using Windows Device Manager

BSOD (blue screen) Following a Board Reset

There are cases where a PC will falsely report a hardware malfunction when the Xtium-CLHS PX4 board is reset. Ensure that you are using Sapera LT 7.50 or later.

Sapera and Hardware Windows Drivers

Any problem seen after installation, such as an error message running CamExpert, first make certain the appropriate Teledyne DALSA drivers have started successfully during the boot sequence. Example, click on the **Start ● Programs ● Accessories ● System Tools ● System Information ● Software Environment** and click on **System Drivers**. Make certain the following drivers have started for the **Xtium-CLHS PX4**.

Device	Description	Type	Started
CorXtiumCLHSPX4	Xtium-CLHS PX4 messaging	Kernel Driver	Yes
CorLog	Sapera Log viewer	Kernel Driver	Yes
CorMem	Sapera Memory manager	Kernel Driver	Yes
CorPci	Sapera PCI configuration	Kernel Driver	Yes
CorSerial	Sapera Serial Port manager	Kernel Driver	Yes

Teledyne DALSA Technical Support may request that you check the status of these drivers as part of the troubleshooting process.

Recovering from a Firmware Update Error

This procedure is required if any failure occurred while updating the Xtium-CLHS PX4 firmware on installation or during a manual firmware upgrade. If on the case the board has corrupted firmware, any Sapera application such as CamExpert or the grab demo program will not find an installed board to control.

Possible reasons for firmware loading errors or corruption are:

- Computer system mains power failure or deep brown-out
- PCI bus or checksum errors
- PCI bus timeout conditions due to other devices
- User forcing a partial firmware upload using an invalid firmware source file

When the Xtium-CLHS PX4 firmware is corrupted, the board will automatically run from the Safe load after a PC reset.

***Solution*:** Update the board using the standard method described in section Firmware Update: Automatic Mode.

Driver Information via the Device Manager Program

The Device Manager program provides a convenient method of collecting information about the installed Xtium-CLHS PX4. System information such as operating system, computer CPU, system memory, PCI configuration space, plus Xtium-CLHS PX4 firmware information is displayed or written to a text file (default file name – BoardInfo.txt). Note that this program also manually uploads firmware to the Xtium-CLHS PX4 (described elsewhere in this manual).

Execute the program via the Windows Start Menu shortcut
Start • Programs • Teledyne DALSA • Xtium-CLHS PX4 Device Driver • Device Manager.

If the Device Manager Program does not run, it will exit with a board was not found message. Possible reasons for an error are:

- Board is not in the computer
- Board driver did not start or was terminated
- PCI conflict after some other device was installed

Information Window

Click to highlight one of the board components and its information shows in the right hand window, as described below.

- Select **Information** to display identification and information stored in the Xtium-CLHS PX4 firmware.
- Select **Firmware** to display version information for the firmware components.
- Select one of the firmware components to load *custom* firmware when supplied by Teledyne DALSA engineering for a future feature.
- Click on **File • Save Device Info** to save all information to a text file. Email this file when requested by Technical Support.

Teledyne DALSA Log Viewer

The third step in the verification process is to save in a text file the information collected by the Log Viewer program. Run the program via the Windows Start Menu shortcut
Start • Programs • Teledyne DALSA • Sapera LT • Tools • Log Viewer.

The Log Viewer lists information about the installed Teledyne DALSA drivers. Click on File • Save and you will be prompted for a text file name to save the Log Viewer contents. Email this text file to Teledyne DALSA Technical Support when requested or as part of your initial contact email.

On-board Image Memory Requirements for Acquisitions

The Xtium-CLHS PX4 by default will allocate the maximum number of buffers that can fit in on-board memory based on the size of the acquired image before cropping, to a maximum of 65535 buffers. Note that an application can change the default number of on-board frame buffers using the Sapera LT API. Usually two buffers will ensure that the acquired video frame is complete and not corrupted in cases where the image transfer to host system memory may be interrupted and delayed by other host system processes. That is, there is no interruption to the image acquisition of one buffer by any delays in transfer of the other buffer (which contains the previously acquired video frame) to system memory.

If allocation for the requested number of buffers fails, the driver will reduce the number of on-board frame buffers requested until they can all fit. If there is not enough memory for 2 on-board buffers, the driver will reduce the size such that it allocates two partial buffers. This mode is dependent on reading out the image data to the host computer faster than the incoming acquisition.

The maximum number of buffers that can fit in on-board memory can be calculated as follows: (Total On-Board memory / (Buffer Size in Bytes + 256 Bytes used to store the DMA)).

For example, assuming 512MB of on-board memory and acquiring 1024 x 1024 x 8 bit images, the number of on-board buffers would be:
512 MB / [(1024 x 1024) + 256] = 511.875 => 511 on- board buffers.

Symptoms: CamExpert Detects no Boards

- When starting CamExpert, with no Teledyne DALSA board detected, CamExpert will start in offline mode. There is no error message and CamExpert is functional for creating or modifying a camera configuration file. If CamExpert should have detected an installed board frame grabber, troubleshoot the installation problem as described below.

Troubleshooting Procedure

When CamExpert detects no installed Teledyne DALSA board, there could be a hardware problem, a system bus problem, a kernel driver problem, or a software installation problem.

- Make certain that the card is properly seated in PCIe slot.
- Perform all installation checks described in this section before contacting Technical Support.
- Try the board in a different PCIe slot if available.

Symptoms: Xtium-CLHS PX4 Does Not Grab

Sapera CamExpert does start but you do not see an image and the frame rate displayed is 0.

- Verify the camera has power.
- Verify the Camera Link HS cable is connected to the camera.
- Verify the camera and timing parameters with the camera in free run mode.
- Verify you can grab with the camera in free run mode.
- Make certain that you provide an external trigger if the camera configuration file requires one. Use the software trigger feature of CamExpert if you do not have a trigger source.
- Make certain that the camera configuration is the required mode. This must match the camera configuration file. Refer to your camera datasheet.
- Try to snap one frame instead of continuous grab.
- Perform all installation checks described in this section before contacting Technical Support.

Symptoms: Card grabs black

You are able to use Sapera CamExpert, the displayed frame rate is as expected, but the display is always black.

- Set your camera to manual exposure mode and set the exposure to a longer period, plus open the lens iris.
- Try to snap one frame instead of continuous grab.
- Make certain that the input LUT is not programmed to output all '0's.
- A PCIe transfer issue sometimes causes this problem. No PCIe transfer takes place, so the frame rate is above 0 but nevertheless no image is displayed in CamExpert.
- Make certain that BUS MASTER bit in the PCIe configuration space is activated. Look in PCI Diagnostics for **BM** button under "Command" group. Make certain that the **BM** button is activated.

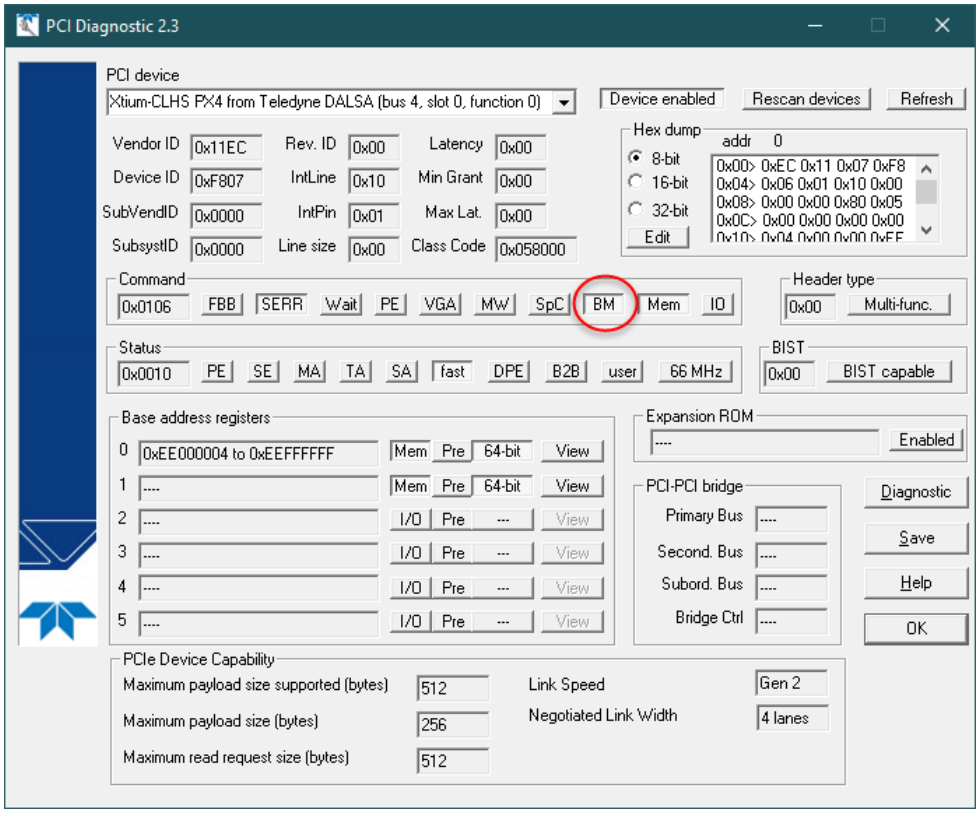


Figure 49: PCI Diagnostic – checking the BUS Master bit

- Perform all installation checks described in this section before contacting Technical Support.

Symptoms: Card acquisition bandwidth is less than expected

The Xtium-CLHS PX4 acquisition bandwidth is less than expected.

- Review the system for problems or conflicts with other expansion boards or drivers.
- Remove other PCI Express, PCI-32 or PCI-64 boards and check acquisition bandwidth again. Engineering has seen this case where other PCI boards in some systems cause limitations in transfers. Each system, with its combination of system motherboard and PCI boards, will be unique and must be tested for bandwidth limitations affecting the imaging application.
- Is the Xtium-CLHS PX4 installed in a PCI Express x16 slot?
  Note that some computer's x16 slot may only support non x16 boards at x1 or not at all. Check the computer documentation or test an Xtium-CLHS PX4 installation. The speed at which the board is running can be viewed using the Diagnostic Tool provided with the driver.
- Is the Xtium-CLHS PX4 installed in a PCI Express Gen1 slot?
  Some older computers only have PCIe Gen1 slots. The Generation at which the board is running can be viewed using the Diagnostic Tool provided with the driver.

Contact Information

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