MC133x

High Speed CMOS Camera

MC133x Hardware Reference Manual Rev. 1.02
Camera-Firmware: B1.21-V1.83-F2.64-C1.77
Kamera ID Nr.: MC133x

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1 General

1.1 Scope of this manual

This manual is written for the experienced programmer/ systems engineer who wants to learn all about the features of the high speed MC133x cameras to be integrated into its own products.

This manual does not cover the installation and the explanation of the driver software on the Host PC. This is covered in the Software Manual for the MC133x.

1.2 For customers in the U.S.A.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense. You are cautioned that any changes or modifications not expressly approved in this manual could void your authority to operate this equipment. The shielded interface cable recommended in this manual must be used with this equipment in order to comply with the limits for a computing device pursuant to Subpart J of Part 15 of FCC Rules.

1.3 For customers in Canada

This apparatus complies with the Class A limits for radio noise emissions set out in Radio Interference Regulations.

1.4 Pour utilisateurs au Canada

Cet appareil est conforme aux normes Classe A pour bruits radioélectriques, spécifiées dans le Règlement sur le brouillage radioélectrique.

1.5 Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Mikrotron customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Mikrotron for any damages resulting from such improper use or sale.

1.6 Declaration of conformity

Manufacturer: **Mikrotron GmbH**

Address: Landshuter Str. 20-22
D-85716 Unterschleissheim
Germany

Product: **camera** **MC1330..MC1337**

The dedicated products conform to the requirements of the Council Directives 89/336/EWG for the approximation of the laws of the Member States relating to electromagnetic consistency. The following standards were consulted for the conformity testing with regard to electromagnetic consistency.

EC regulation	Description
EN 61000-6-3	Electromagnetic compatibility
EN 61000-6-1	Immunity

Eching, June 06th. 2003

Mikrotron GmbH

Dipl.-Ing. Bernhard Mindermann
President of Mikrotron

1.7 Warranty Note

Do not open the body of the camera. The warranty becomes void if the body is opened.

1.8 Remarks, Warnings

This document contains important remarks and warnings. See the corresponding symbols:

	Important remark

	Attention, Warning

2 Introduction

The MC133x is a high resolution high speed CMOS camera camera with 1280•1024 pixel and up to 4GB of internal frame storage. Benefits of CMOS technology are high speed, random access to pixels with free programmability and low power. An internal NiMh battery allows for video recording at 500fps and 1280x1024 for more than ½ hour. Data retention for stored image sequences is up to a few hours without external power. Video data is accessible by the build-in GigaBit high speed serial interface.

The camera uses industry-standard C-Mount lenses. The sensor diagonal is 1,25“ with square pixels measuring 12µm.

2.1 Electronic „Freeze Frame“ Shutter

Preceding exposure, the contents of all light sensitive elements is cleared. When exposure terminates, accumulated charge is transferred to an analog memory associated which each pixel. It stays there until it is read out (and discharged) by the A/D conversion cycle. As all light sensitive elements are exposed at the same time, even fast moving objects are captured without geometric distortion.

2.2 Frame memory

The internal frame memory is build with four SDRAM boards of 512Mbytes or 1Gbyte each for a total capacity of up to 4GB.

2.3 Differences between the camera types

Mikrotron deliveres preferably the below types of cameras. A full explanation with all possible types is given in “Reading camera type & version”

Camera Identifier	Output	Memory	Color	Comment
32	GigaBit	2 pcs. of 1GB memory modules	Mono	
33	GigaBit	2 pcs. of 1GB memory modules	Color	
36	GigaBit	4 pcs. of 1GB memory modules	Mono	
37	GigaBit	4 pcs. of 1GB memory modules	Color	
52	GigaBit	2 pcs. of 512MB memory modules	Mono	Limited frame size/speed
53	GigaBit	2 pcs. of 512MB memory modules	Color	Limited frame size/speed
70	GigaBit	1 pcs. of 1GB memory modules	Mono	Limited frame size/speed
71	GigaBit	1 pcs. of 1GB memory modules	Color	Limited frame size/speed
72	GigaBit	2 pcs. of 1GB memory modules	Mono	Limited frame size/speed
73	GigaBit	2 pcs. of 1GB memory modules	Color	Limited frame size/speed

Table 2.3-1

The MC133x color cameras use a Bayer filter for color separation.

2.4 Using the camera

There are no serviceable parts inside the camera.. The camera may not be opened, otherwise guarantee is lost. Use dry, soft lens-cleaning tissue for cleaning lenses and, if necessary, the sensors window.

3 Getting started

Before starting to operate the camera, make sure that the following equipment is available:
Camera MC133x
C-Mount Lens
Mikrotron Support CD
Image processing system, e.g.: PC, with GigaBit Ethernet interface.

Additional items:
1 power supply 12VDC, 1,25A min.
1 power cable

ⓘ	To specify cables see chapter Connector pinning.

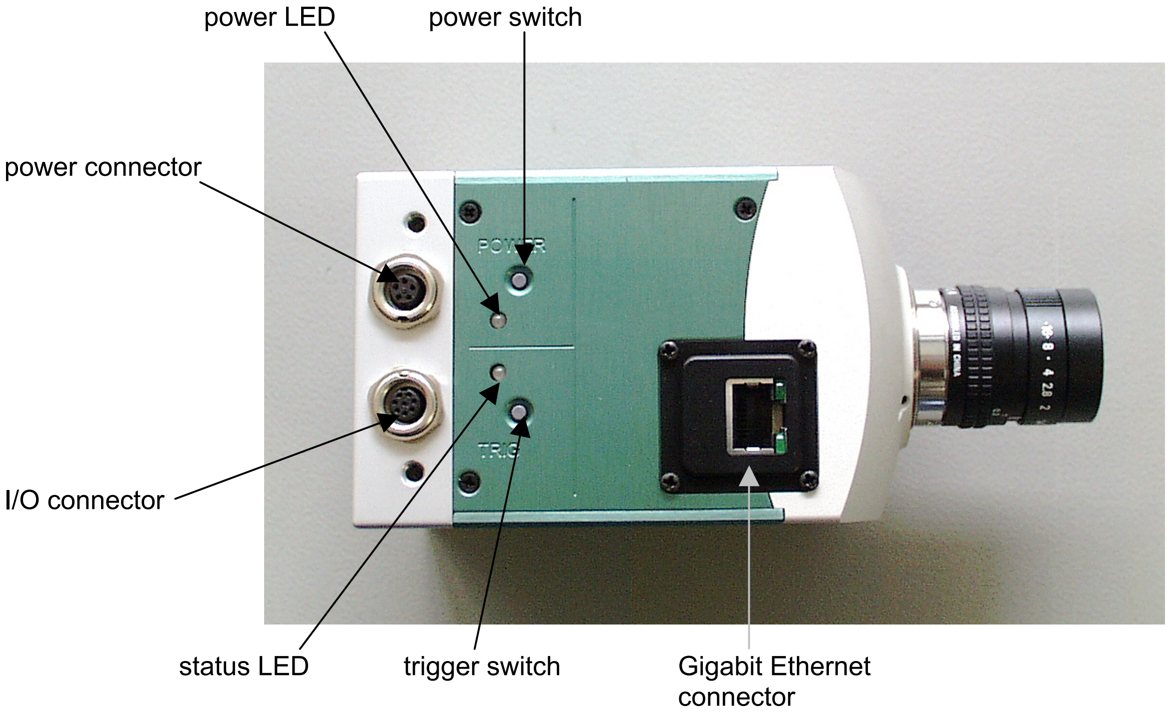
3.1 First steps

1. Install drivers and support software on the image processing system
2. Connect Ethernet cable between camera and PC.
3. Connect power cable.
4. Unscrew dust protection cover, screw in lens.
5. Switch on the image processing system and camera power supply

4 Hardware

4.1 Operating panel

All connectors, switches and LEDs are located on the right side of the MC133x camera.



4.1.1 Power

The MC133x can be operated from its internal NiMh battery and/or an external DC supply with 10,5 … 24 V @ 15 Watt max. See also [Connector pinning](#) .

4.1.1.1 Power switch

The power switch is located on the right side of the MC133x close to the power connector. Use a pen to press the button.

4.1.1.2 Power LED

The green LED above the power switch shows the power on condition if either battery power or external power is available and the charging condition.

Power LED	condition
Off	no power or battery fully charged
Red	Camera switched off, ext. power is on, battery is being charged to full capacity
Green	Power on
Yellow	Power on, battery is charged to app. 1/3 of its capacity

Table 4.1-1

4.1.1.3 Battery

The internal NiMh battery has 1.9Ah capacity and is charged automatically within 3-4h if external power supply is available. When the camera is operating and external power is applied, the battery is charged to app. 1/3 of its total capacity.

4.1.1.4 Status LED

The status LED shows the momentary operating status of the MC133x.

Status LED	Condition	Communication
Off	Power off	no
Off	Power on while new firmware is downloaded	Firmware download
Red	FPGA configuration failed, consult factory.	New firmware download possible
Orange after power on	FPGA configuration is in progress	no
Green	FPGA configuration done, waiting for commands	yes
Orange flashing	Circular recording in progress	yes
Orange	Circular recording is stopped	yes

Table 4.1-2

5 Initial setup

The MC133x is delivered with initial parameters and therefore does not need to be configured via the serial link.

5.1 Power up operating condition

After power up and sucessful firmware load (app. 15sec) the MC133x is prepared for circular recording @ 1280x1024 resolution and 500 frames/sec. The trigger switch or trigger pulse will start recording, the next switch or pulse will stop.

6 Configuration

The MC133x has several registers, r1..rf_h , each 10 bit wide, eight D/A registers, a1..a8, 8-bit wide, one clock table select register, 4 bit wide, two random clock select registers, 6-bytes wide, and three memory control registers, 32-bits wide. The contents of all the above registers is called a profile. The power-up profile may be stored into a non volatile memory.

Any change of a specific register through the serial interface is immediately processed and written to the volatile part of the memory and gets lost when power goes down. A command must be used to store the actual setting of the power-up profile in non volatile memory. After power-up the PowerUpProfile is loaded from the non-volatile to the volatile part of the memory.

All values are given in hexadecimal notation, e.g.: 0xff or 0ffh = 255.

6.1 Commands

ASCII strings are used to change camera settings. All commands start with a colon, followed by one command character (**case sensitive!**) and a value in hexadecimal notation with as many ASCII characters as required by the command. (2..8 characters)

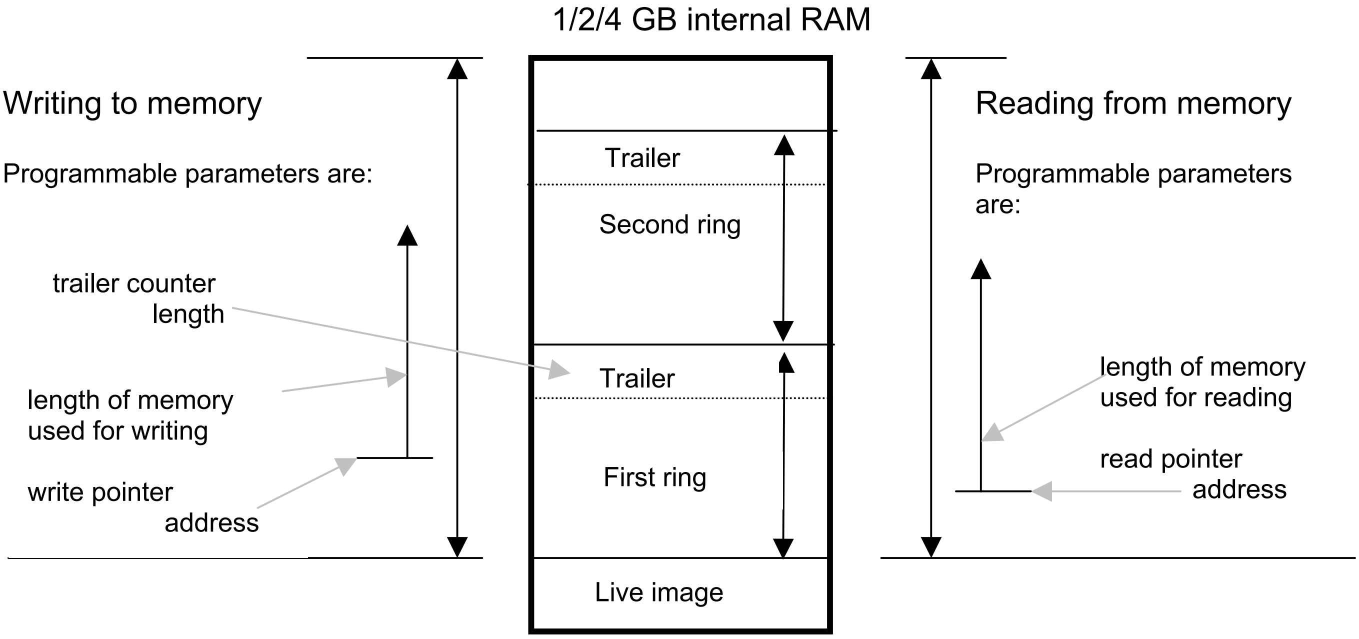
ⓘ	Commands are case sensitive

After a command has been recognized, processing is immediate, for all commands but the save type commands (:px). These need a EEPROM write time of app 1ms. An answer is provided with read type commans (:v, :w, :W, :z) or, if the command “command acknowledge flag” is set, after processing of each command an ACK or NAK character. Processing of wrong command is stopped immediately on recognizing the error. A new command must start with a colon.

6.2 Frame memory overview

There are two independent pointers with three associated counters. The write pointer together with its counter and an independent trailer counter controls writing to memory. The read pointer control reading. All pointers & counters use QWORD (=8-Bytes) entities.

Writing & reading can be done simultaneously up to a total bandwidth of app. 720Mbytes/sec. Read bandwidth is limited to 1/32th of write bandwidth when simultaneous write/read is selected. If read/write is done sequentially, read bandwidth is limited to 1/8 of write bandwidth.



6.2.1 Write pointer/counters

The write pointers start address is programmed in register: :R2[0,29..0], its length in :R2[8,29..0]. Writing to memory can be continuous where the write pointer wraps automatically to its programmed start address when the write counter has expired.

Even if continuous write is selected (:R1[1] = 1), this bit can be cleared at any time by command to stop writing on an expired write- or trailer counter.

If single write is selected, writing will automatically stop on an expired write- or trailer counter.

Multiple ring operation is possible with :R1[31..28] set according to :R1 bit description. Above shown is a two-ring operation.

The camera will continuously write to the first ring (1/2 of memory) until :R1[1] is lowered and the trailer counter is expired. It will then automatically continue to write to ring2 until the second occurrence of :R1[1]=0. At this time memory control logic will lower :R1[0]. The control programme must continuously poll :R1[0] to insure the :R1[1] will not be raised again when :R1[0] is read as 0.

6.2.1.1 Trailer counter

The trailer counter can count in parallel with the write counter, if selected. If selected (:R1[27] = 1), it will stop writing as soon as it is expired. This is useful if a continuous write is interrupted by an external signal but a previously defined number of frames should be recorded after the signal came in. (A “trailer” should be written.)

6.3 Memory commands

6.3.1 MC133x Memory Registers

Memory is organized in QWORDS (8-Bytes), the address is a linear physical address, it starts with 0 and runs up to 0x1FFFFFFF. A memory board contains either 512Mbytes or 1Gbyte. A

MC133x can be equipped with up to four boards of the same capacity for a maximum of 4GB. See :v command for camera identifier and memory sizes.

Use capital letter :R for programming of the memory register.

6.3.2 Memory write register :R1

Register 1 is the memory control register, which defines the size of the memory, image size (line length, no. of lines per image) and the image mode (live image, circular or non circular recording) and some control bits.

It can be read at any time with the :z1 command. It will return its content as 8 ASCII characters.

Syntax	Bits	Value	Description
:R1<xxxxxxxx> xxxxxxxx = 8 ASCII hex characters	0	0 1	Stop Write memory write frames to memory (address = R20xxxxxxx, length = :R28xxxxxxx)
	1	0 1	Write single frame to memory address write frames to memory continuous
	2	1|0	Reserved, was GigE/IEEE1394 switch, default 1
	3	0 1	512Mbyte memory modules 1Gbyte memory modules
	4	0 1	Normal operation reset logic, but not registers
	6..5	0,1,2	Ram size: 1,2,4GB
	7	0 1	Normal operation select internal grey scale camera: linelen = :1+R1[15..8] [qwords] numlin = 1+R1[27..16] [lines]
	15..8	0x9F..1	linelen = 1+:R1[15..8] [qwords]
	25..16	0x3ff..1	numlin = 1+R1[27..16] [lines]
	26	 0 1	Write wrap indicator (read only): Cleared when start write issued Set when write memory counter (:R2[8]) has reached its end position
	27	0 1	Select :R2[8] as write counter Select :R3[31..3] as write counter (trailer counter) (no longer used from FPGA Version C-1.69)
	30..28	0..4	Select number of rings: value 0,1,2,3 = 2,4,8,16 rings
	31	0 1	Single ring Multiple rings

Table 6.3-1

Bits 1..0 select mode of write operation:

If :R1[1..0] = 1, a single frame of length = :R2[8,29..0] is written to memory address :R2[0,29..0]. Bit 0 is cleared automatically on completion of this action.

If :R1[1..0] = 3, frames of length = :R2[8,29..0] are written to memory address :R2[0,29..0] continuously.

If Bit 1 is cleared while writing continuously, the current write action is continued until :R2[8,29..0]. is expired and then writing is stopped and Bit 0 is cleared automatically.

Bits 3..2 are selected according to the camera identifier retrieved with the :v command. These bits are read only.

Bit 4 can be cleared/set if a reset of memory control logic is required.

Bits 6..5 select the memory size: 0=1GB, 1=2GB, 3=4GB, must be initialized by control programme on power up.
Bit 7 selects an internal grey scale camera simulation. This can be used to fill memory with a known pattern.

Bits 15..8 selects a x-counter to generate internal LVAL signals that are necessary for the GigaBit interface. Calculate this value acoording to: :R1[15..8] = (:r5-:r4)*10/8

Bits 25..16 selects a y-counter to generate internal FVAL singnals that are necessary for the GigaBit interface. Calculate this value acoording to: :R1[25..16] = :r3

Linelen and numlin are used only with the GigaBit Ethernet interface. The length of video data stored in memory is defined only by :R2[8,29..0]. Make sure that :R2[8,29..0] is a multiple of Linelen+1*Numlin+1.

Bit 26 is read only and indicates that the write counter has expired once. It is cleared by toggling the write enable bit, e.g.: by restarting write. (:R1[0])

Bit 27 was select trailer counter, now reserved (V >= C-1.69)

Bit 28..30 select number of rings in multiple ring operation: 0..4 = 2,4,8,16 rings, (V >= 1.69)
Bit 31 selects multiple ring operation (V >= 1.69)

6.3.3 Memory pointer/counter register :R2

Memory register :R2 is address/length register. The two most significant bits of register 2 serve as index for WriteBaseAddress, ReadBaseAddress, WriteLength, and ReadLength. The other Bits serve as pointers/counters for memory read or write action. Regiser :R2[0,29..0], R2[4,29..0], :R2[8,29..0], :R2[c,29..0] can be read at any time with the :z2..:z5 command. The length registers reflect the momentary count value if :R2[8,29..0], :R2[c,29..0] is read while read or write action is in progress.

Syntax	Bits	Value	Description
:R2<ixxxxxxx> i = 0, 4, 8, 0xc xxxxxxx = 7 ASCII hex characters	31..30	0 4 8 c	WriteBaseAddress register [qwords] ReadBaseAddress register [qwords] WriteLength register [qwords] ReadLength register [qwords]
	29..0	0x3fffffff..5	Write/Read address/length [qwords]

Table 6.3-2

6.3.4 Memory read register :R3

Apart from 2 read control bits R3 is used to set the trailer counter.

Syntax	Bits	Value	Description
:R3<xxxxxxxx> xxxxxxxx = 8 ASCII hex characters	0	0 1	Stop Read memory read frames from memory (address = R24xxxxxxx, length = :R2Cxxxxxxx)
	1	0 1	Read single frame from memory address Read last previously written frame from memory continuously if :R1[1..0] is 3 and :R3[0] = 1. WriteXorRead frames to/from memory continuous if :R1[1..0] is 1
	2	0	reserved
	31..3	0x3fffffff..5	Write trailer counter

Table 6.3-3

Bits 1..0 select mode of read operation:

If :R3[1..0] = 1, a single frame of length = :R2[c,29..0] is read from memory address :R2[4,29..0]. Bit 0 is cleared automatically on completion of this action. Use this mode to selectively retrieve an image or a sequence of images from memory, one at a time.

If :R3[1..0] = 3, frames of length = :R2[c,29..0] are read from last previously completely written memory address continuously.

If Bit 1 is cleared while reading continuously, the current read action is continued until :R2[c,29..0]. is expired and then reading is stopped and Bit 0 is cleared automatically.

If :R3[1..0] = 3 and :R1[1..0] = 1, a special WriteXorRead action is done continuously. After one single frame is written, a single frame is read. This is repeated indefinite until some other mode is selected. WriteXorRead can be used for automatic life display action without issuing memory commands. It maintains the integrity of the images read. Because reading is much slower than writing (maximum ¼ of write bandwidth) an image being read is otherwise overwritten by new images while reading is in progress.

If :R3[1..0] = 3 and :R1[1..0] = 3, memory is written and read at the same time. Maximum read bandwidth is 1/32 of write bandwidth. Use this mode only fo testing.

Bits 31..3 contains the trailer counter. This counter counts qwords to be written after Bit 2 of :R3 has been set. Make sure that the continuous write Bit is also clear when trailer counter is activated. Register 3 can be read at any time with the :z6 command. It will return its content as 8 ASCII characters.

6.3.5 Concatenated memory register settings

Register :R1 and :R3 Bits 1..0 define several modes of memory operation:

:R1[1..0]	:R3[1..0]	mode	remark
0	0	memory stop	no memory activity, memory is refreshed
1	0	Write single	Write a single frame or a sequence of frames with length: :R2[8,29..0]. to memory pointed to by :R2[0,29..0].
3	0	Write continuous	Write a single frame or a sequence of frames with length: :R2[4,29..0]. to memory pointed to by :R2[0,29..0]. continuously. Use this mode for circular storage. Stop continuous writing by clearing :R1[1] when :R3[31..2] is 0. If :R3[31..2] is > 0, as many qwords are written as defined by the trailer counter after a stop is issued. (not implemented in Ver. C1.28)
0	1	Read single	Read a single frame or a sequence of frames with length: :R2[c,29..0] from memory pointed to by :R2 [4,29..0].

			Use this command to read memory. Set the read length to one or more frames. Length of multiple frames is more efficient, because less commands are issued.
3	1	Write continuous, read single	Use this mode to read data that is being circular written.
1	3	WriteXorRead	Memory is alternatively written and read. Use this mode for live display.
3	3	Write and Read continuous	Frame to be read is the last previously and completely written frame. Use this mode for live display while (continuous) recording is in progress. Size for read frame is :R2[0xC,29..0]

Table 6.3-4

6.3.6 Read single memory registers

Use :z1 .. :z6 commands to read memory registers :R1..:R3. Eight ASCII characters with their hex contents are returned.

Syntax	Description
:z1	Read :R1, Bit 0 might be clear thru previous stop write action
:z2	Read :R2[0,29..0]
:z3	Read :R2[4,29..0]
:z4	Read actual write pointer
:z5	Read actual read pointer
:z6	Read :R3, Bit 0 might be clear thru previous stop read action

Result of command :z4 and :z5 will change on repeated readings if memory read/write is in progress.

6.3.7 Read all memory registers

Use command :Z to read all memory registers R1, R2x and R3 with one instruction. The values are only stored in a volatile memory after non-circular or circular recording mode stopped. The values will be kept until another recording sequence stops and the values are updated. The default value for all registers, which will be returned after power up and before starting a recording sequence for the first time is 00000000 (char).

Syntax	Description
:Z	Read all memory registers

Response (e.g.1.280 x 1.024, 500 fps, 2GB memory, after continuous recording stopped):

07ff9f07000280004433000087fd0000c0028000200800010 5af8258

R1 R20 R24 R28 R2C R3 R_{AWP}

The values of R1, R20, R24, R28, R2C and R3 are saved directly after recording starts. R_{AWP} is the actual write pointer, which is read just after recording stops.

6.4 MC133x sensor commands

The sensor logic of the MC133x is the same as the logic of the industrie proven MC131x camera series. Therefore all MC1310 commands apply for the MC133x.

Syntax	Range	Answer	Description
:a<n><xx>	<n> = 1...8 <xx> = 0...ff_h	--	Set one of eight analog voltages for the sensor
:b<n>	<n> = 0...4	--	Select baud rate: 0=9600 Bd (default setting), 1=19.2 kBd, 2=38.4 kBd, 3=56.8 kBd, 4=115.2 kBd
:c	--	--	RESET and new Initialization of the camera, new load of PowerUpProfile. Duration: some seconds
:d	--	--	receive and save new memory fpga configuration
:e...	--	--	receive and save new sensor fpga configuration
:h			
:i			
:pc	--	--	save PowerUpProfile to non volatile memory
:r<n>	<n> = 1...f_h	--	Write a FPGA - register
:t<n><m>	<n> = 00..$7f_h$ <m> = 00..ff_h	--	Short setting of X- position in units of 10 pixel and Y-position in units of 4 lines.
:v	--	#12345- V1.10-F1.29	Read serial number (#), microcontroller - version (V...) and FPGA - version (F...).
:w	--	camera profile: 44 bytes in hex	Read actual PowerUpProfile, data output in hex
:A<n>	<n> = „y“,“Y“,“n“,“N“		En- or disable a command acknowledge or not acknowledge (ACK or NAK)
:I			
:S	6 Byte Code	--	Program sensor and pixel clock directly.
:T			
:W	--	Camera profile: 44 bytes in ASCII	Read actual PowerUpProfile, data output in ASCII

6.4.1 Sensor registers

All sensor registers are 10 Bits wide and represented by three ASCII hex characters 000..3ff.

Syntax	Bits	Value	Description
:r1<xxx>	9..0	0..0x3ff	Address of irst line to be output
:r2<xxx>	9..0	0..0x3ff	Exposure time = :r2[] * Sensor clock
:r3<xxx>	9..0	0..0x3ff	Number of lines + 1
:r4<xxx>	9..0	0..0x7f	Address of first pixel of a line
:r5<xxx>	9..0	0..0x7f	Address of last pixel of a line
:r6<xxx>	9..0		Modes of operation
	0	0	reserved
	1	0	reserved
	2	0 1	Normal operation Vertical binning
	3	0	Reserved
	7..4	0	Camera stop
		1	synchronous operation, no shutter
		3	synchronous operation, with shutter
		0xB	Asynchronous exposure, shutter control by pulse width
		0xF	Asynchronous exposure, shutter control by timer
	8	0	reserved
	9	0	reserved
:r7<xxx>	9..0		Modes of operation
	0	0	reserved
	1	1->0->1	clear image timer/counter
	3..2	0 1 2 3	Digital gain 0, multiply grey values by 1 Digital gain 0, multiply grey values by 2 Digital gain 0, multiply grey values by 4 Digital gain 0, multiply grey values by 8
	4	0 1	Normal operation enable hor pixelbinning
	5	0	reserved
	6		reserved
	7	1	Reserved
	8	0	Invert trigger input
	9	0	reserved
:r8<xxx>	9..0	0..0x7f	ImageBLITZ window x-start (mod10)
:r9<xxx>	9..0	0..0x7f	ImageBLITZ window x-end (mod10)
:ra<xxx>	9..0	0..0xff	threshold
:rb<xxx>	9..0	0..0x3ff	Release condition 10 is :ra[8]
:rc<xxx>	9..0	0..0x3ff	ImageBLITZ top line address
:rd<xxx>	9..0	0..0x3ff	ImageBLITZ bottom line address
:re<xxx>	9..0	0..0x3ff	Write ImageInformationField
:rf<xxx>	0 1 2 3 4 5 6 9..7	1 1 0/1 1 0/1 0 0/1 0	Enable external sync signal Select „arm“ signal on strobe output Set “arm” signal accordingly Invert external Sync Signal auto async trigger with :r2[9..0] = 1000..1ms (low light Reserved select trigger debounce 100/10 ms Reserved

Tabelle 6.4-1

6.4.2 Image quality

There are three D/A converter to influence image quality: FPN, Gain, and Black up. FPN, Gain and especially Black might be adjusted if sensor clock changes. All three parameters are stored in non-volatile memory as part of the selected profile.

6.4.2.1 FPN

The **F**ixed **P**attern **N**oise setting reduces the fixed pattern noise that is typical to CMOS sensors. This level might be changed if the sensor clock frequency is changed. For adjustment set the lens out of focus and to a medium grey level. Lower FPN until a heavy pattern appears. Then raise by a few points.

Command: **:a1<x_1x_0>** <x_1x_0> : Range, typ. 55h ... 80h
Response: none

6.4.2.2 Gain

This is the threshold for the A/D converters. Its standard value is 66h for app. 1V. One step is app. 10mV. To increase the gain the value of a2 must be lowered.

Command: **:a2<x_1x_0>** <x_1x_0> : Range,
typ. 30h ... 80h
Response: none

6.4.2.3 Black Level

Change Black Level if sensor clock changes. Increase this parameter until grey values in no light condition (closed lens) are close to zero.

Command: **:a5<x_1x_0>** <x_1x_0>: Range,
typ. 00h ...ffh
Response: none

6.4.3 Image size and position

Image size and position within the sensor is defined by four parameters:

Bit(s)	Description
r1[9..0]	Number of first line, 0..3FD$_h$
r3[9..0]	Number of lines, 0..3FF$_h$
r4[6..0]	Address/10 of the first pixel
r5[6..0]	Address/10 of the last pixel

Table 6.4-2

6.4.3.1 Address of the first line

Register r1 defines the first line to be displayed.

Command: **:r1<$x_2x_1x_0$>** <$x_2x_1x_0$> ... Range 000h ...3fdh
Response: none

Example: :r1100
100h = image starts at line 257

> If dual column binning is activated, r1 is doubled within the camera logic.

6.4.3.2 Number of lines

Register r3 defines the number of lines to output.

Command: **:r3<*x₂x₁x₀*>** <*x₂x₁x₀*> ... Range 000 h ...3ffh
Response: none

Example: :r3200 200h = display 513 lines

ⓘ	The sum of r1 and r3 must be ≤ 0x3ff/1023 or 0x1ff/511 if dual column binning is activated!

6.4.3.3 Address of the first pixel of a line

Register r4 defines the leftmost pixel. The value is the pixel address divided by ten.

Command: **:r4<*x₂x₁x₀*>** <*x₂x₁x₀*> ... Range 000h ...7fh
Response: none

Calculation of the value of r4:
Value of r4 = Pixel-Nr./10

6.4.3.4 Address of the last pixel of a line

Register r4 defines the rightmost pixel. The value is the pixeladress divided by ten.

Command: **:r5<*x₂x₁x₀*>** <*x₂x₁x₀*> ... Range 000h ...07fh
Response: none

Calculation of the value of r5:
Value of r5 = Pixel-Nr./10

ⓘ	The difference r5 - r4 must be in the range: 0 ≤ r5-r4 ≤ 7fh and only values mod40 are valid.

6.4.4 Clock selection

The MC133x works with two clocks (pixel and sensor clock) inside. Pixel clock is set to a fixed value of 90,112 MHz and not adjustable. Sensor clock must be adjusted in dependence of the chosen frame rate.

Calculation of sensor clock: F_{SENS} = 136 • FR • (r3[9..0]+1)

FSENS	...	sensor clock in Hz
FR	...	frame rate in 1/s (=Hz)
r3[9..0]	...	no. of lines per frame

The calculated sensor clock has to be translated into a 6 character long code (examples see chapter Frequency selection).

To set the clock in the camera the code must be sent to the camera together with the following command:

Command **:S <x_0>**
< x_0> ... 6 characters, as described in chapter Frequency selection

ⓘ	You've to change the clock when the speed and/or the image format changes. In this case please follow the recommended command sequence of chapter Image Format/Speed change.

6.4.5 Image Format/Speed change

There are several steps necessary for a change of image format:

1) Make sure that the memory controller is idle. (:R3/R1[1..0]==0).
   If the camera is in Rx orW mode (life image) when change is requested, stop this mode and wait for 1/fps (100ms max for 10fps) until the last pending image has been output completely.
2) Set memory controller to new linelen/numlin (:R1) and number of qwords (:R2[8/Cxxxxxxx]) .
3) Set GigE interface to new linelen/numlin parameters
4) Disable sensor controller with :r6[4] = 0
5) Set sensor controller to new image size (:r1,:r2, :r3, :r4, :r5)
6) Set new sensor Clock (:S4xxxxxx).
7) Enable sensor controller (:r6[4]=1) and wait for 1/fps to insure that there are output correct images
8) Enable (if necessary) the memory controller to life image output.

If a speed change is requested without a format change, the new sensor clock command can be sent without any additional action, even if the camera is in RxorW (life) mode. Do not send the pixel clock code (:S6…), even if it is the same as it was before the requested change.

6.4.6 Exposure control

Exposure control is selected with register r6[7..4] and register r2[9..0].

Bit(s)	Description
r6[7..4]	Type of exposure
r2[9..0]	Exposure time

table 6-1

Bits 9..0 of register r2 define exposure time:

$$T_{exp} = (:r2[9..0]) \bullet 1/F_{sens} \bullet 136 \quad [sec]$$

T_{exp} ...exposure time
F_{sens}... Sensorclock

6.4.6.1 Type of exposure

The MC133x can expose the images synchronous or asynchronous.
Synchronous means that the next image is exposed, while the current image is output.
With asynchronous exposure, an external signal starts exposure, and the exposed image is output after the exposure ends. Exposure time is defined either by an internal timer or by the width of the external EXP – signal. Bits 7..4 of registers r6 define exposure type: (**:r6[7..4]**).

r6 Bits	7	6	5	4
Camera stop	x	x	x	0
Synchronous	0	0	0	1
Synchronous, with electr. shutter	0	0	1	1
Asynchronous, pulse width	1	0	1	1
Asynchronous, timer	1	1	1	1

Table 6.4-3

6.4.6.2 Synchronous operation with shutter

In the sensor is implemented a freeze frame shutter, which allows to reduce the exposure time in steps of one line. The minimum value of the exposure time is the duration of 2 line periods, which is determined by the value of r2 (min. 001h).

Command: **:r2<*x*$_2$*x*$_1$*x*$_0$>**
<$x_2x_1x_0$> ... Range 001h ...3ffh
Response: none

Exposure time T_B :

$Tt_B = r2 \bullet T_{ZZ} - T_{ZZ} / 2$

T_B ... exposure time in s
r2 ... value of register 2
T_{ZZ} ... time/line
$T_{zz} = 1/F_{sens} * 136$ [s]
Tt_{zz} ... Time/line
F_{sens}... sensor clock

Typical exposure times:

Sensor clock frequency (MHz)	Zeit/Zeile (µsec)	r2 bei 1/5.000 s	r2 bei 1/10.000 s
66	2,06	97	49
33	4,12	49	24
13,2	10,3	19	10
6,6	20,6	10	5

Table 6.4-4

6.4.6.3 Frame rate with synchronous exposure

The frame rate with synchronous exposure is direct proportional to the selected number of lines.

The time for one line is::

$T_{zz} = 1/F_{sens} \bullet 136$ [sec]

T_{zz} ...time/line
F_{sens}... Sensorclock

Frame rate: = 1 / (time/line • number of lines+1) or:
= $F_{sens}/ (136 \bullet (r3[9..0] +2))$

6.4.6.4 External Synchronisation

Multiple MC133x cameras can be synchronized to an external signal with a frequency that is below the free-running frame rate of the cameras to be synchronized. A “master – camera” strobe output can be used to synchronize the “slave” cameras. Make sure that the “master” cameras free-running frame rate is selected to be a little bit less than the “slave”s cameras.

Use Pin 8 of the I/O connector as input.

Synchronisation is enabled with register **:rf[0] = 1**. Use only with sychronous exposure (:r6[7..4]=3)

6.4.6.5 Asynchronous exposure, shutter control by timer

This operating mode is selected with register 6:
:r6[7..4] = 0xf

The asynchronous exposure time is dependent on :r2[9..0]. The exposure timer counts as many lines as are defined in register :r2[9..0].

Exposure time:

$T_B = 1/F_{sens} * 136 \bullet (1+r2[9..0])$ [Sec]

T_B ... exposure time

F_{sens}.. sensor clock

example: sensor clock = 66MHz

value of r2[9..0] = 6

$T_B = 136 \bullet 6 \bullet 15$ ns = 12,2 µs

6.4.6.6 Frame rate with asynchronous exposure

The frame rate with asynchronous exposure = Frame rate with synchronous exposure – (1 / exposure time).

6.4.7 ImageBLITZ trigger

This signal is generated in the sensor fpga and fed through the microntroller to the memory control fpga to stop a cyclic recording action just as the external trigger switch/signal.

When activated, the grey values of an ROI:

:r8[9..0] = x-start(mod10),
:r9[9..0] = x-end(mod10),
:rc[9..0] = top line address,
:rd[9..0] = bottom line address

within the visible image area are stored as reference, every time the ImageBLITZ trigger is activated:

:r7[0] = 0->1

ⓘ	**The total number of pixel within the trigger window may not exceed 20480 pixel.**

After activation of ImageBLITZ, all subsequent images within the given ROI are compared to the stored image, and if at least once within a group of 10 pixel the absolute value of the difference between actual grey value and stored grey value exceeds the limit given in:

:ra[7..0] = threshold

the release condition counter is incremented. If the counter value equals the value given in:

:rb[9..0] = release condition [9..0]
:ra[8] = release condition 10

the ImageBLITZ output signal is activated and stored until the next activation of ImageBLITZ:

:r7[0] = 0->1

happens.

The trigger ROI is marked by a top & bottom dashed line when activated:

:ra[9] = 1

6.4.8 Horizontal pixelbinning

Pixelbinning adds the gray values of two adjacent pixels and outputs it as one pixel with double sensitivity. In X-direction only 512 pixels are needed to cover the sensors full size.

To retain aspect ratio, every second line is discarded, if this feature is not disabled by setting Bit 8 of register 6 **(:r61xx)** or vertical pixelbinning is activated.

Command: **:r7010**
Response: none

If discarding of every other line is not disabled **(:r61xx)**, the contents of **:r1** is doubled in camera logic. To address a specific line on the sensor, the value written into **:r1** has to be divided by two and **:r3** must not exceed 1ffh.

Example:
To output 256 lines from line 128, set r1 = 63 and r3 = 255 (=0xff).

6.4.9 Vertical pixelbinning

Vertical pixelbinning adds the gray values of two superimposed pixel of a column. This doubles sensitivity and vertical field of view. To retain aspect ratio, in addition horizontal binning must be activated.

To activate, set bit 2 in register 6.

Command example: **:r6034**
Response: none

6.4.10 Digital gain

Digital gain selection is only possible with video data width 2 x 8-Bit or 8 x 8-Bit. Out of the 10-bits sensor data either the most significant 8 bits (gain 1), or bits 8..1 (gain 2), or the least significant 8 bits (gain 4) are selected.

Command: **:r700x**
x = 0: gain 1
x = 4: gain 2
x = 8: gain 4

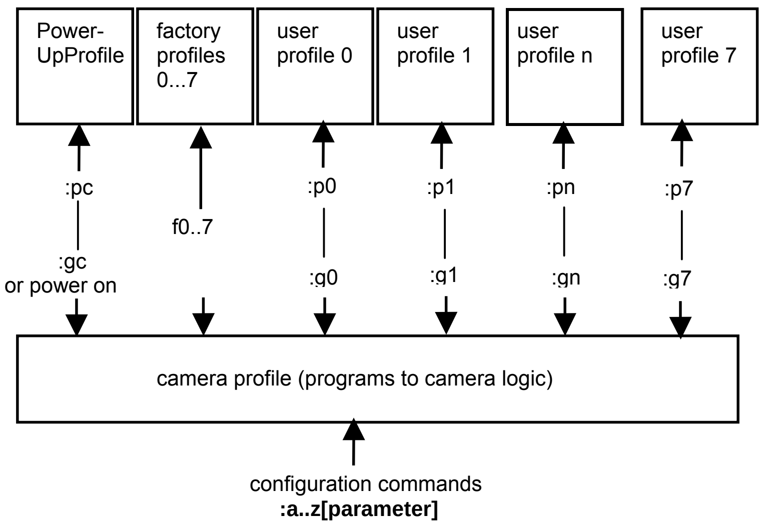
6.4.11 Test image

For testing of camera logic and video data transmission, sensor data can be replaced by an internal gray scale pattern with pixel values of 0..127. Use digital gain command to see pixel values of 0..255.

Command example: **:r7040** r7[6]
Response: none

6.4.12 Profile processing

All camera settings are loaded or stored as complete data blocks (= Profiles). There are 17 profiles, the Camera profile, the PowerUpProfile, eight factory profiles and eight user profiles.



6.4.12.1 Read Camera profile

The response to the read Camera profile command **:w** is a hex string of the contents of all actual camera registers.

Command: **:w**
Response(e.g.): 6d774ac800006a1c61e88c41898c0003ff3ff

0000800300000000000000000000000000000000000000
all values hex, e.g.: $70_{HEX} = 112_{DEC}$

Sequence of transmitted data bytes:

A1 A2 A3 A4 A5 A6 A7 A8 Sa1 Sa2 Sa3 Sb1 Sb2 Sb3 R1h R1l ... R15h R15l ↵

A1...A8	image level control (FPN, contrast…)
Sa1 Sa2 Sa3	3 Byte synthesizer code of pixel clock
Sb1 Sb2 Sb3	3 synthesizer code of sensor clock

(see chapter Arbitrary selection od sensor and pixel clock)

R1…R15 image control (image position, size, sync.…)

R1h ...	high Byte R1
R1l ...	low Byte R1
↵ ...	CR+LF (0dh + 0ah)

6.4.12.2 Write user profile

The PowerUpProfile is transferred to one of the eight user profiles.

Command: **:p<*n*>** <*n*> = 0 ... 7,c

> Issue this command only, if the PowerUpProfile was successfully tested.

6.4.12.3 Load user profile

Load one of eight user profiles to the PowerUpProfile.

Command: **:g<*n*>** <*n*> = 0 ... 7, c

6.4.12.4 Load factory profile

The eight factory profiles can be read but not changed by the user.

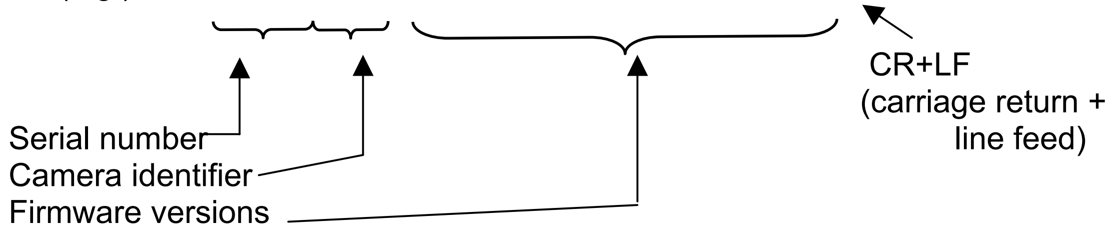
Command: **:f<*n*>** <*n*> = 0 ... 7

6.4.13 Read serial number, firmware revision and model

The serial number the firmware revision and the camera identification can be read with the **:v** command.

Command: **:v**

Response(e.g.): #312340033-B1.21-V1.56-F2.56-C1.68↵



Firmware versions e.g.:

B1.21 ...	bootloader program version of microcontroller
V1.56 ...	application program version of microcontroller
F2.56 ...	sensor FPGA program version
C1.68 ...	memory FPGA program version

Camera Identifier	Output	Memory	Colour	Comment
Even numbers	any	any	monochrome	
Odd numbers	any	any	colour	
Second digit even	IEEE1394	any	any	No longer supported (as of 1Q. 2005)
Second digit odd	GigaBit	any	any	
17..10	GigaBit	4..1 pcs. of 512MB memory modules	any	
37..30	GigaBit	4..1 pcs. of 1GB memory modules	any	
57..50	GigaBit	4..1 pcs. of 512MB memory modules	any	Limited frame size/speed
77..70	GigaBit	4..1 pcs. of 1GB memory modules	any	Limited frame size/speed

Table 6.4-5

6.4.13.1 Read camera settings

The actual camera settings can be read out. The answer are the values of all camera registers.

Command: :w Output as hexadecimal digits (44 Bytes)
:W Output as ASCII-String

Example for ":w" (output as hex digits, 44 Databytes + CR + LF):

6d6448c66500650061e88c41898c0000
03f f03f f0000007f 0030000000000000
000000000000000000000000↵

CR+LF

Example for ":W" (output as ASCII string, 91 Bytes total, 88 databytes, 1x CR preceding the data bytes, 1x CR after 32 ASCII-characters and 1x CR after 64 ASCII- characters):

6d6448c66500650061e88c41898c0000
03f f03f f0000007f 0030000000000000
000000000000000000000000↵

CR

Assignment of data to camera parameters:

6d6448c665006500 61e88c41898c 0000
03f f03f f0000007f 0030000000000000
000000000000000000000000↵

analog settings
image size & position
Codes for pixel- and Sensorclock

transmitted bytes:
A1 A2 A3 A4 A5 A6 A7 A8 Sa1 Sa2 Sa3 Sb1 Sb2 Sb3
R1h R1l ... R15h R15l↵

A1...A8	analog settings
Sa1 Sa2 Sa3	3 Bytes frequency codes of pixelclock (see 6.7)
Sb1 Sb2 Sb3	3 Byte frequency codes for sensorclock (see 6.7)

R1…R15	image size & position
R1h ...	high Byte Register1
R1l ...	low Byte Register1
↵ ...	CR+LF (0dh + 0ah)

Abb.	description	hex. Code
CR	carriage return	0d
LF	line feed	0a

6.4.14 Image information field

Every image is marked with 32 Bytes that replace the first 32 Pixels of every image.

Bytes	Value	Description
3..0	0xFF00FF00	start of image marker
5..4	0..0xFFFF	image counter
7..6	0..0x3FF	image row start address
7, Bits 7..4	0..0xF0	Digital Input 4..1
14..8	0..0xFFFFFFF	Absolute timer, counts every 49,913194444...usec, clear when ImageInformation field is deactivated
15	0..0xFF	Analog Input
23..16	ASCII string	First line of free text
27..24	Camera status 0 1 2 3 7..4 15..8 25..16 26 27	 Enable write (copy of :R1[0]) Write continuous (copy of :R1[1]) Enable read (copy of :R3[0]) Read continuous (copy of :R3[1]) Write counter lsb, saturated to 0xf Linelen-1 (mod8) Numlin-1 Write counter wrap (copy of :R1[26]) Select trailer (copy of :R1[27])
31..28	Camera status	Copy of 27..24

Table 6.4-6

Bytes 23..16 are automatically updated when the first line of Free Text (next chapter) is written.

The image counter and the absolute timer is cleared when this function is deactivated/activated. (toggle r7[1])

Command example: **:r7002** r7[1]
Response: none

6.4.14.1 Memory information field

The life image (memory space 0..0x28000) is marked with 76 Bytes that replace Pixel 33 to 110 of that image. Every four Pixel contain a QWORD with the following description:

Qwords	Bits	Description
15..0	28..0 31	Value of trailer counter within one of 16 rings Wrap flag within one of 16 rings
16	31..0	Register :R1 when recording was started
17	31..0	Register :R2[8] when recording was started
18	31..0	Register :R3 when recording was started

Table 6.4-7

6.4.15 Free Text

Up to 16 lines, 16 characters of free text are stored as long as the MC133x is powered. Use this command to store descriptive text and absolute time together with recorded sequences.

Command: **:i<n><16char.text>** ; write free text
n = text line number

Command: **:I<n>** ; read free text
n = text line number

6.4.16 Firmware

6.4.16.1 Update Firmware

MC133x's logic is integrated into two FPGAs (**F**ield **P**rogrammable **G**ate **A**rray), which's configuration is stored in an EEPROM. Upon power up or a command the FPGA is loaded with this configuration. Configuration data can be downloaded via the Gigabit Ethernet interface. Mikrotron may provide configuration files (*.ibf) on request.

After download of configuration data, this data is permanently stored in EEPROM and the FPGA is configured with the new data. Besides a power cycle, the **:c** command can be used to reconfigure the FPGA with the internally stored configuration data.

Download of *.ibf file via serial link with 19.200 Bd takes app. 1.5 min. There should be no loss of power or communication during this time!

6.4.16.2 Reset and configuration of the internal FPGA

The command **:c** executes a reset in the camera. The FPGA will be reconfigured and all internal registers reloaded with the last saved PowerUpProfile. The FPGA is also configured after each power up.

Command: **:c**
Response: none

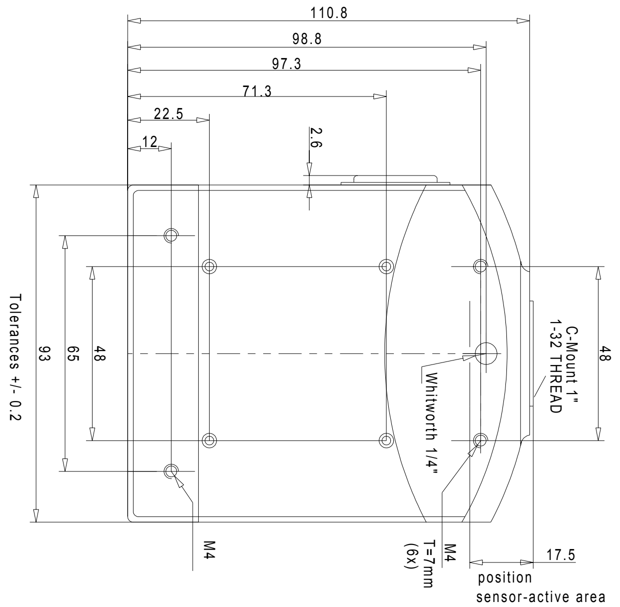
7 Mechanical dimensions

7.1 Camera body

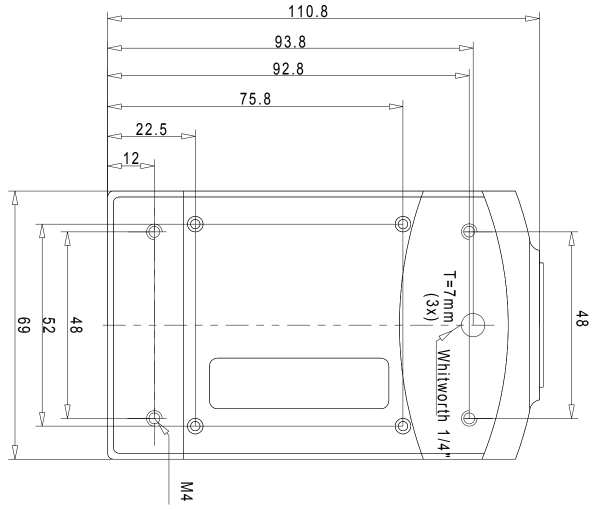
The camera body is with its dimensions of 93 x 69 x 111 mm (WxHxD, without lens) very compact. To fasten the camera there are two mounting holes M4x7mm and one tripod connection on each side available.

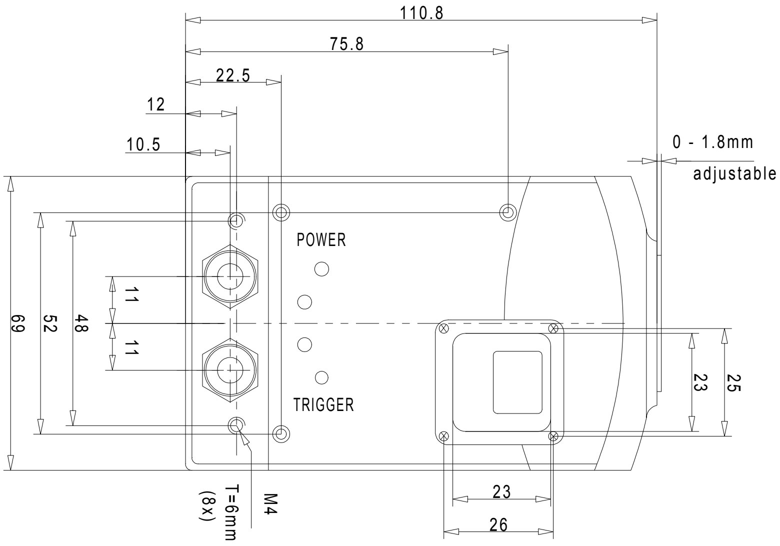
7.1.1 Dimensioned drawing, top/bottom view

Maximum torque for M4 fastening screws: 2.5 Nm



7.1.2 Dimensioned drawing, side view





7.2 Lens adjustment

7.2.1 Adjustable lens adapter

For fine adjustment of the focal length a lens adapter with an adjustment range of ± 1 mm is provided. Use the three screws nearby the sensor window to fasten the lens adapter after a proper adjustment together with the chosen lens.

7.2.2 Lens selection

Due to the size of the sensor use C-Mount lenses with the largest possible optical diameter or an adapter for lenses like F-Mount, especially for lenses with a focal length < 25mm..

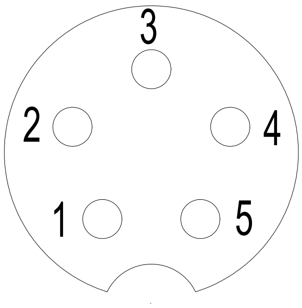
8 Technical Features

8.1 Technical Data

MC133x	Monochrome Bayer Filter
Number of pixel	1280 x 1024
Pixel size	12 x 12 µm
Active area	15,36 (H) x 12,29 (V) mm
Fill factor	40%
Sensitivity at 550 nm @ Vref = 1V (a2 = 66h)	1600LSB/lux-sec
Spectral response	400..800nm
Shutter	Electronic „Freeze Frame“ Shutter
Trigger	Asynchronous shutter, shutter time selectable with internal timer
Internal Dynamic	59 dB
Power supply	10,5 ... 24 V
Power consumption max., continuous recording @ 660 Mbytes/sec Thermal resistance typ.	15 W 6.25°/W
Serial data link	Thru GigaBit Ethernet, baud rate 19.200 Bd
Digital video MC133x	GigaBit Ethernet
Shock & vibration	70g, 7grms
Dimensions (WxHxD)	94 x 70 x 106 mm
Case temperature	+5 ... +60° C
Weight	ca. 1030 g
Lens mount	C-mount

Table 8.1-1

8.2 Power connector



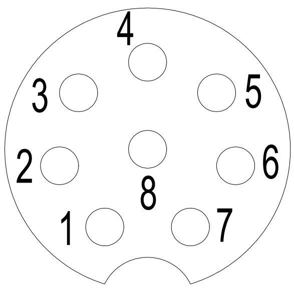
Mating connector, view: Solder side
180°: Binder # 99-0413-00-05 (w/o shielding)
180°; Binder # 99-0413-10-05 (shielded, recommended)
90°: Binder # 99-0413-70-05 (w/o shielding)
90°: Binder # 99-0413-75-05 (shielded, recommended)

www.binder-connector.de

Pin Nr.	Signal Level	Description
1	Power	+10,5..24V=
2	Power	+10,5..24V=
3		
4	Power	GND
5	Power	GND

Table 8.2-1

8.3 Signal input connector



Mating connector, view: Solder side
180°: Binder # 99-0425-00-08 (w/o shielding)
180°; Binder # 99-0425-10-08 (shielded, recommend.)
90°: Binder # 99-0425-70-08 (w/o shielding)
90°: Binder # 99-0425-75-08 (shielded, recommend.)

www.binder-connector.de

Pin Nr.	Signal Level	Description
1		GND
2	0..2.5V@ 1MΩ	Analog input votage, 8-Bit resolution
3	LVTTL	STROBE Output
4	LVTTL	Digital Input 1
5	LVTTL	Digital Input 2
6	LVTTL	Digital Input 3
7	LVTTL	Digital Input 4/ Trigger Input
8	LVTTL	SYNC Input

Table 8.3-1

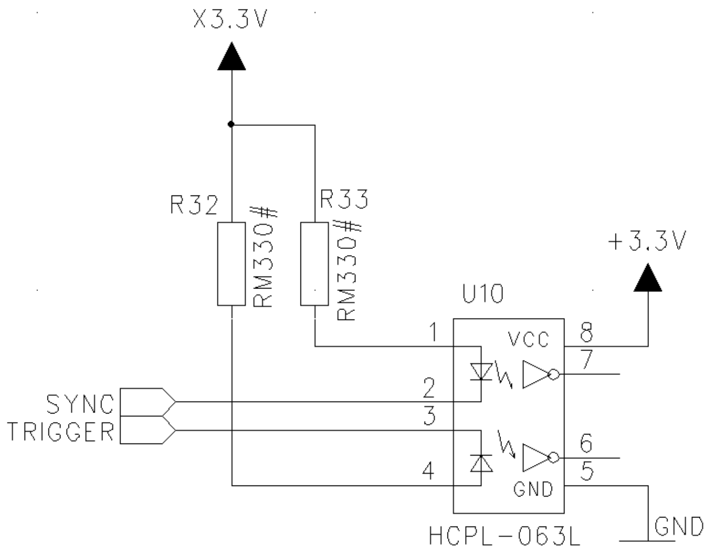
8.4 I/O signals

8.4.1 TRIGGER / SYNC input signal definition

The Digital Input 4/ Trigger and the Sync Input is isolated from the rest of the circuitry by an optocoupler. The pull-up resistors R33/R32 are powered by a internal DC/DC converter (X3.3V). The optocoupler will switch if the input is connected to the common GND signal (Pin 1 on Signal I/O connector).

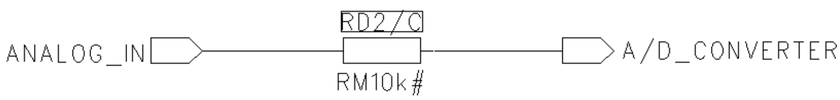
A positive edge on the SYNC input will output the next image, if the positive “Sync edge” is selected in the camera menu. (:rf[3] = 0/1 = pos/neg edge)

A positive edge on the Trigger input will stop a circular recording if the positive “Trigger edge” is selected in the camera menu.(:r7[8])
The trigger input is debounced with 100ms retrigger suppress time.



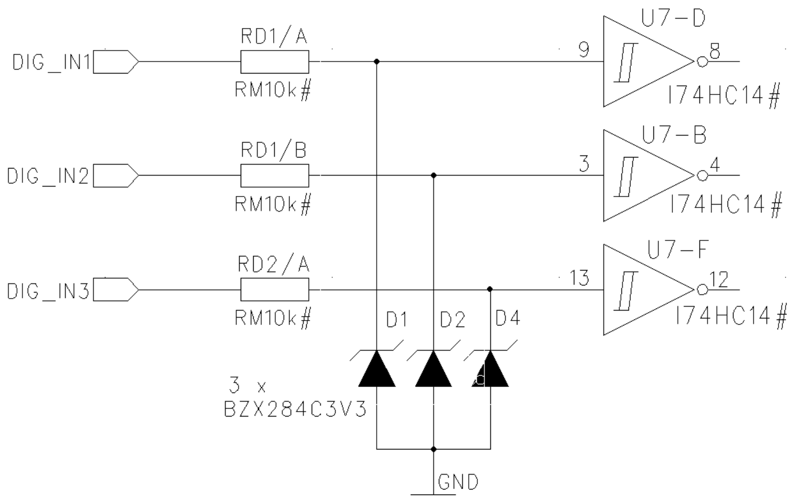
8.4.2 Analog input signal definition

The analog input is protected by a 10kΩ series resistor.



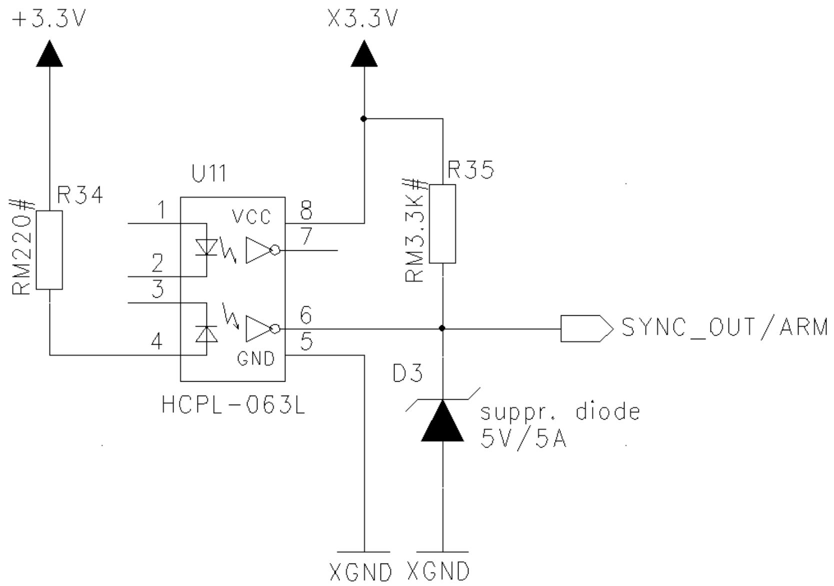
8.4.3 Digital Inputs 1-3 signal definition

The signals DIG IN1-3 are TTL input signals and are used as process signals, which are superimposed to the image. The input of the signals



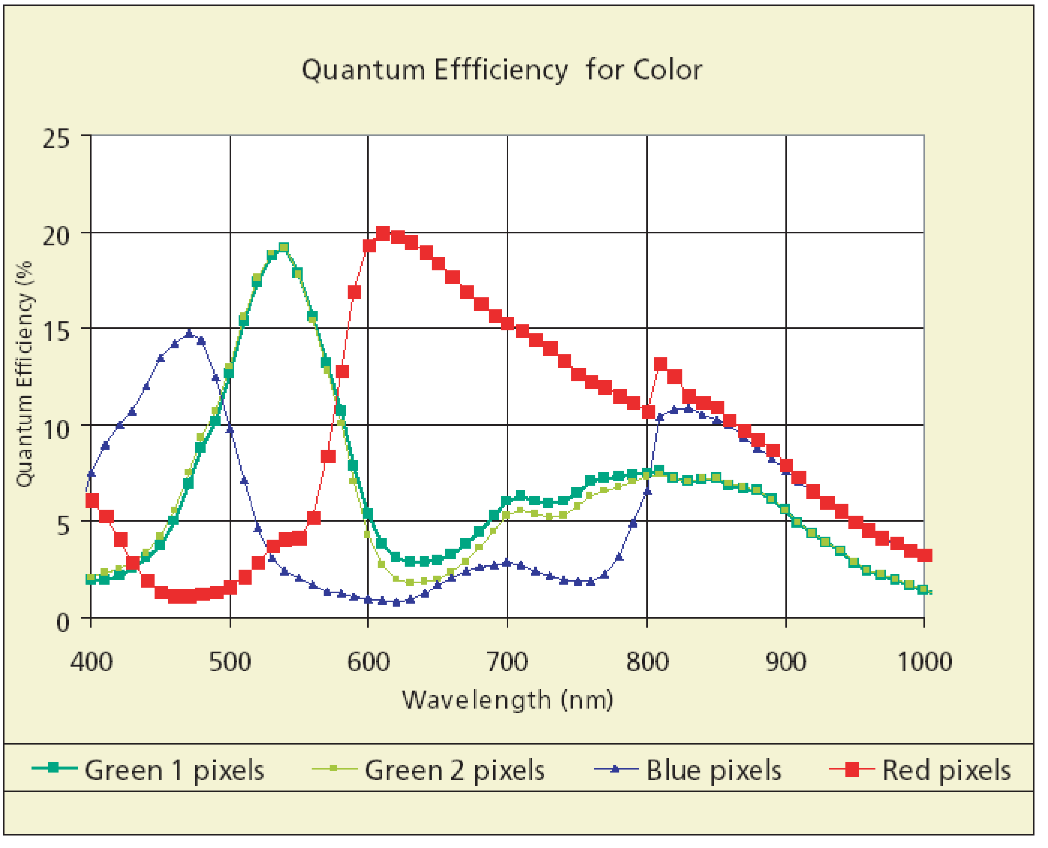
8.4.4 SYNC OUT / ARM output signal definition

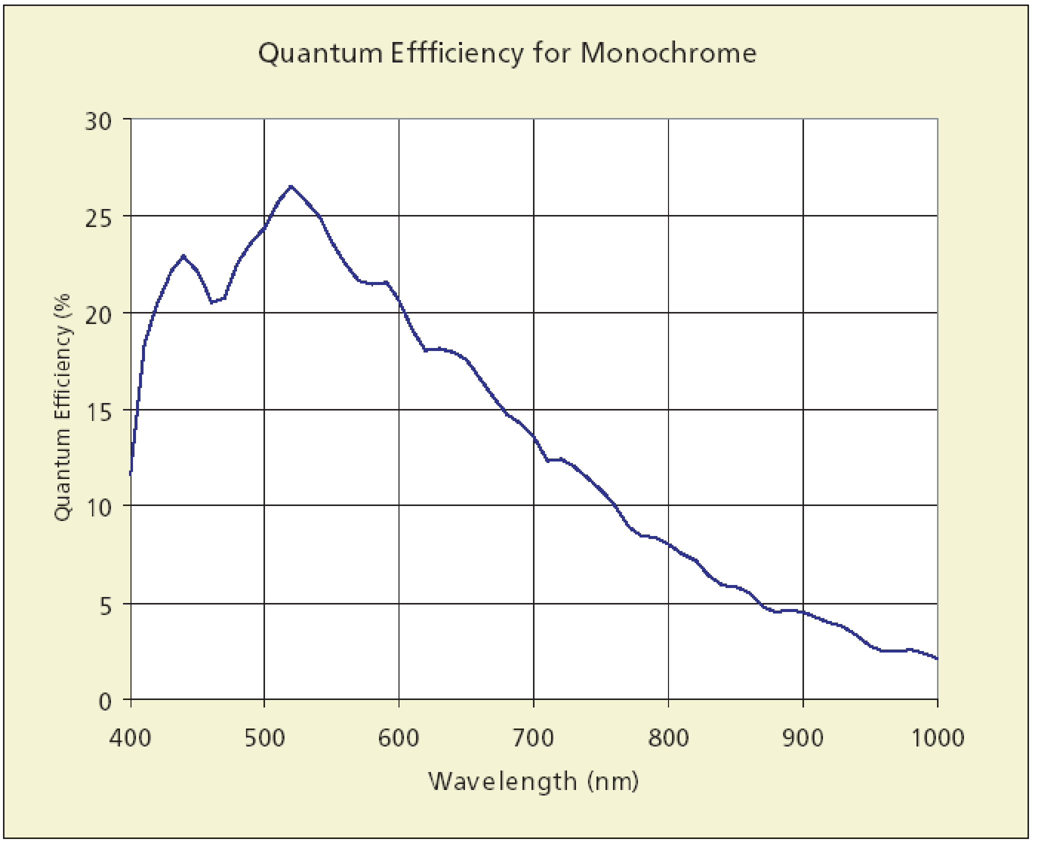
This pin can output a SYNC OUT signal or a ARM signal, which can be selected by switching register bit rf[1]. If SYNC OUT is selected, this output will carry a strobe that corresponds to the selected exposure time of the camera. If ARM is selected, it will be active if the camera runs in circular recording mode.



The optocouplers output will sink 13 mA with max. 0.6V output voltage. The output polarity is positive when the selected signal is active. The suppressor diode protects the output against reverse voltages. It starts conducting if the voltage on the output pin is greater 6V.

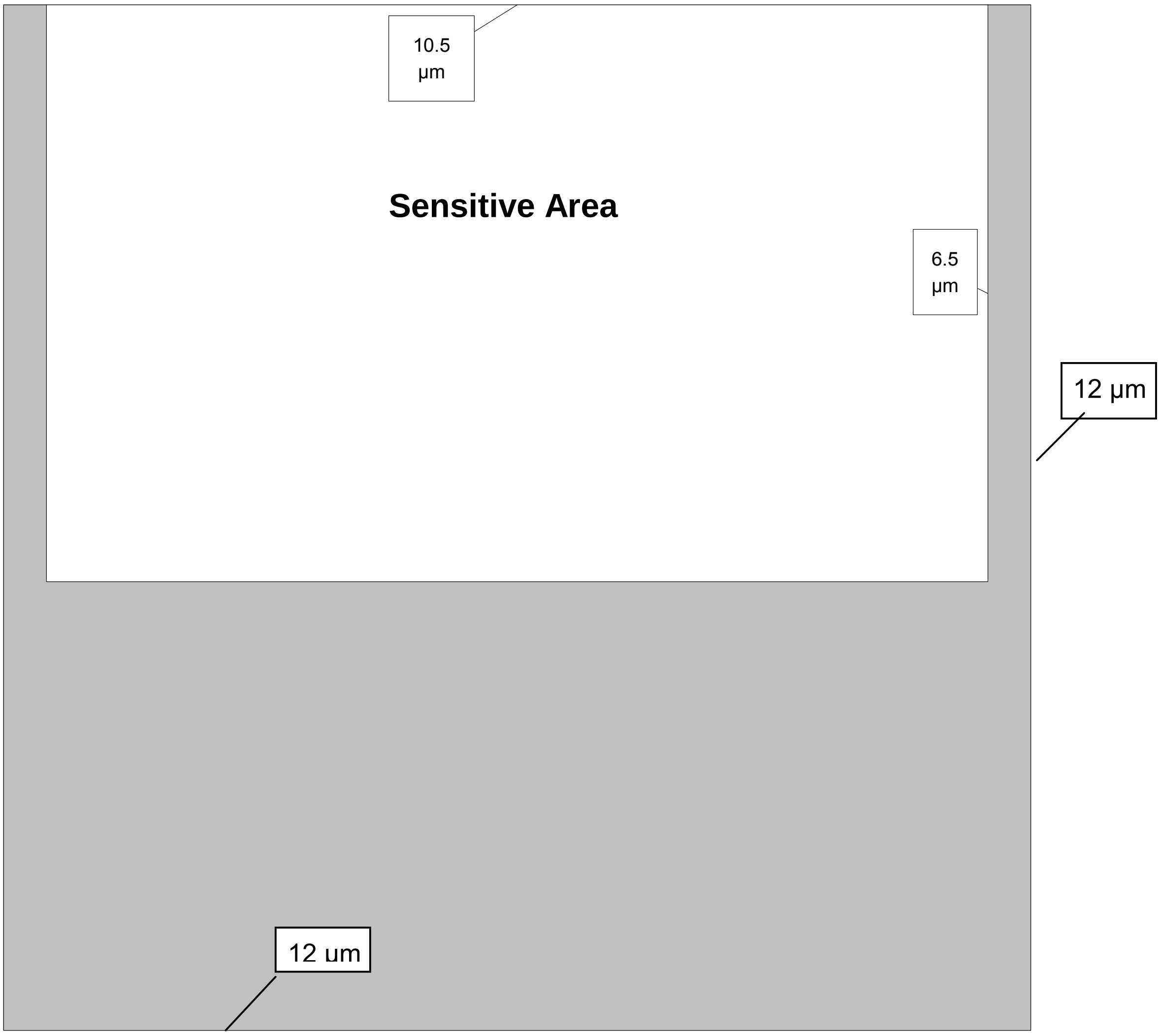
8.5 Spectral response





8.6 Sensitive area of a pixel

Pixel size: 12 x 12 µm
Fill factor: 40 %
Sensitive area: 10,5 x 6,5 µm



8.7 Frequency selection

The below selection of frequencies are examples for possible adjustments of the sensor clock in the MC133x . Any other frequency can be programmed by an arbitrary clock command.

Frequency / MHz		Code	Frequency / MHz		Code	Frequency / MHz		Code
Wanted	Real		Wanted	Real		Wanted	Real	
1.0	1.001	41bb0b	24.5	24.488	416905	48.0	47.923	409081
1.5	1.497	409301	25.0	24.986	41dd07	48.5	48.538	413084
2.0	2.002	41ba8b	25.5	25.498	41408a	49.0	48.976	416885
2.5	2.501	412685	26.0	26.010	41f090	49.5	49.503	416c85
3.0	2.995	409281	26.5	26.496	41c08e	50.0	49.971	41dc87
3.5	3.502	408e03	27.0	27.034	404c81	50.5	50.475	41580b
4.0	4.005	41ba0b	27.5	27.506	41788b	51.0	50.995	41400a
4.5	4.501	41f20b	28.0	28.017	408c83	51.5	51.610	404801
5.0	5.003	412605	28.5	28.508	41c48d	52.0	52.019	41f010
5.5	5.483	41d208	29.0	29.000	41cc8d	52.5	52.477	41d80f
6.0	5.990	409201	29.5	29.491	405481	53.0	52.992	41c00e
6.5	6.502	41f190	30.0	29.983	41dc8d	53.5	53.453	406802
7.0	7.004	408d83	30.5	30.497	416089	54.0	54.067	404c01
7.5	7.495	41dd8d	31.0	31.027	41888a	54.5	54.445	41740b
8.0	8.010	41b98b	31.5	31.502	416c89	55.0	55.012	41780b
8.5	8.499	414187	32.0	32.043	41b88b	55.5	55.513	41f40f
9.0	9.003	41f18b	32.5	32.507	417889	56.0	56.033	408c03
9.5	9.492	419188	33.0	32.914	41e88c	56.5	56.525	405001
10.0	10.006	412585	33.5	33.513	418489	57.0	57.016	41c40d
10.5	10.506	40d983	34.0	33.997	414087	57.5	57.508	409003
11.0	10.967	41d188	34.5	34.518	419089	58.0	57.999	41cc0d
11.5	11.520	40bd82	35.0	35.021	408c82	58.5	58.491	41d00d
12.0	11.981	409181	35.5	35.482	412886	59.0	58.982	405401
12.5	12.493	41dd87	36.0	36.013	41f08b	59.5	59.509	41b80c
13.0	13.005	41f110	36.5	36.495	418088	60.0	59.965	41dc0d
13.5	13.517	404d01	37.0	36.864	406c81	60.5	60.457	409803
14.0	14.008	408d03	37.5	37.478	40e884	61.0	60.993	416009
14.5	14.500	41cd0d	38.0	37.970	419088	61.5	61.440	405801
15.0	14.991	41dd0d	38.5	38.502	416c87	62.0	62.054	41880a
15.5	15.514	41890a	39.0	39.014	41f08a	62.5	62.423	41f00d
16.0	16.022	41b90b	39.5	39.497	412085	63.0	63.004	416c09
16.5	16.457	41e90c	40.0	40.024	412485	63.5	63.520	41b40b
17.0	16.998	414107	40.5	40.550	407881	64.0	64.087	41b80b
17.5	17.510	408d02	41.0	41.011	415886	64.5	64.512	408002
18.0	18.007	41f10b	41.5	41.472	40a882	65.0	65.015	417809
18.5	18.432	406d01	42.0	42.025	40d883	65.5	65.536	413407
19.0	18.985	419108	42.5	42.561	41f089	66.0	65.829	41e80c
19.5	19.507	41f10a	43.0	43.008	408081	66.5	66.355	406001
20.0	20.012	412505	43.5	43.500	40e083	67.0	67.025	418409
20.5	20.506	415906	44.0	43.868	41d088	67.5	67.489	41d00b
21.0	21.012	40d903	44.5	44.605	41d888	68.0	67.994	414007
21.5	21.504	408101	45.0	44.974	40e883	68.5	68.462	40f805
22.0	21.934	41d108	45.5	45.466	408881	69.0	69.036	419009
22.5	22.487	40e903	46.0	46.080	40bc82	69.5	69.515	40fc05
23.0	23.040	40bd02	46.5	46.541	418886	70.0	70.042	408c02
23.5	23.501	40c102	47.0	47.002	40c082			
24.0	23.962	409101	47.5	47.514	41c487			

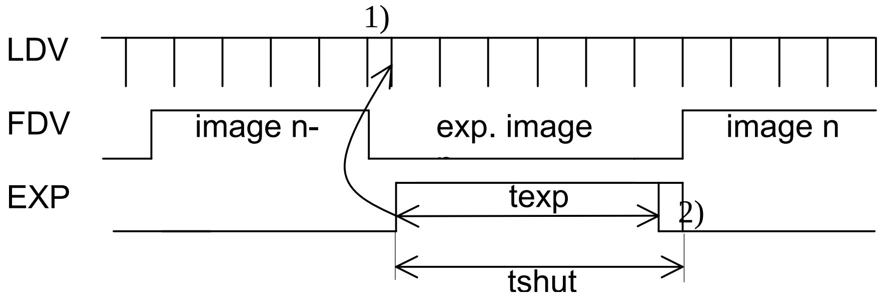
Table 8.7-1

8.8 Timing

8.8.1 Trigger Signal (EXP)

If the MC133x is set for single, asynchronously triggered images, the trigger input drives the internal EXP signal. It is positive active if register 7, Bit 8 = 0, negativ active if register 7, Bit 8 = 1. The EXP Signal may not be asserted at a frequency higher than 1/(frame time+exp time)

The sensors exposure starts and the strobe output activates (texp, (1) three sensor clocks after the active edge of the EXP signal (tshut), and ends up to 135 sensor clocks after deactivation (2).



1) The active edge of the EXP signal clears the horizontal counter.

2) End of exposure time is synchronised with the internal horizontal counter.